

FEATURES

- Flash Memory and SRAM
- Stacked Die Chip Scale Package
- 72-ball CSP (FBGA072-P-0811) plastic package
- Power supply: 2.7 V to 3.6 V
- Operating temperature: -25°C to +85°C
- Flash Memory
 - Access time (MAX.): 100 ns
 - Operating current (MAX.):
The current for F-V_{CC} pin
 - Read: 25 mA (t_{CYCLE} = 200 ns)
 - Word write: 17 mA
 - Block erase: 17 mA
 - Deep power down current (the current for F-V_{CC} pin): 10 µA (MAX. F-CE ≥ F-V_{CC} - 0.2 V, F-RP ≤ 0.2 V, F-V_{PP} ≤ 0.2 V)
 - Optimized array blocking architecture
 - Two 4K-word boot blocks
 - Six 4K-word parameter blocks

- Thirty-one 32K-word main blocks
- Top/Bottom boot location versions
- Extended cycling capability
 - 100,000 block erase cycles
- Enhanced automated suspend options
 - Word write suspend to read
 - Block erase suspend to word write
 - Block erase suspend to read
- SRAM
 - Access time (MAX.): 85 ns
 - Operating current (MAX.):
 - 45 mA
 - 8 mA (t_{RC}, t_{WC} = 1 µs)
 - Standby current: 45 µA (MAX.)
 - Data retention current: 35 µA (MAX.)

DESCRIPTION

The LRS1341/LRS1342 is a combination memory organized as 1,048,576 × 16-bit flash memory and 131,072 × 16-bit static RAM in one package.

PIN CONFIGURATION

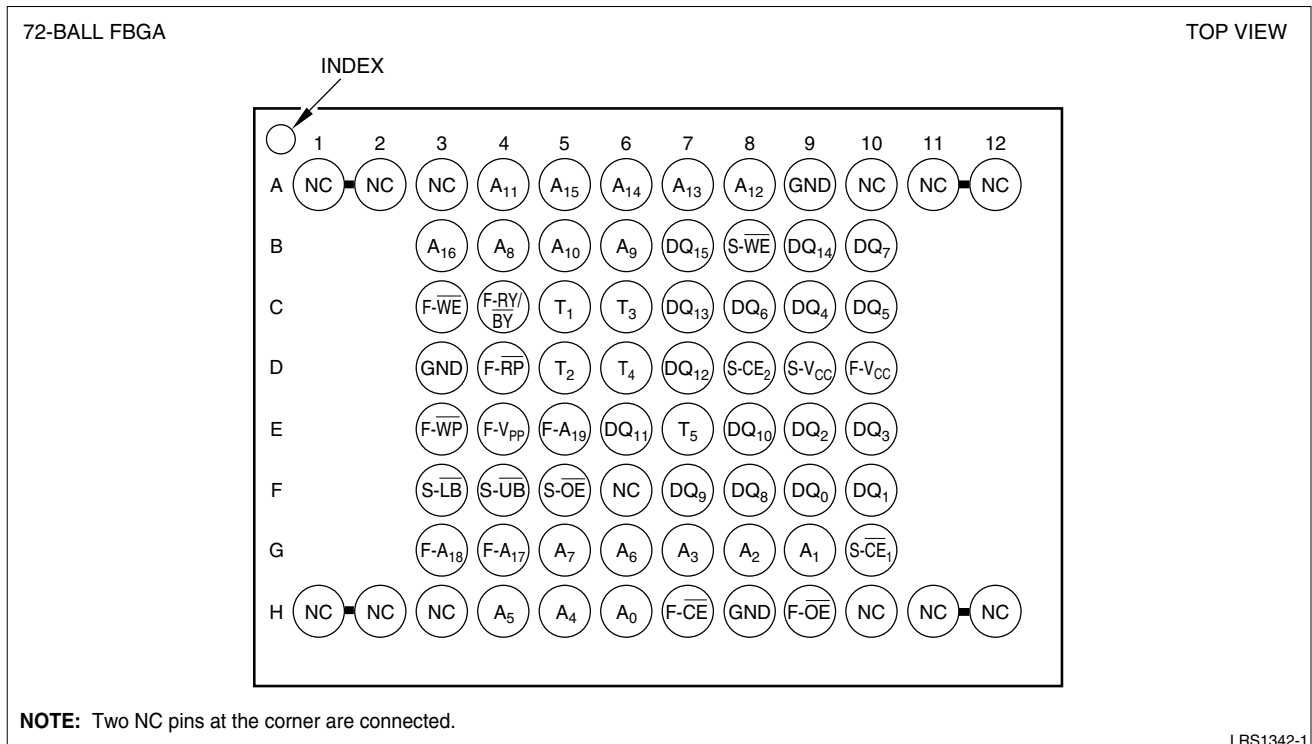


Figure 1. LRS1341/LRS1342 Pin Configuration

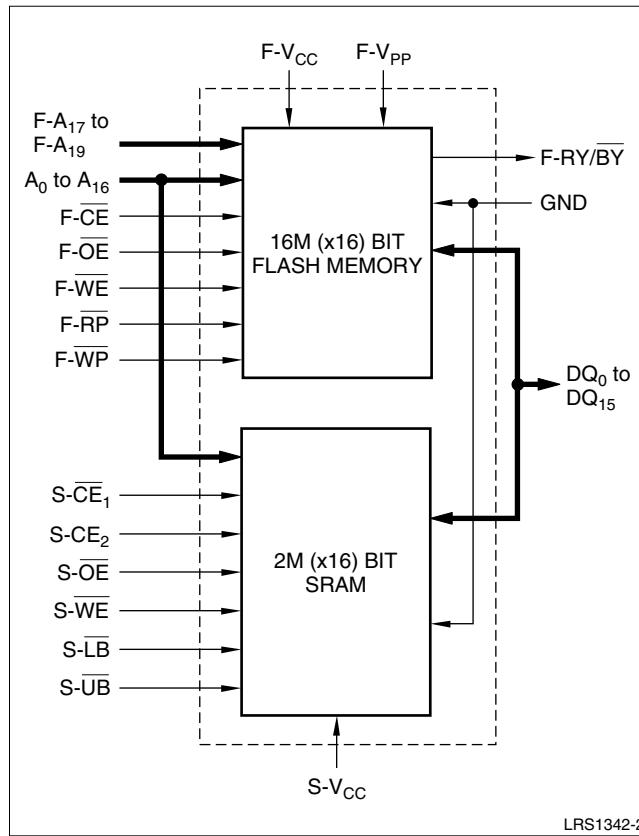


Figure 2. LRS1341/LRS1342 Block Diagram

Table 1. Pin Descriptions

PIN	DESCRIPTION	TYPE
A ₀ to A ₁₆	Address Inputs (Common)	Input
F-A ₁₇ to F-A ₁₉	Address Inputs (Flash)	Input
F- \overline{CE}	Chip Enable Input (Flash)	Input
S- \overline{CE}_1 , S-CE ₂	Chip Enable Inputs (SRAM)	Input
F- \overline{WE}	Write Enable Input (Flash)	Input
S- \overline{WE}	Write Enable Input (SRAM)	Input
F- \overline{OE}	Output Enable Input (Flash)	Input
S- \overline{OE}	Output Enable Input (SRAM)	Input
S- \overline{LB}	SRAM Byte Enable Input (DQ ₀ to DQ ₇)	Input
S- \overline{UB}	SRAM Byte Enable Input (DQ ₈ to DQ ₁₅)	Input
F- \overline{RP}	Reset/Power Down (Flash) Block erase and Word Write: V _{IH} or V _{HH} Read: V _{IH} or V _{HH} Reset/Power Down: V _{IL}	Input
F- \overline{WP}	Write Protect (Flash) Two Boot Blocks Locked: V _{IL} (with F- \overline{RP} = V _{HH}) Erase of Write can operate to all blocks)	Input
F-RY/ \overline{BY}	Ready/Busy (Flash) During an Erase or Write operation: V _{OL} Block Erase and Word Write Suspend: HIGH-Z Deep Power Down: V _{OH}	Output
DQ ₀ to DQ ₁₅	Data Input/Outputs (Common)	Input/Output
F-V _{CC}	Power Supply (Flash)	Power
S-V _{CC}	Power Supply (SRAM)	Power
F-V _{PP}	Write, Erase Power Supply (Flash) Block Erase and Word Write: F-V _{PP} = V _{PPLK} All Blocks Locked: F-V _{PP} < V _{PPLK}	Power
GND	Ground (Common)	Power
NC	No Connection	—
T ₁ to T ₅	Test Pins (Should be Open)	—

Table 2. Truth Table¹

FLASH	SRAM	F-CE	F-RP	F-OE	F-WE	S-CE ₁	S-CE ₂	S-OE	S-WE	S-LB	S-UB	DQ ₀ - DQ ₇	DQ ₈ - DQ ₁₅	NOTES
Read	Standby	L	H	L	H	See Note 4		X	X	See Note 4		D _{OUT}		2, 3
Output Disable	Standby	L	H	H	H			X	X			HIGH-Z		3
Write	Standby	L	H	H	L			X	X			D _{IN}		2, 3, 5, 6
Standby	Read	H	H	X	X	L	H	L	H	See Note 7				
	Output Disable	H	H	X	X	L	H	H	H	X	X	HIGH-Z		
		H	H	X	X	L	H	X	X	H	H	HIGH-Z		
Write	H	H	X	X	L	H	L	L	See Note 7					
Reset/Power Down	Read	X	L	X	X	L	H	L	H	See Note 7				
	Output Disable	X	L	X	X	L	H	H	H	X	X	HIGH-Z		
		X	L	X	X	L	H	X	X	H	H	HIGH-Z		
Write	X	L	X	X	L	H	L	L	See Note 7					
Standby	Standby	H	H	X	X	See Note 4		X	X	See Note 4		HIGH-Z		3
Reset/Power Down	Standby	X	L	X	X			X	X			HIGH-Z		3

NOTES:

- L = V_{IL}, H = V_{IH}, X = H or L. Refer to DC Characteristics.
- Refer to the 'Flash Memory Command Definition' section for valid D_{IN} during a write operation.
- F-WP set to V_{IL} or V_{IH}.
- SRAM standby mode. See Table 2a.
- Command writes involving block erase or word write are reliably executed when F-V_{PP} = V_{PPH} and F-V_{CC} = 2.7 V to 3.6 V. Block erase or word write with V_{IH} < RP < V_{HH} produce spurious results and should not be attempted.
- Never hold F-OE LOW and F-WE LOW at the same time.
- S-LB, S-UB control mode. See Table 2b.

Table 2a.

MODE	PINS			
	S-CE ₁	S-CE ₂	S-LB	S-UB
Standby (SRAM)	H	X	X	X
	X	L	X	X
	X	X	H	H

Table 2b.

MODE (SRAM)	PINS			
	S-LB	S-UB	DQ ₀ - DQ ₇	DQ ₈ - DQ ₁₅
Read/Write	L	L	D _{OUT} /D _{IN}	D _{OUT} /D _{IN}
	L	H	D _{OUT} /D _{IN}	HIGH-Z
	H	L	HIGH-Z	D _{OUT} /D _{IN}

Table 3. Command Definition for Flash Memory¹

COMMAND	BUS CYCLES REQUIRED	FIRST BUS CYCLE			SECOND BUS CYCLE			NOTES
		OPERATION ²	ADDRESS ³	DATA ³	OPERATION ²	ADDRESS ³	DATA ³	
Read Array/Reset	1	Write	XA	FFH				
Read Identifier Codes	≥ 2	Write	XA	90H	Read	IA	ID	4
Read Status Register	2	Write	XA	70H	Read	XA	SRD	
Clear Status Register	1	Write	XA	50H				
Block Erase	2	Write	BA	20H	Write	BA	D0H	5
Word Write	2	Write	WA	40H or 10H	Write	WA	WD	5
Block Erase and Word Write Suspend	1	Write	XA	B0H				5
Block Erase and Word Write Resume	1	Write	XA	D0H				5

NOTES:

- Commands other than those shown in table are reserved by SHARP for future device implementations and should not be used.
- BUS operations are defined in Table 2.
- XA = Any valid address within the device;
IA = Identifier code address;
BA = Address within the block being erased;
- WA = Address of memory location to be written;
SRD = Data read from status register, see Table 6;
WD = Data to be written at location WA. Data is latched on the rising edge of F-WE or F-CE (whichever goes high first);
ID = Data read from identifier codes.
- See Table 4 for Identifier Codes.
See Table 5 for Write Protection Alternatives.

Table 4. Identifier Codes

CODES	ADDRESS (A ₀ - A ₁₈)	LRS1341 DATA (DQ ₀ - DQ ₇)	LRS1342 DATA (DQ ₀ - DQ ₇)
Manufacture Code	00000H	B0H	B0H
Device Code	00001H	48H	49H

Table 5. Write Protection Alternatives

OPERATION	F-V _{PP}	F-R _P	F-W _P	EFFECT
Block Erase or Word Write	V _{IL}	X	X	All blocks locked
	> V _{PPLK}	V _{IL}	X	All blocks locked
		V _{HH}	X	All blocks unlocked
		V _{IH}	V _{IL}	Two boot blocks locked
		V _{IH}	V _{IH}	All blocks unlocked

Table 6. Status Register Definition

WSMS	ESS	ES	WWS	VPPS	WWSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = Write State Machine Status (WSMS)

- 1 = Ready
- 0 = Busy

SR.6 = Erase Suspend Status (ESS)

- 1 = Block Erase Suspended
- 0 = Block Erase in Progress/Completed

SR.5 = Erase Status (ES)

- 1 = Error in Block Erasure
- 0 = Successful Block Erase

SR.4 = Word Write Status (WWS)

- 1 = Error in Word Write
- 0 = Successful Word Write

SR.3 = V_{PP} Status (VPPS)

- 1 = F-V_{PP} LOW Detect, Operation Abort
- 0 = F-V_{PP} Okay

SR.2 = Word Write Suspend Status (WWSS)

- 1 = Word Write Suspended
- 0 = Word Write in Progress/Completed

SR.1 = Device Protect Status (DPS)

- 1 = F-W_P and/or F-R_P Lock Detected,
Operation Abort
- 0 = Unlock

SR.0 = Reserved for future enhancements (R)

NOTES:

1. Check RY/ $\overline{\text{BY}}$ or SR.7 to determine block erase or word write completion. SR.6 - SR.0 are invalid while SR.7 = 0.
2. If both SR.5 and SR.4 are '1's after a block erase attempt, an improper command sequence was entered.
3. SR.3 does not provide a continuous indication of F-V_{PP} level. The WSM interrogates and indicates the F-V_{PP} level only after Block Erase or Word Write command sequences. SR.3 is not guaranteed to report accurate feedback only when F-V_{PP} ≠ V_{PPH1}, V_{PPH2}.
4. The WSM interrogates the F-W_P and F-R_P only after Block Erase or Word Write command sequences. It informs the system, depending on the attempted operation, if the F-W_P is not V_{IH} or F-R_P is not V_{HH}.
5. SR.0 is reserved for future use and should be masked out when polling the status register.

MEMORY MAPS

[A ₀ - A ₁₉]		
FFFF		
F8000	32K-WORD MAIN BLOCK	30
F7FFF	32K-WORD MAIN BLOCK	29
F0000		
EFFFF	32K-WORD MAIN BLOCK	28
E8000		
E7FFF	32K-WORD MAIN BLOCK	27
E0000		
DFFFF	32K-WORD MAIN BLOCK	26
D8000		
D7FFF	32K-WORD MAIN BLOCK	25
D0000		
CFFFF	32K-WORD MAIN BLOCK	24
C8000		
C7FFF	32K-WORD MAIN BLOCK	23
C0000		
BFFFF	32K-WORD MAIN BLOCK	22
B8000		
B7FFF	32K-WORD MAIN BLOCK	21
B0000		
AFFFF	32K-WORD MAIN BLOCK	20
A8000		
A7FFF	32K-WORD MAIN BLOCK	19
A0000		
9FFFF	32K-WORD MAIN BLOCK	18
98000		
97FFF	32K-WORD MAIN BLOCK	17
90000		
8FFFF	32K-WORD MAIN BLOCK	16
88000		
87FFF	32K-WORD MAIN BLOCK	15
80000		
7FFFF	32K-WORD MAIN BLOCK	14
78000		
77FFF	32K-WORD MAIN BLOCK	13
70000		
6FFFF	32K-WORD MAIN BLOCK	12
68000		
67FFF	32K-WORD MAIN BLOCK	11
60000		
5FFFF	32K-WORD MAIN BLOCK	10
58000		
57FFF	32K-WORD MAIN BLOCK	9
50000		
4FFFF	32K-WORD MAIN BLOCK	8
48000		
47FFF	32K-WORD MAIN BLOCK	7
40000		
3FFFF	32K-WORD MAIN BLOCK	6
38000		
37FFF	32K-WORD MAIN BLOCK	5
30000		
2FFFF	32K-WORD MAIN BLOCK	4
28000		
27FFF	32K-WORD MAIN BLOCK	3
20000		
1FFFF	32K-WORD MAIN BLOCK	2
18000		
17FFF	32K-WORD MAIN BLOCK	1
10000		
0FFFF	32K-WORD MAIN BLOCK	0
08000		
07FFF	4K-WORD PARAMETER BOOT BLOCK	5
07000		
06FFF	4K-WORD PARAMETER BOOT BLOCK	4
06000		
05FFF	4K-WORD PARAMETER BOOT BLOCK	3
05000		
04FFF	4K-WORD PARAMETER BOOT BLOCK	2
04000		
03FFF	4K-WORD PARAMETER BOOT BLOCK	1
03000		
02FFF	4K-WORD PARAMETER BOOT BLOCK	0
02000		
01FFF	4K-WORD BOOT BLOCK	1
01000		
00FFF	4K-WORD BOOT BLOCK	0
00000		

BOTTOM BOOT

LRS1342-3

Figure 3. Bottom Boot for Flash Memory

[A ₀ - A ₁₉]		
FFFF		
F8000	4K-WORD BOOT BLOCK	0
F7FFF		
F0000	4K-WORD BOOT BLOCK	1
EFFFF		
E8000	4K-WORD PARAMETER BOOT BLOCK	0
E7FFF		
E0000	4K-WORD PARAMETER BOOT BLOCK	1
DFFFF		
D8000	4K-WORD PARAMETER BOOT BLOCK	2
D7FFF		
D0000	4K-WORD PARAMETER BOOT BLOCK	3
CFFFF		
C8000	4K-WORD PARAMETER BOOT BLOCK	4
C7FFF		
C0000	4K-WORD PARAMETER BOOT BLOCK	5
BFFFF		
B8000	32K-WORD MAIN BLOCK	0
B7FFF		
B0000	32K-WORD MAIN BLOCK	1
AFFFF		
A8000	32K-WORD MAIN BLOCK	2
A7FFF		
A0000	32K-WORD MAIN BLOCK	3
9FFFF		
98000	32K-WORD MAIN BLOCK	4
97FFF		
90000	32K-WORD MAIN BLOCK	5
8FFFF		
88000	32K-WORD MAIN BLOCK	6
87FFF		
80000	32K-WORD MAIN BLOCK	7
7FFFF		
78000	32K-WORD MAIN BLOCK	8
77FFF		
70000	32K-WORD MAIN BLOCK	9
6FFFF		
68000	32K-WORD MAIN BLOCK	10
67FFF		
60000	32K-WORD MAIN BLOCK	11
5FFFF		
58000	32K-WORD MAIN BLOCK	12
57FFF		
50000	32K-WORD MAIN BLOCK	13
4FFFF		
48000	32K-WORD MAIN BLOCK	14
47FFF		
40000	32K-WORD MAIN BLOCK	15
3FFFF		
38000	32K-WORD MAIN BLOCK	16
37FFF		
30000	32K-WORD MAIN BLOCK	17
2FFFF		
28000	32K-WORD MAIN BLOCK	18
27FFF		
20000	32K-WORD MAIN BLOCK	19
1FFFF		
18000	32K-WORD MAIN BLOCK	20
17FFF		
10000	32K-WORD MAIN BLOCK	21
0FFFF		
08000	32K-WORD MAIN BLOCK	22
07FFF		
07000	32K-WORD MAIN BLOCK	23
06FFF		
06000	32K-WORD MAIN BLOCK	24
05FFF		
05000	32K-WORD MAIN BLOCK	25
04FFF		
04000	32K-WORD MAIN BLOCK	26
03FFF		
03000	32K-WORD MAIN BLOCK	27
02FFF		
02000	32K-WORD MAIN BLOCK	28
01FFF		
01000	32K-WORD MAIN BLOCK	29
00FFF		
00000	32K-WORD MAIN BLOCK	30

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Figure 4. Top Boot for Flash Memory

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT	NOTES
Supply voltage	V_{CC}	-0.2 to +3.9	V	1, 2
Input voltage	V_{IN}	-0.2 to $V_{CC} + 0.3$	V	1, 3, 4
Operating temperature	T_{OPR}	-25 to +85	°C	
Storage temperature	T_{STG}	-55 to +125	°C	
F- V_{PP} voltage	F- V_{PP}	-0.2 to +14.0	V	1, 4, 5
F- \overline{RP} voltage	F- \overline{RP}	-0.5 to +14.0	V	1, 4, 5

NOTES:

1. The maximum applicable voltage on any pins with respect to GND.
2. Except F- V_{PP} .
3. Except F- \overline{RP} .
4. -2.0 V undershoot is allowed when the pulse width is less than 20 ns.
5. +14.0 V overshoot is allowed when the pulse width is less than 20 ns.

RECOMMENDED DC OPERATING CONDITIONS

$$T_A = -25^\circ\text{C to } +85^\circ\text{C}$$

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
Input voltage	V_{IH}	2.2		$V_{CC} + 0.2$	V	1
	V_{IL}	-0.2		0.6	V	2
	V_{HH}	11.4		12.6	V	3

NOTES:

1. V_{CC} is the lower one of S- V_{CC} and F- V_{CC} .
2. -2.0 V undershoot is allowed when the pulse width is less than 20 ns.
3. This voltage is applicable to F- \overline{RP} pin only.

PIN CAPACITANCE

$$T_A = 25^\circ\text{C, } f = 1 \text{ MHz}$$

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input capacitance*	C_{IN}	$V_{IN} = 0 \text{ V}$			20	pF
I/O capacitance*	$C_{I/O}$	$V_{I/O} = 0 \text{ V}$			22	pF

NOTE: *Sampled by not 100% tested.

DC CHARACTERISTICS

 $T_A = -25^{\circ}\text{C to } +85^{\circ}\text{C}, V_{CC} = 2.7\text{ V to } 3.6\text{ V}$

PARAMETER		SYMBOL	CONDITION	MIN.	TYP. ¹	MAX.	UNIT	NOTES	
Input leakage current		I_{LI}	$V_{IN} = V_{CC}$ or GND	-1.5		+1.5	μA		
Output leakage current		I_{LO}	$V_{OUT} = V_{CC}$ or GND	-1.5		+1.5	μA		
F- V_{CC}	Standby Current	I_{CCS}	F- $\overline{CE} = F\text{-}\overline{RP} = F\text{-}V_{CC} \pm 0.2\text{ V}$ F- $\overline{WP} = F\text{-}V_{CC} \pm 0.2\text{ V}$ or F-GND $\pm 0.2\text{ V}$		25	50	μA	2	
			F- $\overline{CE} = F\text{-}\overline{RP} = V_{IH}$, F- $\overline{WP} = V_{IH}$ or V_{IL}		0.2	2	mA		
	Deep Power-Down Current	I_{CCD}	F- $\overline{RP} = F\text{-}GND \pm 0.2\text{ V}$, $I_{OUT} (F\text{-}RY/BY) = 0\text{ mA}$		5	10	μA		
	Read Current	I_{CCR}	CMOS input, F- $\overline{CE} = F\text{-}GND$, $f = 5\text{ MHz}$, $I_{OUT} = 0\text{ mA}$				25	mA	3, 4
			TTL input, F- $\overline{CE} = F\text{-}GND$, $f = 5\text{ MHz}$, $I_{OUT} = 0\text{ mA}$				30	mA	3, 4
	Word Write Current	I_{CCW}	F- $V_{PP} = 2.7\text{ V to } 3.6\text{ V}$				17	mA	
			F- $V_{PP} = 11.4\text{ V to } 12.6\text{ V}$				12	mA	
Block Erase Current	I_{CCE}	F- $V_{PP} = 2.7\text{ V to } 3.6\text{ V}$				17	mA		
		F- $V_{PP} = 11.4\text{ V to } 12.6\text{ V}$				12	mA		
Word Write Block Erase Suspend Current	I_{CCWS} I_{CCES}	F- $\overline{CE} = V_{IH}$				6	mA		
F- V_{PP}	Standby or Read Current	I_{PPS} I_{PPR}	F- $V_{PP} = F\text{-}V_{CC}$		± 2	± 15	μA		
			F- $V_{PP} > F\text{-}V_{CC}$		10	200	μA		
	Deep Power-Down Current	I_{PPD}	F- $\overline{RP} = F\text{-}GND \pm 0.2\text{ V}$		0.1	5	μA		
	Word Write Current	I_{PPW}	F- $V_{PP} = 2.7\text{ V to } 3.6\text{ V}$		12	40	mA		
			F- $V_{PP} = 11.4\text{ V to } 12.6\text{ V}$				30	mA	
	Block Erase Current	I_{PPE}	F- $V_{PP} = 2.7\text{ V to } 3.6\text{ V}$		8	25	mA		
F- $V_{PP} = 11.4\text{ V to } 12.6\text{ V}$						20	mA		
Word Write or Block Erase Suspend Current	I_{PPWS} I_{PPES}	F- $V_{PP} = V_{PPH}$		10	200	μA			
S- V_{CC}	Standby Current	I_{SB}	S- \overline{CE}_1 , S- $\overline{CE}_2 \geq S\text{-}V_{CC} - 0.2\text{ V}$ or S- $\overline{CE}_2 \leq 0.2\text{ V}$			45	μA		
			S- $\overline{CE}_1 = V_{IH}$ or S- $\overline{CE}_2 = V_{IL}$			3	mA		
	Operation Current	I_{CC1}	S- $\overline{CE}_1 = V_{IL}$, S- $\overline{CE}_2 = V_{IH}$, $V_{IN} = V_{IL}$ or V_{IH} , $t_{CYCLE} = \text{MIN.}$, $I_{IO} = 0\text{ mA}$				45	mA	
			S- $\overline{CE}_1 = 0.2\text{ V}$, S- $\overline{CE}_2 = S\text{-}V_{CC} - 0.2\text{ V}$, $V_{IN} = S\text{-}V_{CC} - 0.2\text{ V}$, or 0.2 V $t_{CYCLE} = 1\text{ }\mu\text{s}$, $I_{IO} = 0\text{ mA}$				8	mA	
Input LOW Voltage	V_{IL}		-0.2		0.6	V			
Input HIGH Voltage	V_{IH}		2.2		$V_{CC} + 0.2$	V			
Output LOW Voltage	V_{OL}	$I_{OL} = 0.5\text{ mA}$			0.4	V	2		
Output HIGH Voltage (CMOS)	V_{OH1}	$I_{OH} = -0.5\text{ mA}$	2.2			V	2		
F- V_{PP} Lockout during Normal Operations	V_{PPLK}				1.5	V	5		
F- V_{PP} Word Write or Block Erase Operations	V_{PPH1}		2.7		3.6	V			
	V_{PPH2}		11.4		12.6	V			
F- V_{CC} Lockout Voltage	V_{LKO}		1.5			V			
F- \overline{RP} Unlock Voltage	V_{HH}	Unavailable F- \overline{WP}	11.4		12.6	V	6		

NOTES:

- Reference values at $V_{CC} = 3.0\text{ V}$ and $T_A = +25^{\circ}\text{C}$.
- Includes F- $\overline{RY}/\overline{BY}$.
- Automatic Power Savings (APS) for Flash Memory reduces typical I_{CCR} to 3 mA at 2.7 V_{CC} in static operation.
- CMOS inputs are either $V_{CC} \pm 0.2\text{ V}$ or $GND \pm 0.2\text{ V}$. TTL inputs are either V_{IL} or V_{IH} .

- Block erases and word writes are inhibited when $F\text{-}V_{PP} \leq V_{PPLK}$ and not guaranteed in the range between V_{PPLK} (MAX.) and V_{PPH} (MIN.), and above V_{PPH} (MAX.).
- F- \overline{RP} connection to a V_{HH} supply is allowed for a maximum cumulative period of 80 hours.

FLASH MEMORY AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITION
Input pulse level	0 V to 2.7 V
Input rise and fall time	10 ns
Input and Output timing reference level	1.35 V
Output load	1TTL + C _L (30 pF)

Read Cycle

T_A = -25°C to +85°C, V_{CC} = 2.7 V to 3.6 V

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read Cycle Time	t _{AVAV}	100		ns
Address to Output Delay	t _{AVQV}		100	ns
F- $\overline{\text{CE}}$ to Output Delay*	t _{ELQV}		100	ns
F- $\overline{\text{RP}}$ HIGH to Output Delay	t _{PHQV}		10	μs
F- $\overline{\text{OE}}$ to Output Delay*	t _{GLQV}		45	ns
F- $\overline{\text{CE}}$ to Output in LOW-Z	t _{ELQX}	0		ns
F- $\overline{\text{CE}}$ HIGH to Output in HIGH-Z	t _{EHQZ}		45	ns
F- $\overline{\text{OE}}$ to Output in LOW Z	t _{GLQX}	0		ns
F- $\overline{\text{OE}}$ HIGH to Output in HIGH-Z	t _{GHQZ}		20	ns
Output Hold from Address, F- $\overline{\text{CE}}$ or F- $\overline{\text{OE}}$ change, whichever occurs first	t _{OH}	0		ns

NOTE: *F- $\overline{\text{OE}}$ may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of F- $\overline{\text{CE}}$ without impact on t_{ELQV}.

Write Cycle (F- $\overline{\text{WE}}$ Controlled)¹
 $T_A = -25^\circ\text{C to } +85^\circ\text{C}, V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write Cycle Time	t_{AVAV}	100		ns
F- $\overline{\text{RP}}$ HIGH Recovery to F- $\overline{\text{WE}}$ going to LOW	t_{PHWL}	10		μs
F- $\overline{\text{CE}}$ Setup to F- $\overline{\text{WE}}$ going LOW	t_{ELWL}	0		ns
F- $\overline{\text{WE}}$ Pulse Width	t_{WLWH}	50		ns
F- $\overline{\text{RP}}$ V_{HH} Setup to F- $\overline{\text{WE}}$ going HIGH	t_{PHHWH}	100		ns
F- $\overline{\text{WP}}$ V_{IH} Setup to F- $\overline{\text{WE}}$ going HIGH	t_{SHWH}	100		ns
F- V_{PP} Setup to F- $\overline{\text{WE}}$ going HIGH	t_{VPWH}	100		ns
Address Setup to F- $\overline{\text{WE}}$ going HIGH ²	t_{AVWH}	50		ns
Data Setup to F- $\overline{\text{WE}}$ going HIGH ²	t_{DVWH}	50		ns
Data Hold from F- $\overline{\text{WE}}$ HIGH	t_{WHDX}	0		ns
Address Hold from F- $\overline{\text{WE}}$ HIGH	t_{WHAX}	0		ns
F- $\overline{\text{CE}}$ Hold from F- $\overline{\text{WE}}$ HIGH	t_{WHEH}	0		ns
F- $\overline{\text{WE}}$ Pulse Width HIGH	t_{WHWL}	30		ns
F- $\overline{\text{WE}}$ HIGH to F-RY/ $\overline{\text{BY}}$ going LOW	t_{WHRL}		100	ns
Write Recovery before Read	t_{WHGL}	0		ns
F- V_{PP} Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ HIGH-Z	t_{QVVL}	0		ns
F- $\overline{\text{RP}}$ V_{HH} Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ HIGH-Z	t_{QVPH}	0		ns
F- $\overline{\text{WP}}$ V_{IH} Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ HIGH	t_{QVSL}	0		ns

NOTES:

1. Read timing characteristics during block erase and word write operations are the same as during read-only operations. Refer to AC Characteristics for Read Cycle.
2. Refer to the 'Flash Memory Command Definition' section for valid A_{IN} and D_{IN} for block erase or word write.

Write Cycle (F- $\overline{\text{CE}}$ Controlled)¹ $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 2.7\text{ V}$ to 3.6 V

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write Cycle Time	t_{AVAV}	100		ns
F- $\overline{\text{RP}}$ HIGH Recovery to F- $\overline{\text{CE}}$ going to LOW	t_{PHEL}	10		μs
F- $\overline{\text{WE}}$ Setup to F- $\overline{\text{CE}}$ going LOW	t_{WLEL}	0		ns
F- $\overline{\text{CE}}$ Pulse Width	t_{ELEH}	70		ns
F- $\overline{\text{RP}}$ V_{HH} Setup to F- $\overline{\text{CE}}$ going HIGH	t_{PHEH}	100		ns
F- $\overline{\text{WP}}$ V_{IH} Setup to F- $\overline{\text{CE}}$ going HIGH	t_{SHEH}	100		ns
F- V_{PP} Setup to F- $\overline{\text{CE}}$ going HIGH	t_{VPEH}	100		ns
Address Setup to F- $\overline{\text{CE}}$ going HIGH ²	t_{AVEH}	50		ns
Data Setup to F- $\overline{\text{CE}}$ going HIGH ²	t_{DVEH}	50		ns
Data Hold from F- $\overline{\text{CE}}$ HIGH	t_{EHDX}	0		ns
Address Hold from F- $\overline{\text{CE}}$ HIGH	t_{EHAX}	0		ns
F- $\overline{\text{WE}}$ Hold from F- $\overline{\text{CE}}$ HIGH	t_{EHWH}	0		ns
F- $\overline{\text{CE}}$ Pulse Width HIGH	t_{EHEL}	25		ns
F- $\overline{\text{CE}}$ HIGH to F-RY/ $\overline{\text{BY}}$ going LOW	t_{EHRL}		100	ns
Write Recovery before Read	t_{EHGL}	0		ns
F- V_{PP} Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ HIGH-Z	t_{QVVL}	0		ns
F- $\overline{\text{RP}}$ V_{HH} Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ HIGH-Z	t_{QVPH}	0		ns
F- $\overline{\text{WP}}$ V_{IH} Hold from Valid SRD, F-RY/ $\overline{\text{BY}}$ HIGH	t_{QVSL}	0		ns

NOTES:

- Read timing characteristics during block erase and word write operations are the same as during read-only operations. Refer to AC Characteristics for Read Cycle.
- Refer to the 'Flash Memory Command Definition' section for valid A_{IN} and D_{IN} for block erase or word write.

Block Erase and Word Write Performance $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 2.7\text{ V}$ to 3.6 V

SYMBOL	PARAMETER	$V_{PP} = 2.7\text{ V to }3.6\text{ V}$			$V_{PP} = 11.4\text{ V to }12.6\text{ V}$			UNIT	NOTES
		MIN.	TYP. ¹	MAX.	MIN.	TYP. ¹	MAX.		
t_{WHQV1}	Word Write Time 32K-word Block		55			15		μs	2
t_{EHQV1}	Word Write Time 4K-word Block		60			30		μs	2
	Block Write Time 32K-word Block		1.8			0.6		s	2
	Block Write Time 4K-word Block		0.3			0.2		s	2
t_{WHQV2}	Block Erase Time 32K-word Block		1.2			0.7		s	2
t_{EHQV2}	Block Erase Time 4K-word Block		0.5			0.5		s	2
t_{WHRZ1} t_{EHRZ1}	Word Write Suspend Latency Time to Read		7.5	8.6		6.5	7.5	μs	
t_{WHRZ2} t_{EHRZ2}	Erase Suspend Latency Time to Read		19.3	23.6		11.8	15	μs	

NOTES:

- Reference values at $T_A = +25^\circ\text{C}$ and $V_{CC} = 3.0\text{ V}$, $V_{PP} = 3.0\text{ V}$.
- Excludes system-level overhead.

FLASH MEMORY AC CHARACTERISTICS TIMING DIAGRAMS

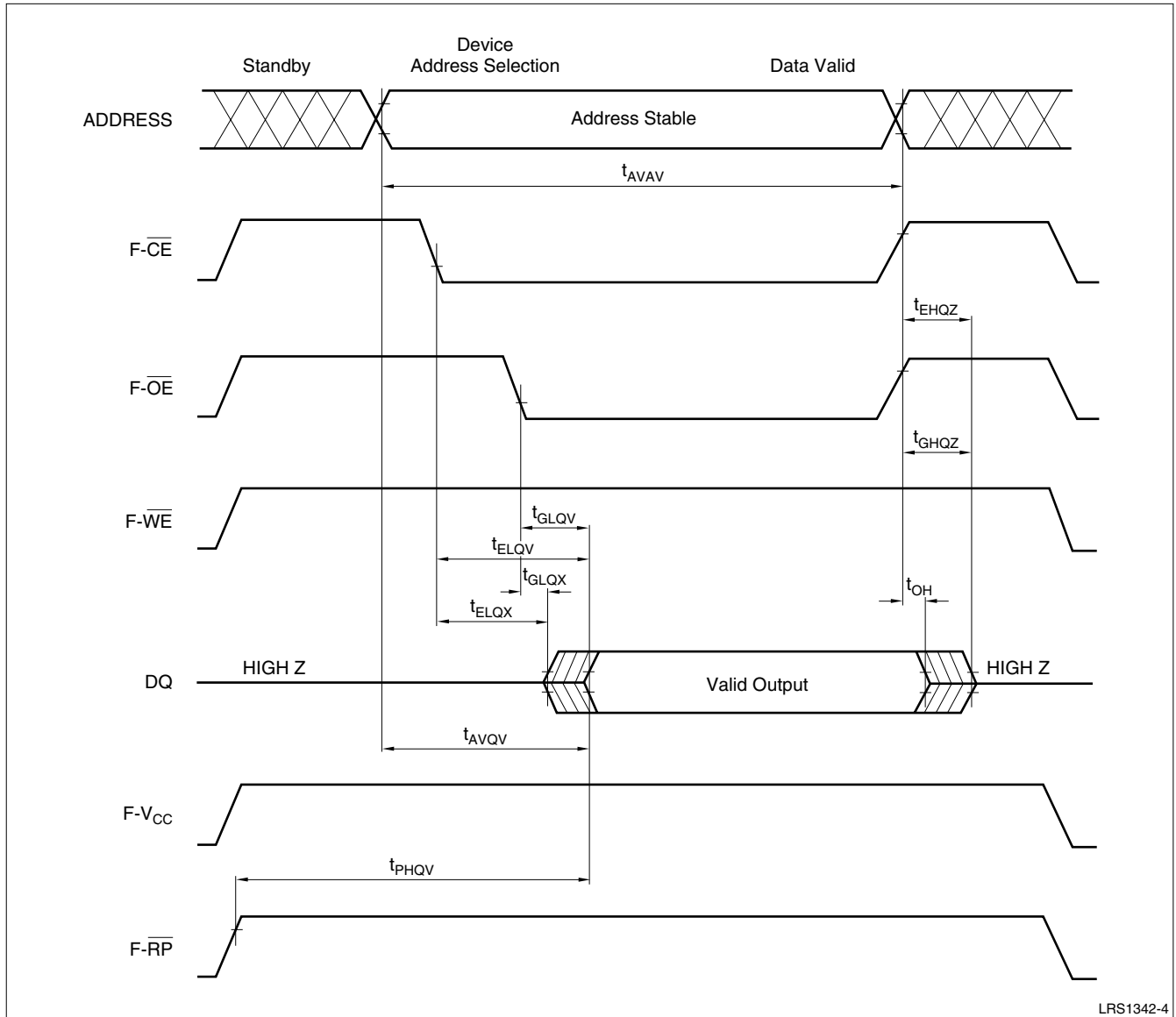


Figure 5. Read Cycle Timing Diagram

LRS1342-4

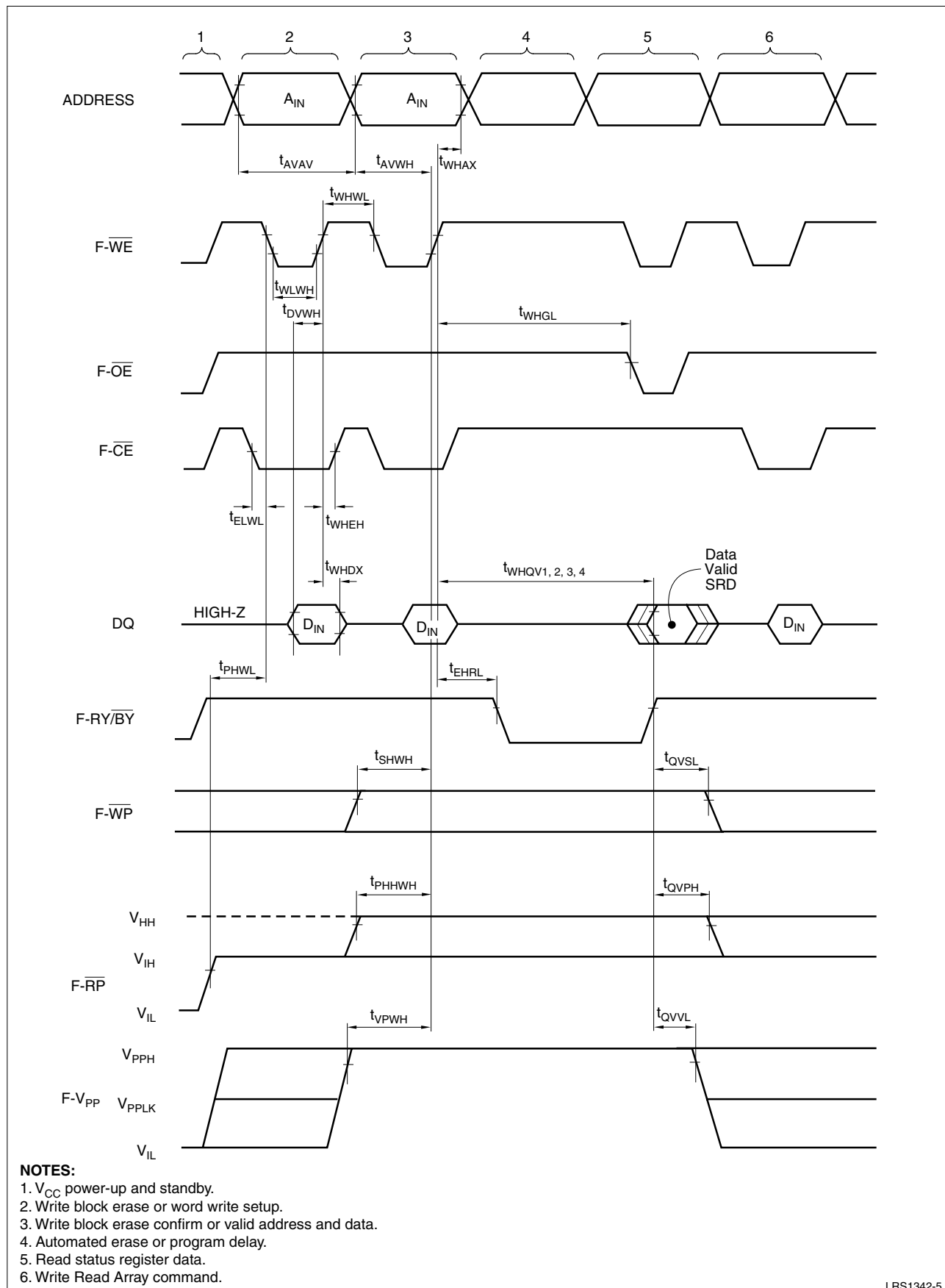
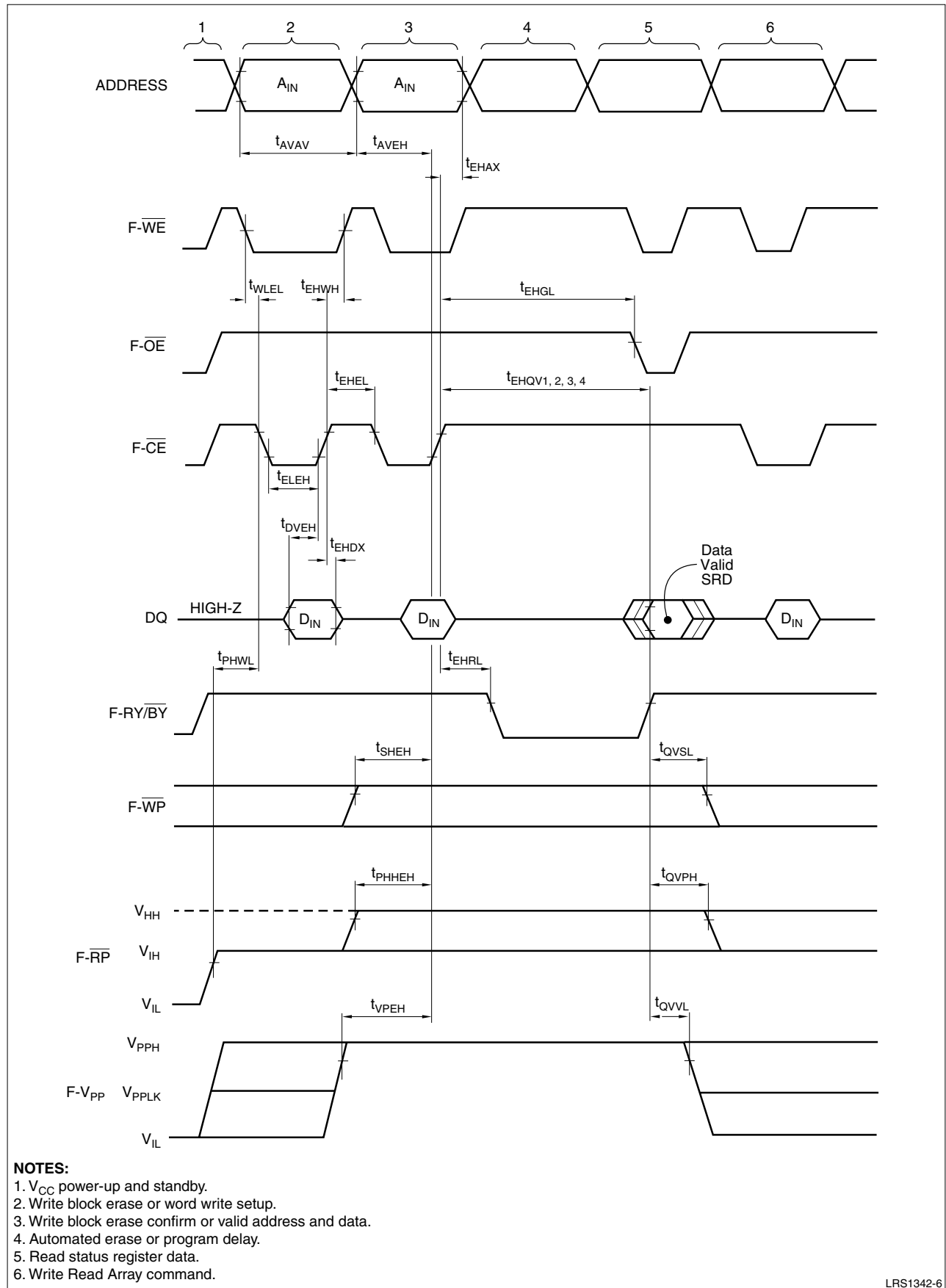


Figure 6. Write Cycle Timing Diagram (F-WE Controlled)



LRS1342-6

Figure 7. Write Cycle Timing Diagram ($F\text{-}\overline{CE}$ Controlled)

RESET OPERATIONS

$T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 2.7\text{ V}$ to 3.6 V

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTES
F- $\overline{\text{RP}}$ Pulse LOW Time (if F- $\overline{\text{RP}}$ is tied to V_{CC} , this specification is not applicable).	t_{PLPH}	100		ns	
F- $\overline{\text{RP}}$ LOW to Reset during Block Erase or Word Write	t_{PLRZ}		23.6	μs	1, 2
F- V_{CC} 2.7 V to F- $\overline{\text{RP}}$ HIGH	t_{VPH}	100		ns	3

NOTES:

- If F- $\overline{\text{RP}}$ is asserted while a block erase or word write operation is not executing, the reset will complete with 100 ns.
- A reset time t_{PHQV} is required from the later of F-RY/ $\overline{\text{BY}}$ going HIGH-Z, or F- $\overline{\text{RP}}$ going HIGH until outputs are valid.
- When the device power-up, holding F- $\overline{\text{RP}}$ LOW minimum 100 ns is required after V_{CC} has been in predefined range and also has been stable there.

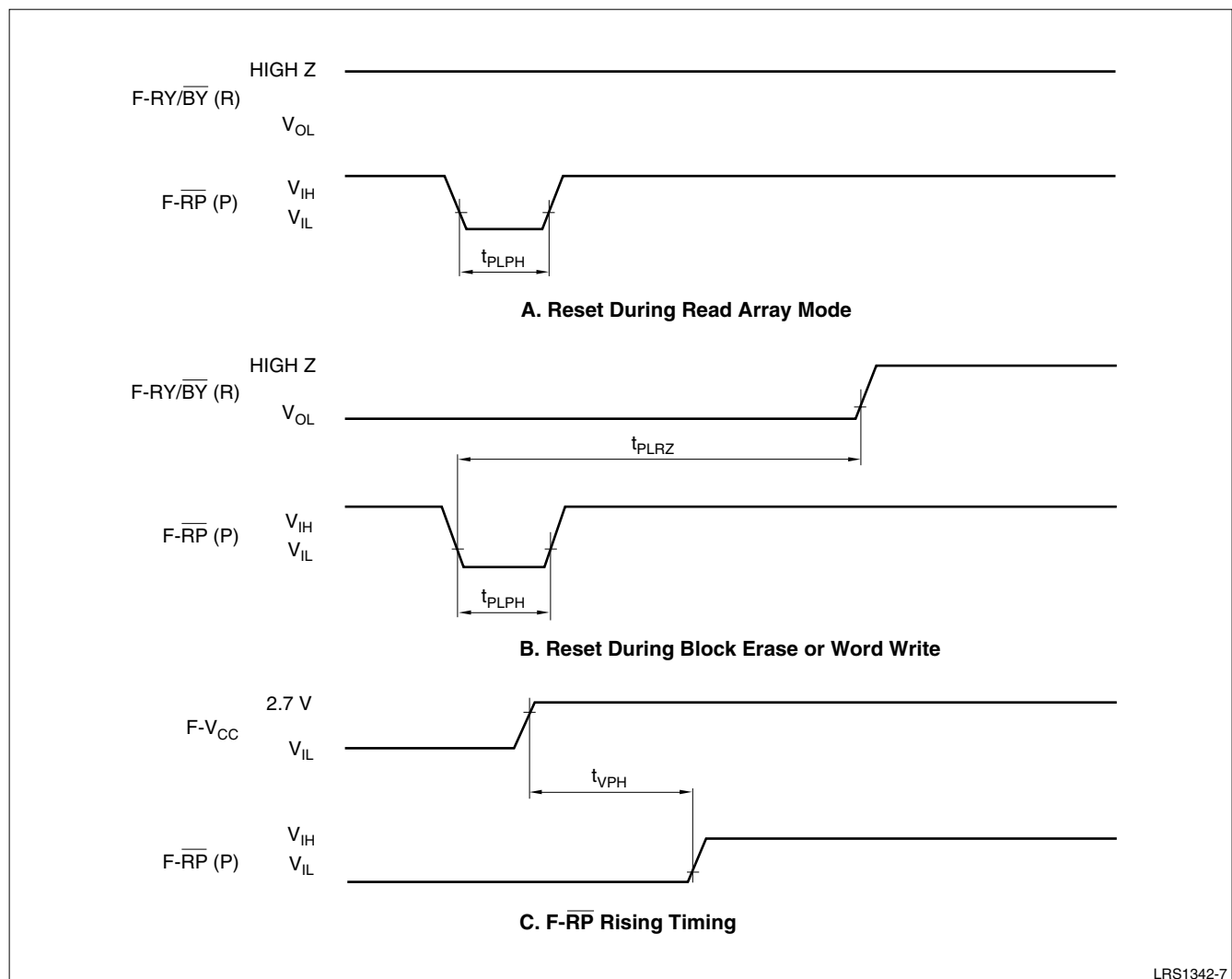


Figure 8. AC Waveform for Reset Operation

SRAM AC ELECTRICAL CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITION
Input Pulse Level	0.4 V to 2.7 V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Level	1.5 V
Output Load*	1TTL + C _L (30 pF)

NOTE: *Including scope and jig capacitance.

Read Cycle

T_A = -25°C to +85°C, V_{CC} = 2.7 V to 3.6 V

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read Cycle Time	t _{RC}	85		ns
Address Access Time	t _{AA}		85	ns
Chip Enable Access Time	S- $\overline{\text{CE}}_1$	t _{ACE1}	85	ns
	S-CE ₂	t _{ACE2}	85	ns
Byte Enable Access Time	t _{BE}		85	ns
Output Enable to Output Valid	t _{OE}		45	ns
Output hold from address change	t _{OH}	10		ns
S- $\overline{\text{CE}}_1$, S-CE ₂ LOW to Output Active*	S- $\overline{\text{CE}}_1$	t _{LZ1}	10	ns
	S-CE ₂	t _{LZ2}	10	ns
S- $\overline{\text{OE}}$ LOW to Output Active*	t _{OLZ}	10		ns
S- $\overline{\text{UB}}$ or S- $\overline{\text{LB}}$ LOW to Output in HIGH Impedance*	t _{BLZ}	10		ns
S- $\overline{\text{CE}}_1$, S-CE ₂ HIGH to Output in HIGH Impedance*	S- $\overline{\text{CE}}_1$	t _{HZ1}	0	25
	S-CE ₂	t _{HZ2}	0	25
S- $\overline{\text{OE}}$ HIGH to Output in HIGH Impedance*	t _{OHZ}	0	25	ns
S- $\overline{\text{UB}}$ or S- $\overline{\text{LB}}$ HIGH to Output in HIGH Impedance*	t _{BHZ}	0	25	ns

NOTE: *Active output to HIGH impedance and HIGH impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

Write Cycle

T_A = -25°C to +85°C, V_{CC} = 2.7 V to 3.6 V

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write Cycle Time	t _{WC}	85		ns
Chip Enable to End of Write	t _{CW}	75		ns
Address Valid to End of Write	t _{AW}	75		ns
Byte Enable to End of Write	t _{BW}	75		ns
Address Setup Time	t _{AS}	0		ns
Write Pulse Width	t _{WP}	65		ns
Write Recovery Time	t _{WR}	0		ns
Input Data Setup Time	t _{DW}	35		ns
Input Data Hold Time	t _{DH}	0		ns
S- $\overline{\text{WE}}$ HIGH to Output Active*	t _{OW}	5		ns
S- $\overline{\text{WE}}$ LOW to Output in HIGH Impedance*	t _{WZ}	0	25	ns

NOTE: *Active output to HIGH impedance and HIGH impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

SRAM AC CHARACTERISTICS TIMING DIAGRAMS

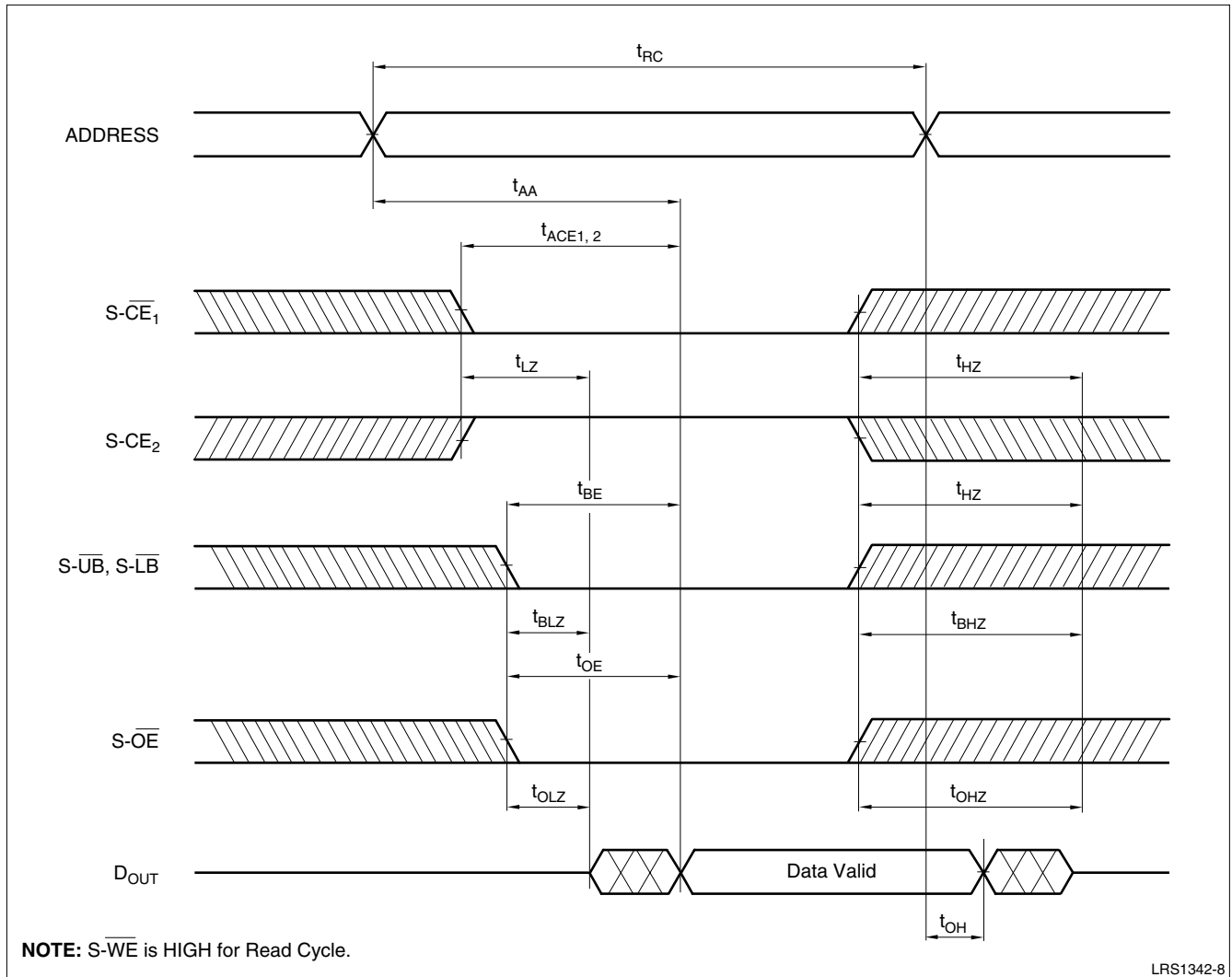
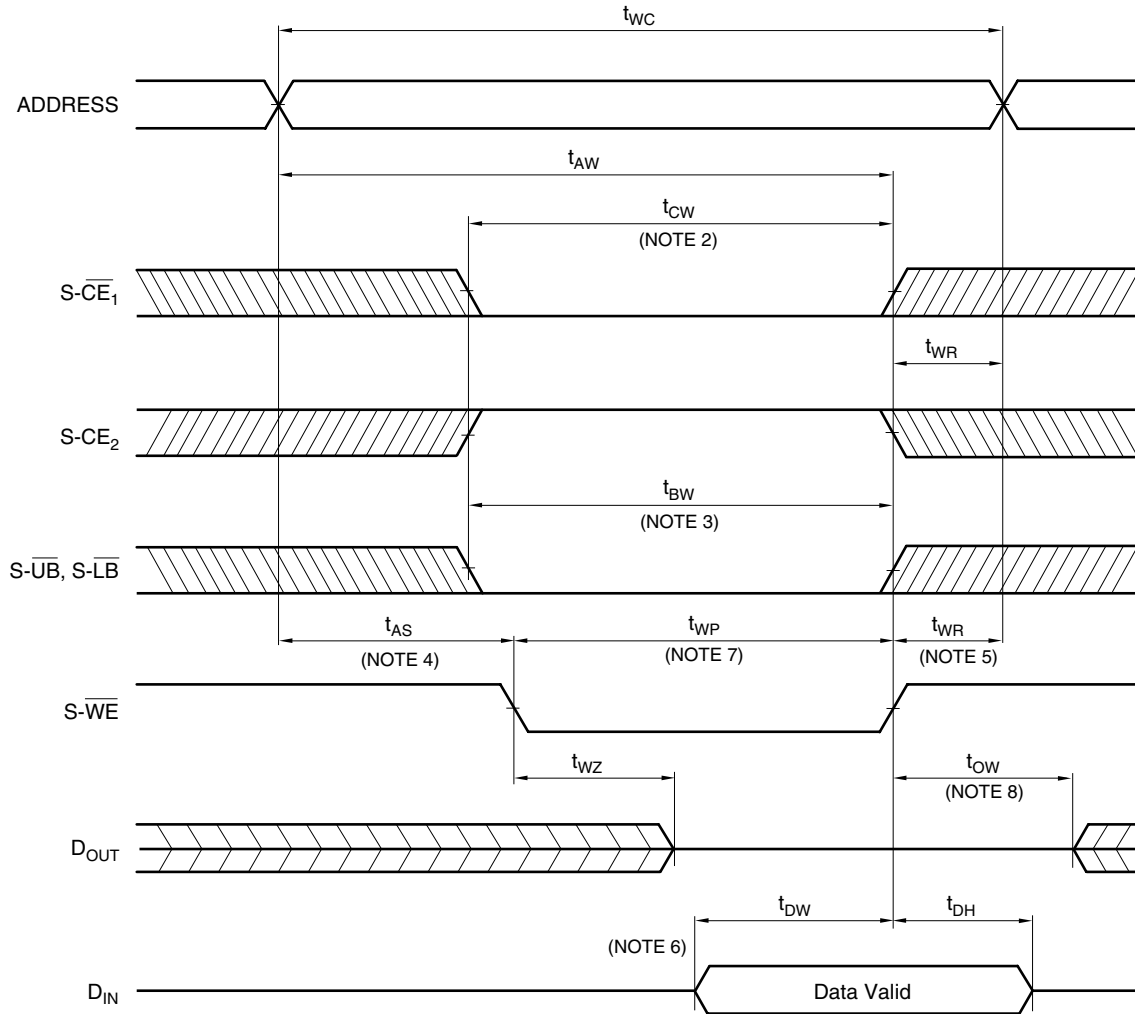


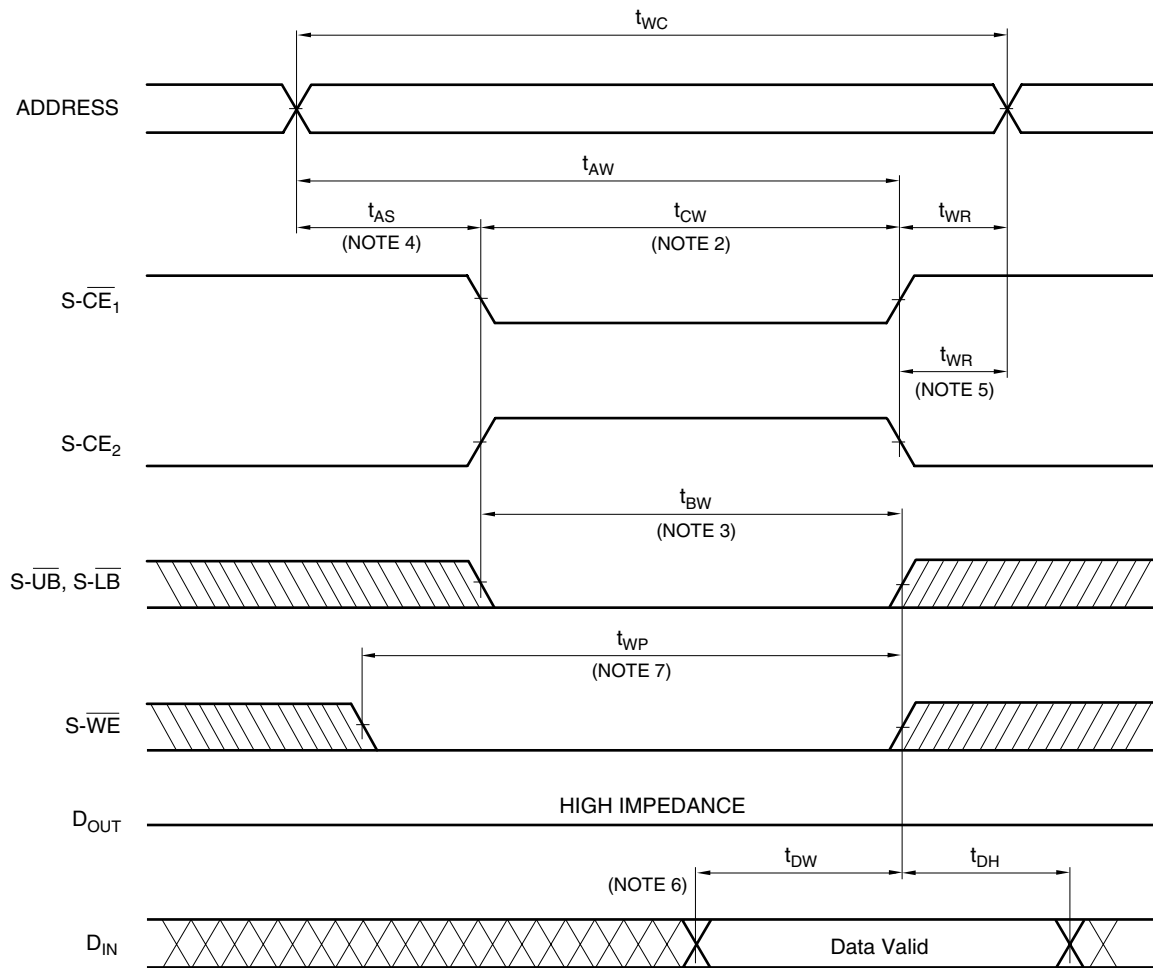
Figure 9. Read Cycle Timing Diagram

**NOTES:**

1. A write occurs during the overlap of a LOW S- \overline{CE}_1 , a HIGH S-CE₂ and a LOW S- \overline{WE} . A write begins at the latest transition among S- \overline{CE}_1 going LOW, S-CE₂ going HIGH and S- \overline{WE} going LOW. A write ends at the earliest transition among S- \overline{CE}_1 going HIGH, S-CE₂ going LOW and S- \overline{WE} going HIGH. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S- \overline{CE}_1 going LOW or S-CE₂ going HIGH to the end of write.
3. t_{BW} is measured from the time of going LOW S- \overline{UB} or LOW S- \overline{LB} to the end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change.
6. During this period, DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
7. If S- \overline{CE}_1 goes LOW or S-CE₂ goes HIGH simultaneously with S- \overline{WE} going LOW or after S- \overline{WE} going LOW, the outputs remain in HIGH impedance state.
8. If S- \overline{CE}_1 goes HIGH or S-CE₂ goes LOW simultaneously with S- \overline{WE} going HIGH or S- \overline{WE} going HIGH, the outputs remain in HIGH impedance state.

LRS1342-9

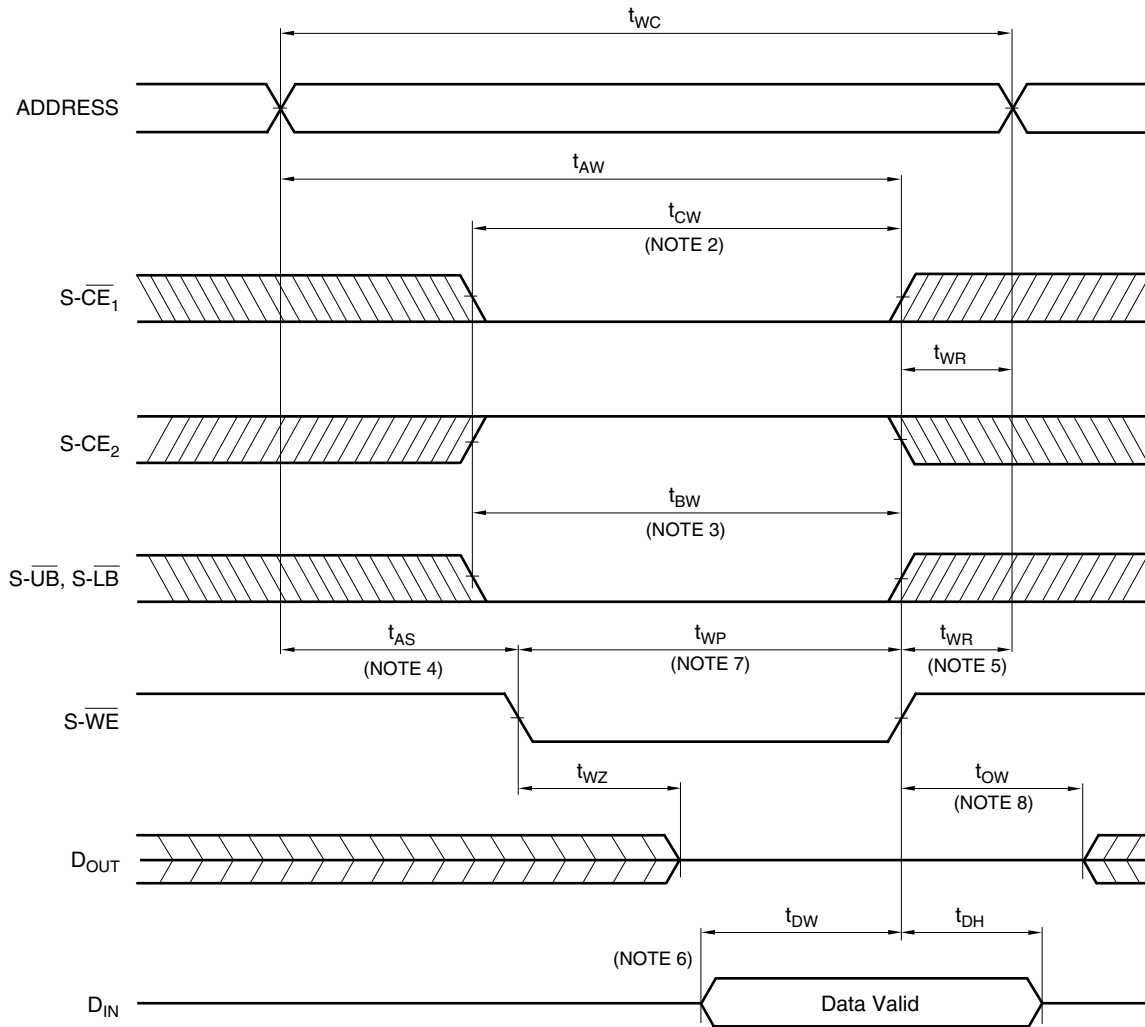
Figure 10. Write Cycle Timing Diagram (S- \overline{WE} Controlled)

**NOTES:**

1. A write occurs during the overlap of a LOW $\overline{S-CE_1}$, a HIGH $S-CE_2$ and a LOW $\overline{S-WE}$.
A write begins at the latest transition among $\overline{S-CE_1}$ going LOW, $S-CE_2$ going HIGH and $\overline{S-WE}$ going LOW. A write ends at the earliest transition among $\overline{S-CE_1}$ going HIGH, $S-CE_2$ going LOW and $\overline{S-WE}$ going HIGH. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{S-CE_1}$ going LOW or $S-CE_2$ going HIGH to the end of write.
3. t_{BW} is measured from the time of going LOW $\overline{S-UB}$ or LOW $\overline{S-LB}$ to the end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change.
6. During this period, DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
7. If $\overline{S-CE_1}$ goes LOW or $S-CE_2$ goes HIGH simultaneously with $\overline{S-WE}$ going LOW or after $\overline{S-WE}$ going LOW, the outputs remain in HIGH impedance state.

LRS1342-10

Figure 11. Write Cycle Timing Diagram ($\overline{S-CE}$ Controlled)

**NOTES:**

1. A write occurs during the overlap of a LOW S- \overline{CE}_1 , a HIGH S- CE_2 and a LOW S- \overline{WE} .
A write begins at the latest transition among S- \overline{CE}_1 going LOW, S- CE_2 going HIGH and S- \overline{WE} going LOW. A write ends at the earliest transition among S- \overline{CE}_1 going HIGH, S- CE_2 going LOW and S- \overline{WE} going HIGH. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S- \overline{CE}_1 going LOW or S- CE_2 going HIGH to the end of write.
3. t_{BW} is measured from the time of going LOW S- \overline{UB} or LOW S- \overline{LB} to the end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change.
6. During this period, DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
7. If S- \overline{CE}_1 goes LOW or S- CE_2 goes HIGH simultaneously with S- \overline{WE} going LOW or after S- \overline{WE} going LOW, the outputs remain in HIGH impedance state.
8. If S- \overline{CE}_1 goes HIGH or S- CE_2 goes LOW simultaneously with S- \overline{WE} going HIGH or S- \overline{WE} going HIGH, the outputs remain in HIGH impedance state.

LRS1342-11

Figure 12. Write Cycle Timing (S- \overline{UB} , S- \overline{LB} Controlled)

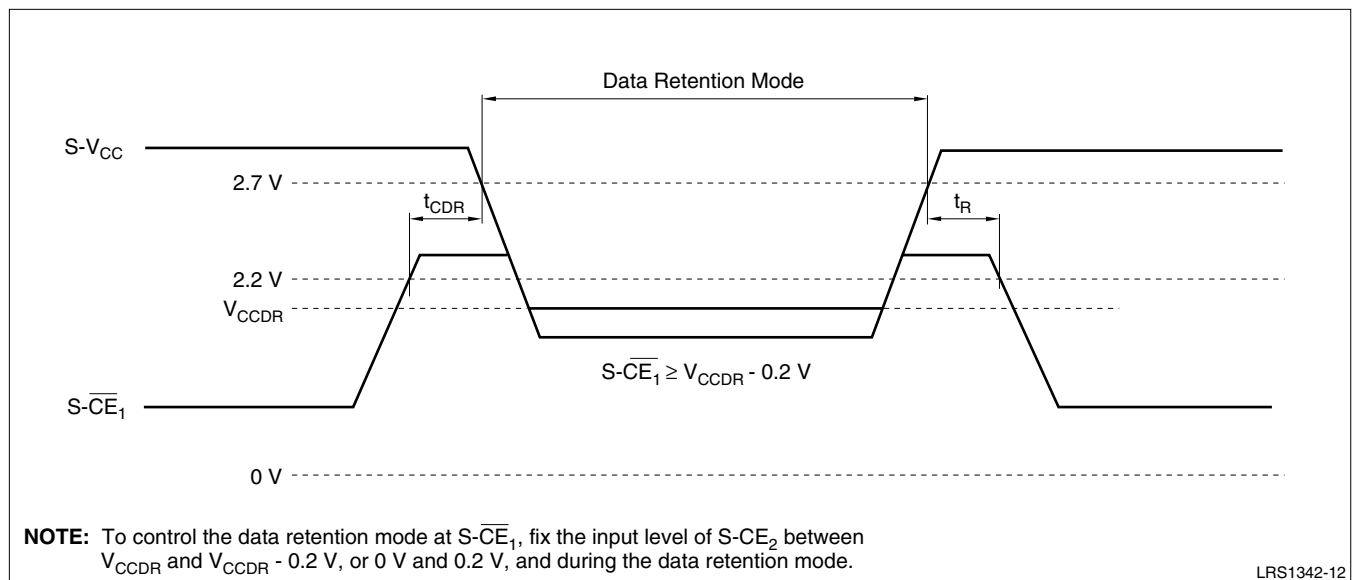
SRAM DATA RETENTION CHARACTERISTICS

 $T_A = -25^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

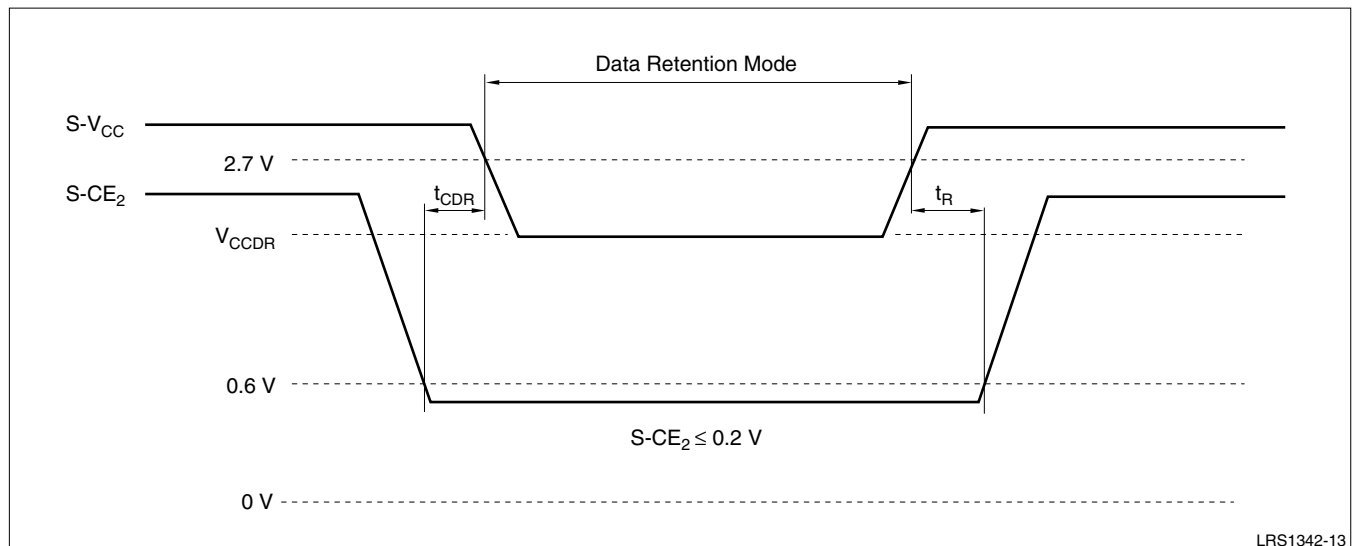
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP. ¹	MAX.	UNIT	NOTES
Data Retention Supply Voltage	V_{CCDR}	$S\text{-CE}_2 \leq 0.2\text{ V}$ or $S\text{-}\overline{\text{CE}}_1 \geq V_{\text{CCDR}} - 0.2\text{ V}$	2.0		3.6	V	2
Data Retention Supply Current	I_{CCDR}	$V_{\text{CCDR}} = 3\text{ V}$, $S\text{-CE}_2 \leq 0.2\text{ V}$ or $S\text{-}\overline{\text{CE}}_1 \geq V_{\text{CCDR}} - 0.2\text{ V}$			35	μA	2
Chip Enable Setup Time	t_{CDR}		0			ns	
Chip Enable Hold Time	t_{R}		5			ms	

NOTES:

- Reference value at $T_A = 25^{\circ}\text{C}$, $S\text{-}V_{\text{CC}} = 3.0\text{ V}$.
- $S\text{-}\overline{\text{CE}}_1 \geq V_{\text{CC}} - 0.2\text{ V}$, $S\text{-CE}_2 \geq V_{\text{CC}} - 0.2\text{ V}$ ($S\text{-}\overline{\text{CE}}_1$ controlled) or $S\text{-CE}_2 \leq 0.2\text{ V}$ ($S\text{-CE}_2$ controlled).



LRS1342-12

Figure 13. Data Retention Timing Diagram ($S\text{-}\overline{\text{CE}}_1$ Controlled)

LRS1342-13

Figure 14. Data Retention Timing Diagram ($S\text{-CE}_2$ Controlled)

GENERAL DESIGN GUIDELINES

Supply Power

Maximum difference (between $F-V_{CC}$ and $S-V_{CC}$) of the voltage is less than 0.3 V.

Power Supply and Chip Enable of Flash Memory and SRAM

$S-\overline{CE}_1$ should not be LOW and $S-CE_2$ should not be HIGH when $F-\overline{CE}$ is LOW simultaneously.

If the two memories are active together, they may not operate normally because of interference noises or data collision on DQ bus.

Both $F-V_{CC}$ and $S-V_{CC}$ need to be applied by the recommended supply voltage at the same time except SRAM data retention mode.

Power Up Sequence

When turning on Flash memory power supply, keep $F-\overline{RP}$ LOW. After $F-V_{CC}$ reaches over 2.7 V, keep $F-\overline{RP}$ LOW for more than 100 ns.

Device Decoupling

The power supply needs to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals ($F-\overline{CE}$, $S-\overline{CE}_1$, $S-CE_2$).

FLASH MEMORY DATA PROTECTION

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems.

Such noises, when induced onto $F-\overline{WE}$ signal or power supply may be interpreted as false commands, causing undesired memory updating.

To protect the data stored in the flash memory against unwanted overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

Protecting Data in Specific Block

By setting a $F-\overline{WP}$ to LOW, only the boot block can be protected against overwriting. Parameter and main blocks cannot be locked. System program, etc., can be locked by storing them in the boot block. When a high voltage is applied to $F-\overline{RP}$, overwrite operation is enabled for all blocks.

For further information on setting/resetting of block bit, and controlling of $F-\overline{WP}$ and $F-\overline{RP}$, refer to the 'Command Definitions' section.

Data Protection Through $F-V_{PP}$

When the level of $F-V_{PP}$ is lower than $F-V_{PPLK}$ (lock-out voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected.

For the lockout voltage refer to the 'DC Characteristics' section.

Data Protection During Voltage Transition

DATA PROTECTION THROUGH $F-\overline{RP}$

When the $F-\overline{RP}$ is kept LOW during power up and power down sequence, write operation on the flash memory is disabled, write protecting all blocks.

For details of $F-\overline{RP}$ control refer to the 'Flash Memory AC Electrical Characteristics' section.

DESIGN CONSIDERATIONS

Power Supply Decoupling

To avoid a bad effect on the system by flash memory power switching characteristics, each device should have a 0.1 μ F ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. LOW inductance capacitors should be placed as close as possible to package leads.

V_{PP} Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} Power Supply trace. Use similar trace widths and layout considerations given to the V_{CC} power bus.

The Inhibition of Overwrite Operation

Please do not execute reprogramming '0' for the bit which has already been programmed '0'. Overwrite operation may generate unerasable bit. In case of reprogramming '0' to the data which has been programmed '1'.

- Program '0' for the bit in which you want to change data from '1' to '0'.
- Program '1' for the bit which has already been programmed '0'.

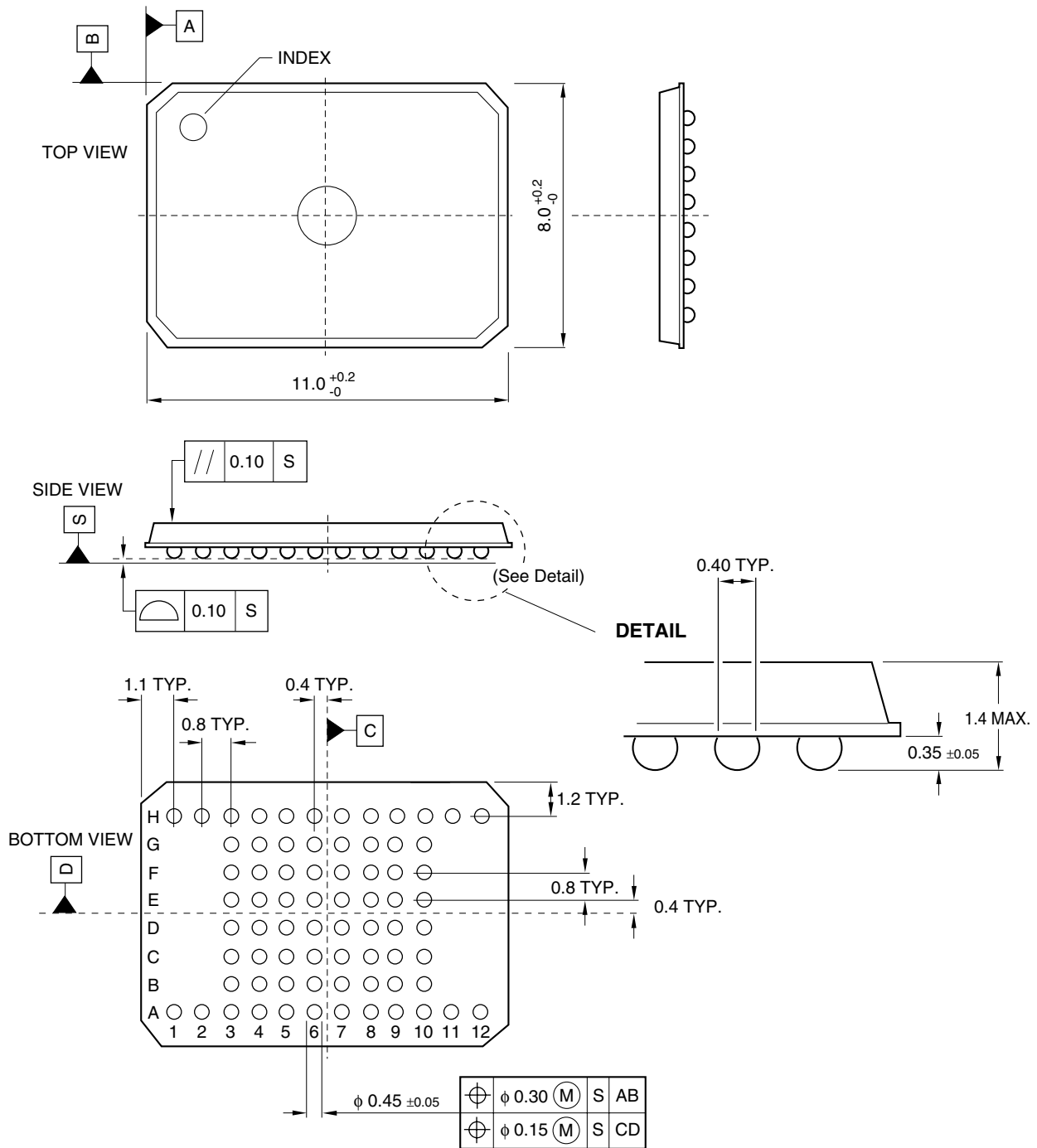
For example, changing data from '101110110111101' to '1010110110111100' requires '111011111111110' programming.

Power Supply

Block erase, full chip erase, word write and lock-bit configuration with an invalid V_{PP} (see 'DC Characteristics') produce spurious results and should not be attempted. Device operations at invalid V_{CC} voltage produce spurious results and should be attempted.

OUTLINE DIMENSIONS

FBGA072-P-0811



NOTE: Dimensions are in mm.

72FBGA

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SHARP components should not be used in medical devices with life support functions or in safety equipment (or similar applications where component failure would result in loss of life or physical harm) without the written approval of an officer of the SHARP Corporation.

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SHARP[®]**NORTH AMERICA**

SHARP Microelectronics
of the Americas
5700 NW Pacific Rim Blvd.
Camas, WA 98607, U.S.A.
Phone: (360) 834-2500
Telex: 49608472 (SHARPCAM)
Facsimile: (360) 834-8903
<http://www.sharpsma.com>

EUROPE

SHARP Electronics (Europe) GmbH
Microelectronics Division
Sonninstraße 3
20097 Hamburg, Germany
Phone: (49) 40 2376-2286
Facsimile: (49) 40 2376-2232
<http://www.sharpmed.com>

ASIA

SHARP Corporation
Integrated Circuits Group
2613-1 Ichinomoto-Cho
Tenri-City, Nara, 632, Japan
Phone: +81-743-65-1321
Facsimile: +81-743-65-1532
<http://www.sharp.co.jp>