M62281P/FP

GENERAL PURPOSE CURRENT MODE PWM CONTROL IC

DESCRIPTION

M62281P/FP is designed as a high speed current mode PWM control IC.

This small10 pin package contains many functions and protection circuits allowing simpler peripheral circuit and compact set design.

This IC can operate high speed switching (700kHz max.) with high speed current sense comparator and current limiting circuit.

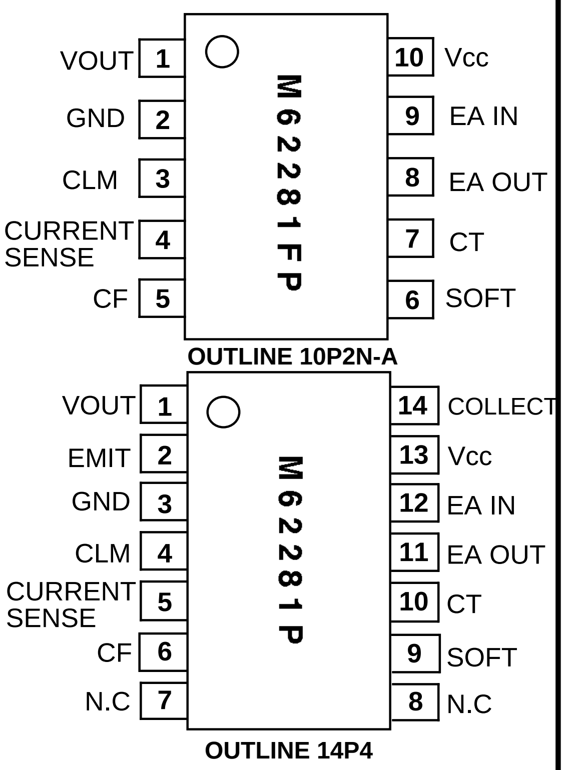
FEATURES

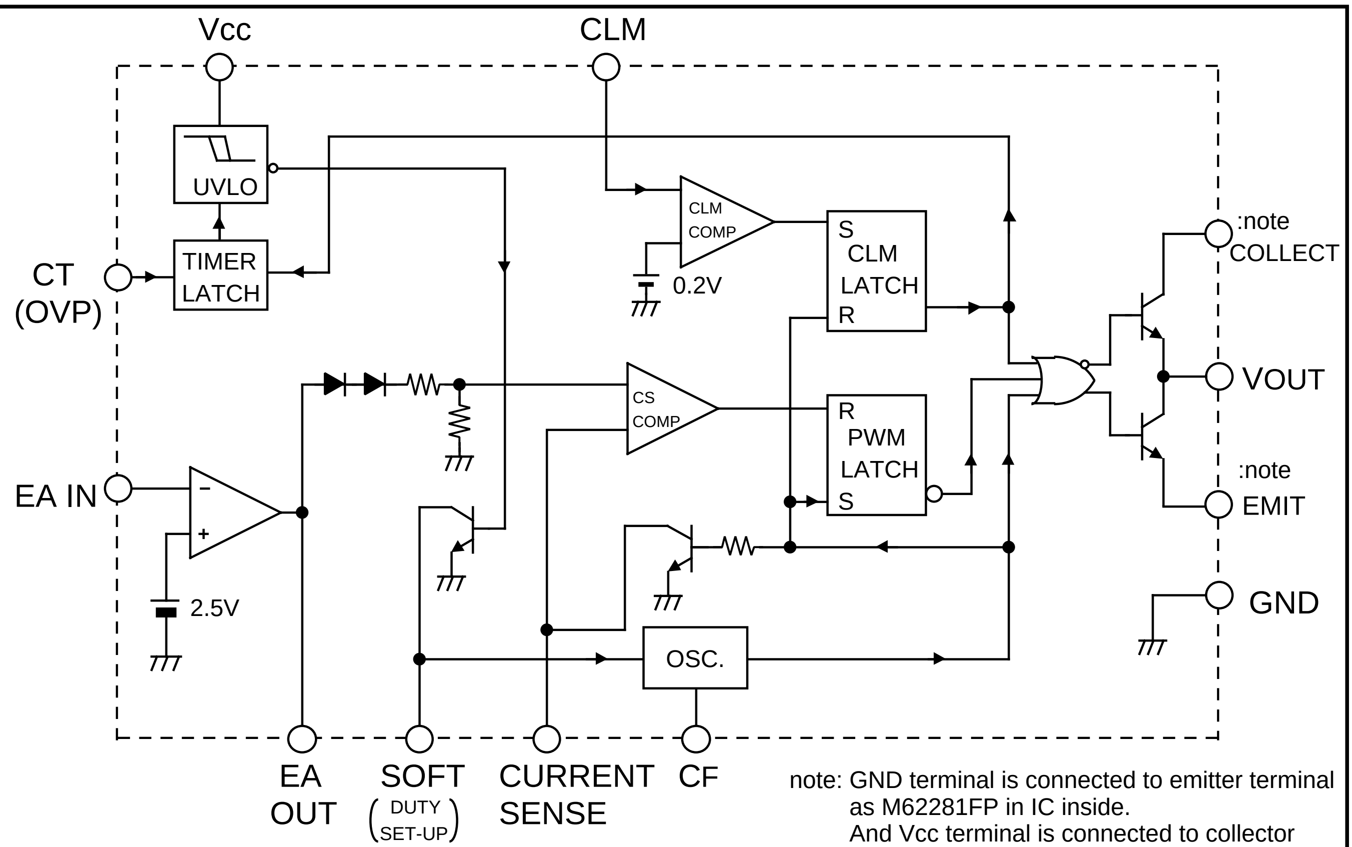
- 700kHz applicable to MOS-FET
  - Output current Io(peak) = ±1A
  - Totem pole output
- CURRENT SENSE terminal separate form CLM terminal makes SMPS strong in noise.
- High speed pulse-by-pulse current limiting
- Timer type latch protection circuit with OVP(external reset is possible)
- Soft start operation is possible (with dead time control)
- Built-in OPAmp for feedback control (photo coupler can be driven)
- Small start-up current 180µA
- Start-up voltage 12.5V, Stop voltage 8.3V

APPLICATION

- Switching Regulator
- DC-DC converter

PIN CONFIGURATION (TOP VIEW)





note: GND terminal is connected to emitter terminal as M62281FP in IC inside.
And Vcc terminal is connected to collector terminal as M62281FP in IC inside.

ABSOLUTE MAXIMUM RATINGS (Ta=25˚C, unless otherwise noted)

Symbol	Parameter	Condition		Rating	Unit
V_{CC}	Supply voltage			36	V
I_{OUT}	Output current		Continuous	150	mA
			Peak	1.0	A
V_{CT}	CT terminal Supply voltage			36	V
$V_{EA\ IN}$	EA IN terminal Supply voltage			10	V
V_{CLM}	CLM terminal Supply voltage			- 0.3 ~ + 4.0	V
V_{CS}	CURENT SENSE terminal Supply voltage			- 0.3 ~ + 5.8	V
Pd	Power dissipation		P	1500	mW
			FP	440	mW
K_{theta}	Thermal derating	Ta≥25˚C	P	12	mW/˚C
			FP	3.52	mW/˚C
Topr	Operating temperature			- 20 ~ + 85	˚C
Tstg	Storage temperature			- 40 ~ + 150	˚C

ELECTRICAL CHARACTERISTICS (Ta=25˚C, Vcc=14V, unless otherwise noted)

Block	Symbol	Parameter	Test condition	Limits Min	Limits Typ	Limits Max	Unit
All device	V_{CC}	Supply voltage range		$V_{CC(STOP)}$	——	35	V
	$V_{CC(START)}$	Operation start-up voltage		11.5	12.5	13.5	V
	$V_{CC(STOP)}$	Operation stop voltage		7.6	8.3	9.0	V
	ΔV_{CC}	Start-up and stop voltage difference		3.5	4.2	5.1	V
	I_{CCL}	Stand-by current	$V_{CC}=V_{CC(START)}$ - 0.5V	90	180	270	µA
	I_{CCO}	Operating current		7.5	13	19	mA
	I_{CCOFF}	Timer latch circuit current	Vcc=14V	0.9	2.0	3.0	mA
			$V_{CC}=V_{CC(STOP)}$ + 0.2V	0.8	1.8	2.7	mA
CT	V_{THCTH}	CT term."H" threshold voltage		3.5	4.0	4.5	V
	V_{THCTL}	CT term."L" threshold voltage		0.4	0.7	1.0	V
	$I_{TIMEOFFIN}$	CT term. input current (timer off mode)		70	115	165	µA
	$I_{TIMEOFFOUT}$	CT term. output current (timer on mode)		-33	-14	-5	µA
Error Amp	V_B	Reference voltage		2.4	2.5	2.6	V
	I_B	Input bias current		-300	-100	0	nA
	A_{VO}	Open loop gain			70		dB
	f_T	Unity gain bandwidth			1		MHz
	I_{OS}	Output source current		-460	-370	-240	µA
	V_{Om+}	Output voltage (High)		5.3	5.8	6.25	V
	V_{Om-}	Output voltage (Low)		0	0.2	0.35	V
CURRENT SENSE	A_{VCS}	CS term. input voltage gain			3.0		V/V
	I_B	Input bias burrent		-5	-1		µA
	T_{PDCS}	CS term. delay time	Delay time to output		150		nS

ELECTRICAL CHARACTERISTICS (Ta=25˚C, Vcc=14V, unless otherwise noted)

Block	Symbol	Parameter	Test condition	Limits			Unit
				Min	Typ	Max	
CLM	VTHCLM	CLM term. threshold voltage		180	200	220	mV
	IOUTCLM	CLM term. output current	VCLM=0V	-270	-200	-140	µA
	TPDCLM	CLM term. delay time	Delay time to output		100		nS
SOFT	VSOFT(0%)	Soft term. input voltage range to set 0% duty	Soft term. input voltage range to set 0% duty	0		1.0	V
	VSOFT(50%)	Soft term. voltage when 50% duty			2.7		V
	Duty Max	Maximum duty		83	90	97	%
	ISOFT	Soft term. input current		-50	-43	-36	
OSC.	foscmax	Maximum oscillation frequency				700	KHz
	fosc	Oscillation frequency	CF= 270pF	130	180	230	KHz
	VOSCH	Oscillation upper limit voltage	CF= 270pF	3.2	3.6	4.0	V
	VOSCL	Oscillation lower limit voltage	CF= 270pF	1.2	1.4	1.6	V
	ΔVOSC	Oscillation voltage	CF= 270pF	1.9	2.2	2.5	V
OUTPUT	VOL1	Output low voltage	Vcc=14V, Io=10mA		0.04	0.4	V
	VOL2		Vcc=14V, Io=100mA		0.3	1.4	V
	VOH1	Output high voltage	Vcc=14V, Io=-10mA	12.0	12.7		V
	VOH2		Vcc=14V, Io=-100mA	11.5	12.5		V
	TRISE	Output voltage rise time	No load		50		nS
	TFALL	Output voltage fall time	No load		35		nS

FUNCTION DESCRIPTION AND APPLICATION

(1) EA IN, EA OUT TERMINAL

Circuit for EAOUT terminal is connected to constant current load(370µA typ.) shown in Fig.1. Output voltage of error amp. is controlled by the output transistor to provide current-sense comp. with the controlled voltage.

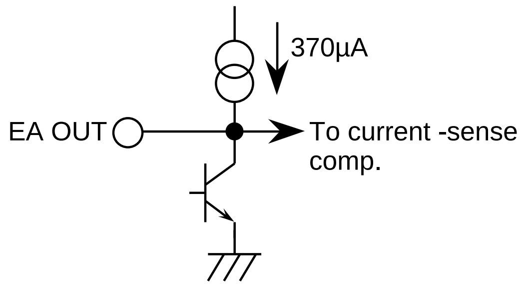


Fig.1 Circuit diagram of EAOUT terminal

Peripheral circuit of Error Amp

Detected voltage devided by R1 and R2 is input to EAIN terminal in such case as fly-back system where VCC line voltage is proportional to output voltage, or in the case that the voltage detection is made on the primary side. In this case operating region is set by R1 and R2, and AC gain by R1// R2, RF.

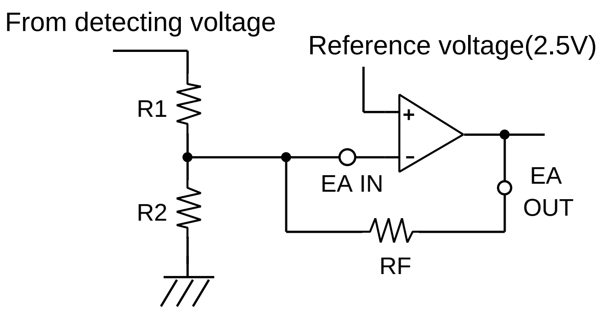


Fig.2 Method to detect the voltage on the primary side

In the case that feedforward system by photo-coupler is applied, following two methods are available.
One is the method by error amp. as in Fig.3-1, the other is by the direct connection to photo-coupler as in Fig.3-2.
When photo-coupler is directly connected to EAOUT terminal, input terminal of error amp. is connected to GND, photo-coupler is connected directly to EAOUT terminal.

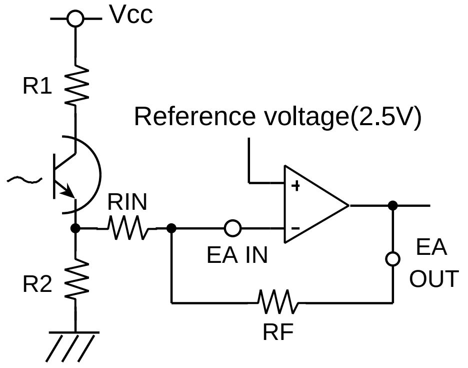


Fig.3-1 Method to use photo-coupler (1)

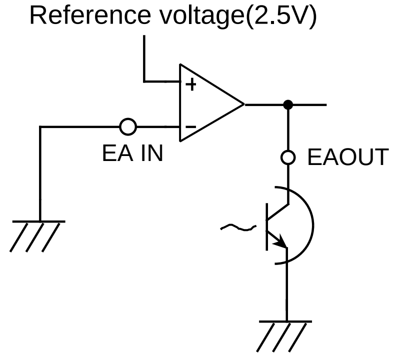


Fig.3-2 Method to use photo-coupler (2)

In Fig. 3-1, AC gain is represented as:

$$| Av | = | RF/ RIN |$$

Proper gain setting is about 40dB.
RF should be 52KΩ or more due to the current source capability of error amp.
R1, R2 should meet the condition as below so that the voltage of EAIN terminal should not be over 5V.

$$R2 * Vcc/ (R1 + R2) \leq 5V$$

Due to the input impedance of EAIN terminal, the current in R1, R2 should be less than several mA.

(2) CT(OVP) TERMINAL

Timer type latch circuit works as follows.
Constant charge current flows out from CT terminal to the external capacitor when CLM is operative.
When the voltage of CT terminal rises up to over 4.0V(typ.), the latch circuit operates to make functions of this IC inoperative. Inoperative status is sustained until supply voltage becomes less than stop voltage. The value for start-up register has to be set so that the current over 1.8mA(typ.) can flow the resistor because the stop status has to be kept by the current in start-up resistor R1 shown in application circuit.
When timer latch circuit is operative, supply current increases at high voltage as shown in Fig.4 to avoid the damage caused by unnecessarily increased supply voltage.
Inoperative status goes back to operation by forcibly decreasing the voltage of CT terminal to less than 0.7V.

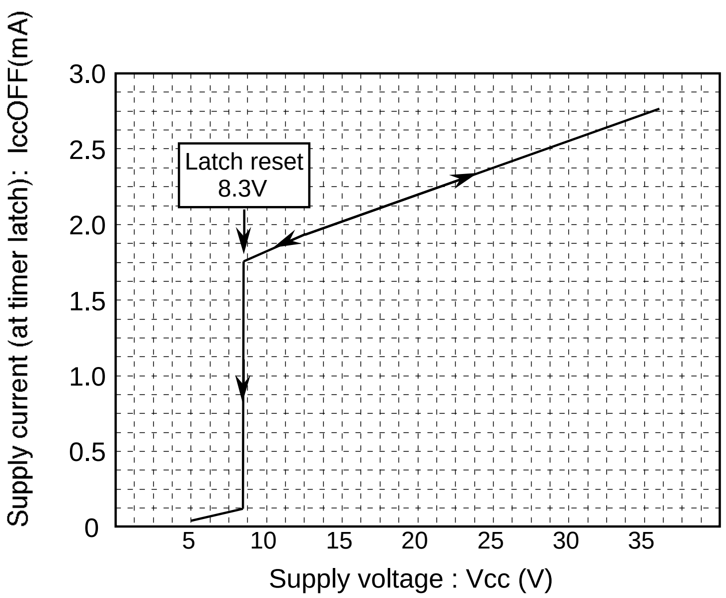


Fig.4 Supply current/voltage chracteristics (at timer latch)

Even if the timer function is not needed, latch function operates, that is, IC becomes inoperative when the voltage of CT terminal is forced to be high voltage. Therefore, CT terminal can also be used for OVP(over voltage protection).
When only OVP function is needed(timer latch function is not necessary), connect the resistor between CT terminal and GND. In this case, the above mentioned charge current cannot make the voltage of CT terminal rise up to "H" threshold, thus latch function does not operate. (Refer to Fig.5-1, 5-2)

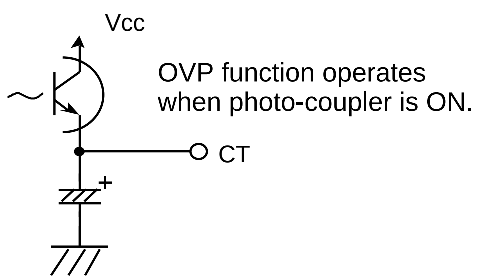


Fig.5-1 Method to use timer type latch and OVP

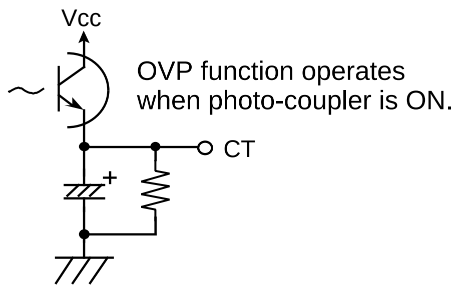


Fig.5-2 Method to use only OVP

(3) SOFT(DUTY SET-UP) TERMINAL

The voltage of SOFT terminal determines the maximum duty.
Maximum duty can be set by connecting the resistor as in Fig.6 because the constant current compensated for temperature flows out of this terminal.
And by connecting the capacitor between the terminal and GND, soft start function operates. That is, we can get the gradual increase of maximum duty at start-up.
Maximum duty is represented as:

$$\text{Duty(max.)} \approx (42 * \text{VSOFT}) - 59\ (\%)$$

,where VSOFT=ISOFT * RSOFT (V), ISOFT=43µA(typ.)

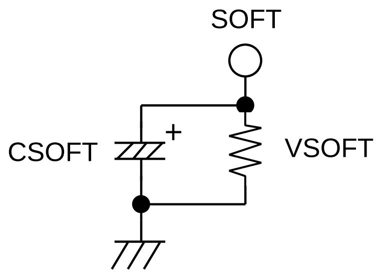


Fig.6
Method to set up duty
and SOFT start function.

If the voltage of SOFT terminal is higher than 3.53V(typ.)(upper limit voltage of the oscillation waveform), maximum duty is internally decided to be 90%.
Soft start time (TSOFT) is represented as:

$$\text{TSOFT} \approx \text{CSOFT} * 31 * 10^{3}\ \text{(sec)}$$

TSOFT means the time from start-up until the voltage of SOFT terminal goes up to higher than 1.4V(typ.) (lower limit voltage of the oscillation waveform).
Discharging circuit operative before start-up at Vcc is internally equipped so that the soft start never fail to operate at the restart of voltage supply.

(4) CLM TERMINAL

This terminal is for pulse-by-pulse current limiting.
Current limiting circuit is almost the same as that of M51995.
CLM terminal is separate from CURRENT SENSE terminal allowing the noise filter to be optimized and the high-speed over current protection.
The voltage detected by the current detecting resistor can be directly input as shown in Fig.7-1, if the detected voltage is about the threshold voltage(200mV(typ.)), but if the voltage is larger than the threshold, the voltage has to be input divided by resistors as shown in Fig.7-2.

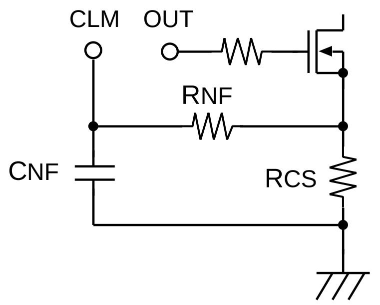


Fig.7-1 peripheral circuit of CLM

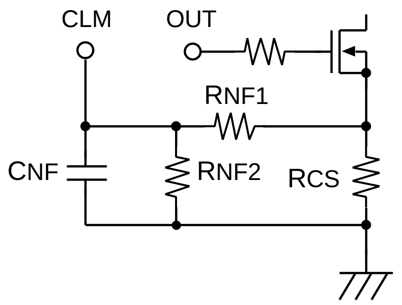


Fig. 7-2 peripheral circuit of CLM when the detected voltage is high.

1000pF to 22000pF is recommended for CNF. Be sure to use 100Ω or less for RNF and RNF1// RNF2 (*)so that the detection sensitivity is not influenced by the current flown out from CLM terminal.
Non-inductive resistor is recommended for current detecting resistor.
* RNF1//RNF2 = (RNF1 * RNF2)/(RNF1 + RNF2)

(5) CURRENT SENSE TERMINAL

The voltage proportional to the switching current is supplied to this terminal.
Output duty is controlled by comparing this voltage with the output of error amp..
CLM and CURRENT SENSE terminal is separate from each other, so various settings are available depending upon the application.

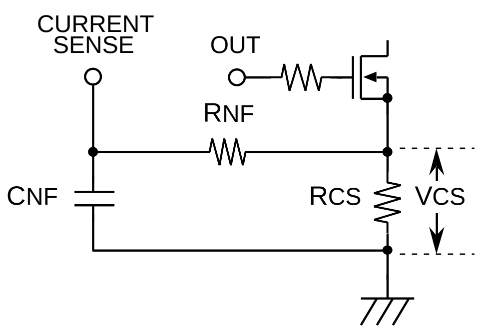


Fig.8 peripheral circuit of CURRENT SENSE

RCS is determined by:
VCS = (VEAOUT - 1.3)/3 (V), where VEAOUT represents the voltage of EAOUT terminal.

(6) CF TERMINAL

Oscillation frequency is set by capacitor connected to CF terminal.
The waveform of CF terminal is triangular one with the ratio of 9:1 for charge-discharge period.
Oscillation frequency is represented as:

$$f_{OSC} = \frac{1}{(19.4 * 10^{3} * C_{OSC}) + (0.4 * 10^{-6})} \quad (Hz)$$

(7) Attention for heat generation

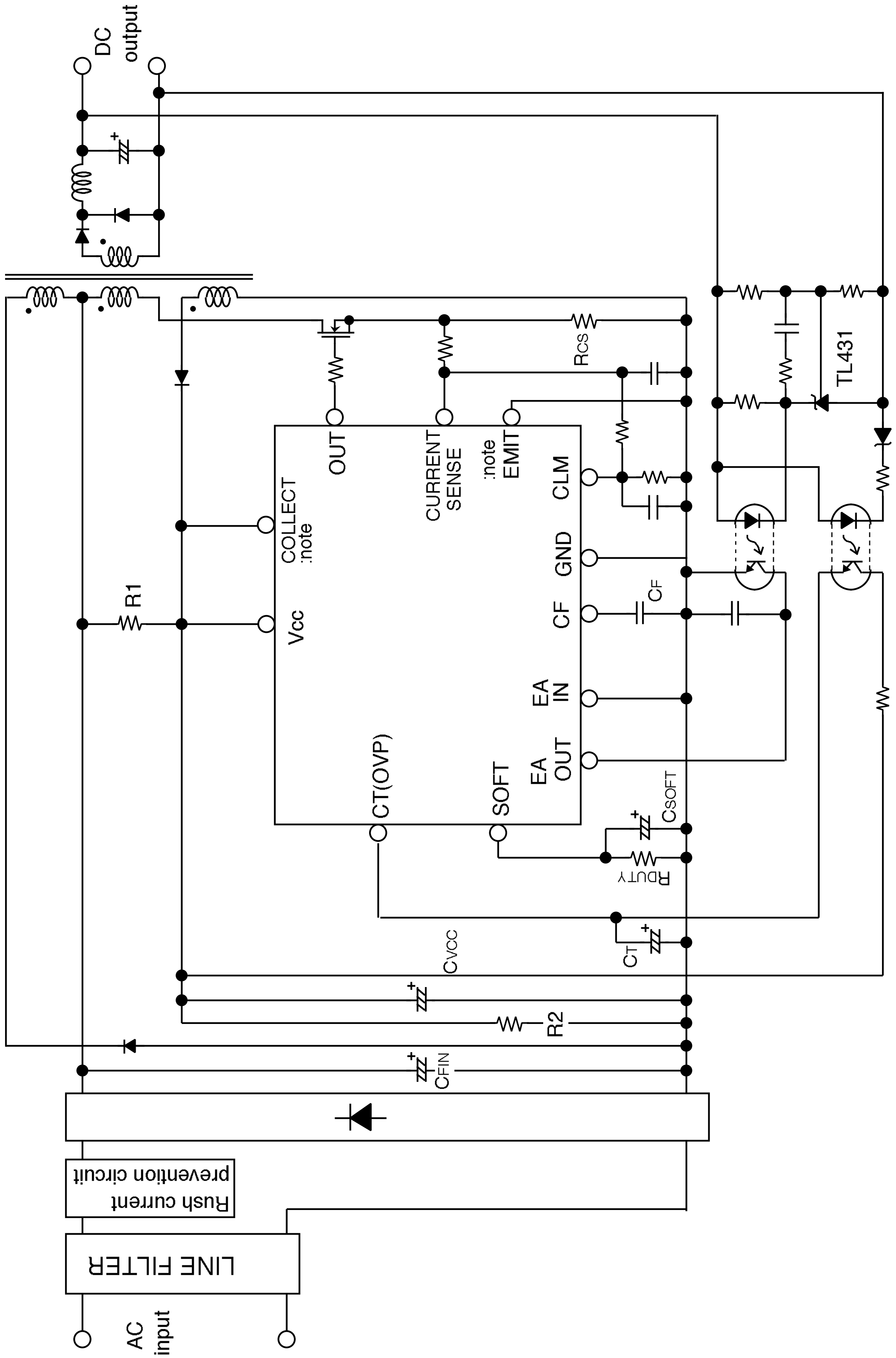
Although the absolute maximum rating of ambient temperature is spelled out as 85˚C, it is always annoying to specify the location this temperature refers to because the power dissipation generated locally in switching regulator is fairly large and the temperature in the vicinity of the IC varies from place to place.

One of the recommendable ways to solve this problem is to check the teperature on the surface of the IC.

The difference in temperature between IC junction and the surface of IC package is 30˚C or less when IC junction temperature is measured by utilizing the temperature characteristics of p-n junction forward voltage, and the surface temperature by "thermo-viewer" on the condition that the IC is mounted on the "phenol-base" PC board in normal atomosphere.

This concludes that maximum case temperature (surface temperature of IC package) rating is 100˚C with adequate margin considering the absolute maximum rating of junction temperature is 150˚C.

M62281 APPLICATION CIRCUIT (FEED-FORWARD)



:note GND terminal is connected to emitter terminal as M62281FP in IC inside.
And Vcc terminal is connected to collector terminal as M62281FP in IC inside.