



# STT2PF60L

## P-CHANNEL 60V - 0.20 $\Omega$ - 2A SOT23-6L STripFET™ II POWER MOSFET

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STT2PF60L	60 V	<0.25 $\Omega$	2 A

- TYPICAL R<sub>DS(on)</sub> = 0.20  $\Omega$
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

### DESCRIPTION

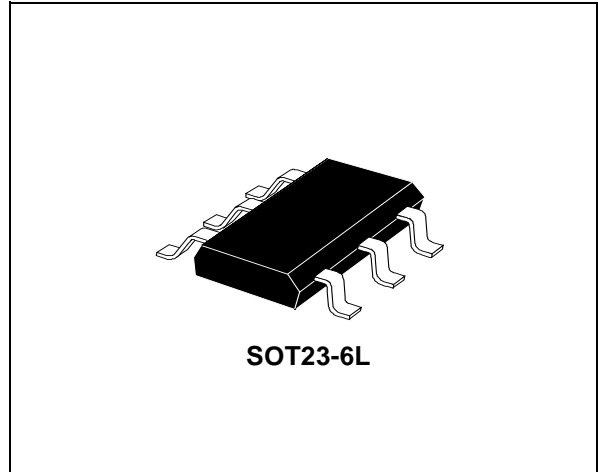
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### APPLICATIONS

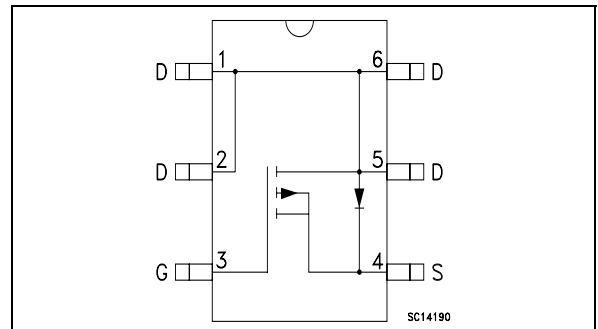
- DC MOTOR DRIVE
- DC-DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN PORTABLE/DESKTOP PCs
- CELLULAR

### MARKING

- STP6



### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	60	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	60	V
V <sub>GS</sub>	Gate- source Voltage	$\pm 15$	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	2	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	1.3	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	8	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	1.6	W

(●) Pulse width limited by safe operating area.

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

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## THERMAL DATA

Rthj-amb	(*)Thermal Resistance Junction-ambient	Max	78	°C/W
Rthj-amb	(**)Thermal Resistance Junction-ambient	Max	156	°C/W
T <sub>j</sub>	Max. Operating Junction Temperature		150	°C
T <sub>stg</sub>	Storage Temperature		-55 to 150	°C

(\*) Mounted on a 1 in<sup>2</sup> pad of 2 oz Cu in FR-4 board

(\*\*) Mounted on a minimum pad of 2 oz Cu in FR-4 board

## ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C unless otherwise specified)

### OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>C</sub> = 125°C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 15 V			±100	nA

### ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	1			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 1 A V <sub>GS</sub> = 4.5 V I <sub>D</sub> = 1 A		0.20 0.24	0.25 0.30	Ω Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> = 10 V I <sub>D</sub> = 1 A		3		S
C <sub>iSS</sub> C <sub>oSS</sub> C <sub>rSS</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 25V f = 1 MHz, V <sub>GS</sub> = 0		313 67 25		pF pF pF

**ELECTRICAL CHARACTERISTICS** (continued)

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 30\text{ V}$ $I_D = 1\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 1)		44 34		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 30\text{ V}$ $I_D = 2\text{ A}$ $V_{GS} = 5\text{ V}$ (see test circuit, Figure 2)		5 0.5 2.2	7	nC nC nC

## SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 30\text{ V}$ $I_D = 1\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 1)		42 15		ns ns

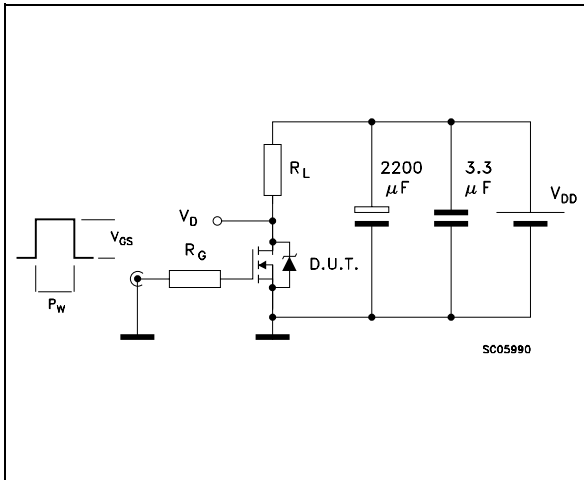
## SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				2 8	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 2\text{ A}$ $V_{GS} = 0$			1.2	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 2\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 3)		38 47.5 2.5		ns nC A

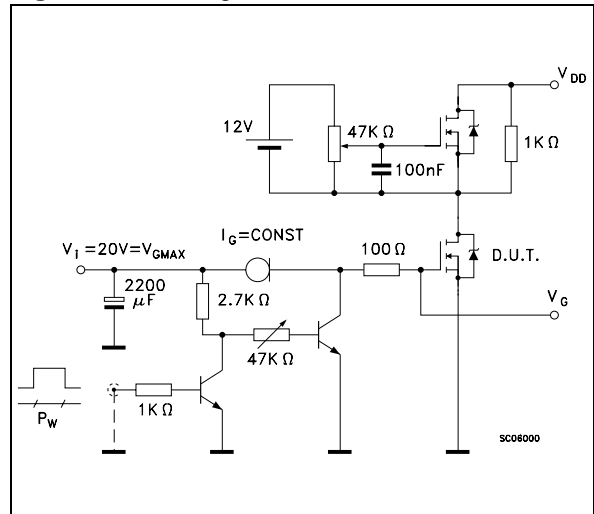
(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

(\bullet) Pulse width limited by safe operating area.

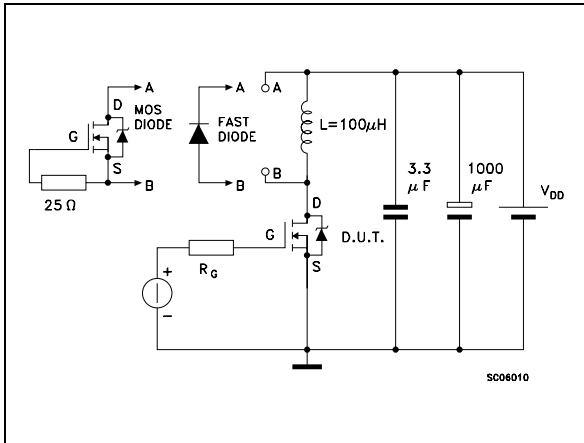
**Fig. 1: Switching Times Test Circuits For Resistive Load**



**Fig. 2: Gate Charge test Circuit**

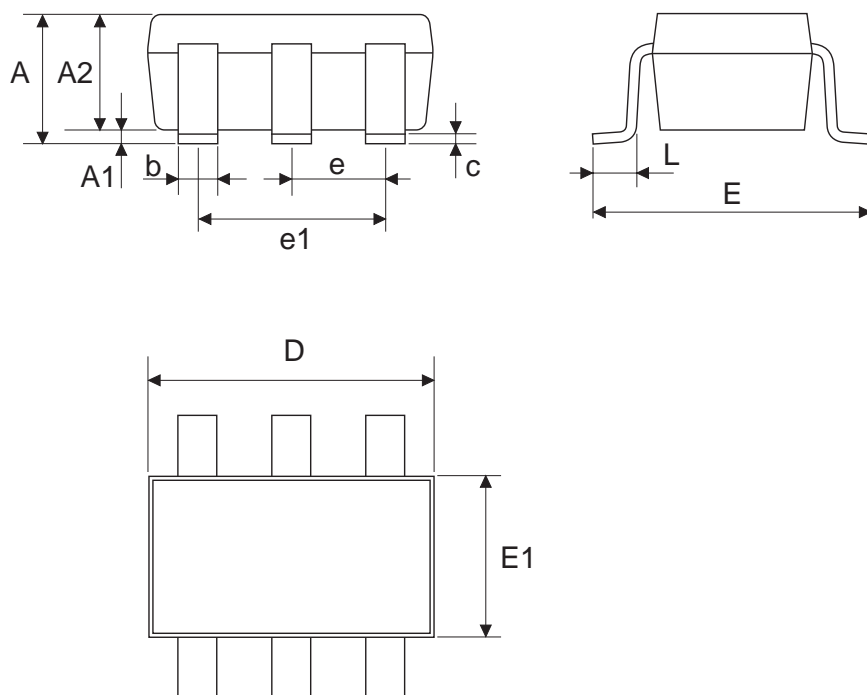


**Fig. 3: Test Circuit For Diode Recovery Behaviour**



## SOT23-6L MECHANICAL DATA

DIM.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	0.035		0.057
A1	0.00		0.15	0.000		0.006
A2	0.90		1.30	0.035		0.051
b	0.25		0.50	0.010		0.020
C	0.09		0.20	0.004		0.008
D	2.80		3.10	0.110		0.122
E	2.60		3.00	0.102		0.118
E1	1.50		1.75	0.059		0.069
L	0.35		0.55	0.014		0.022
e		0.95			0.037	
e1		1.90			0.075	



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