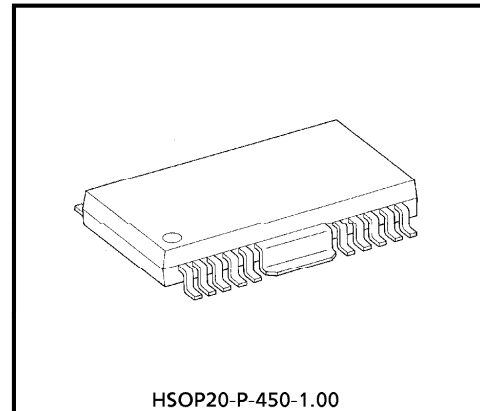


TD6336F

8-BIT SERIAL-IN PARALLEL-OUT DRIVER

The TD6336F is an automotive 8-bit SI/PO driver IC using a Bi-CMOS process characterized by high output withstand voltage.

The shift registers share a common clock and a common reset signal. Data is shifted on the leading edge of the clock. The IC also has $\overline{\text{LATCH}}$ and $\overline{\text{ENABLE}}$ inputs. Its output is an N-channel open-drain output, and I_{sink} is up to 100mA. When the supply voltage becomes low, the output turns off.

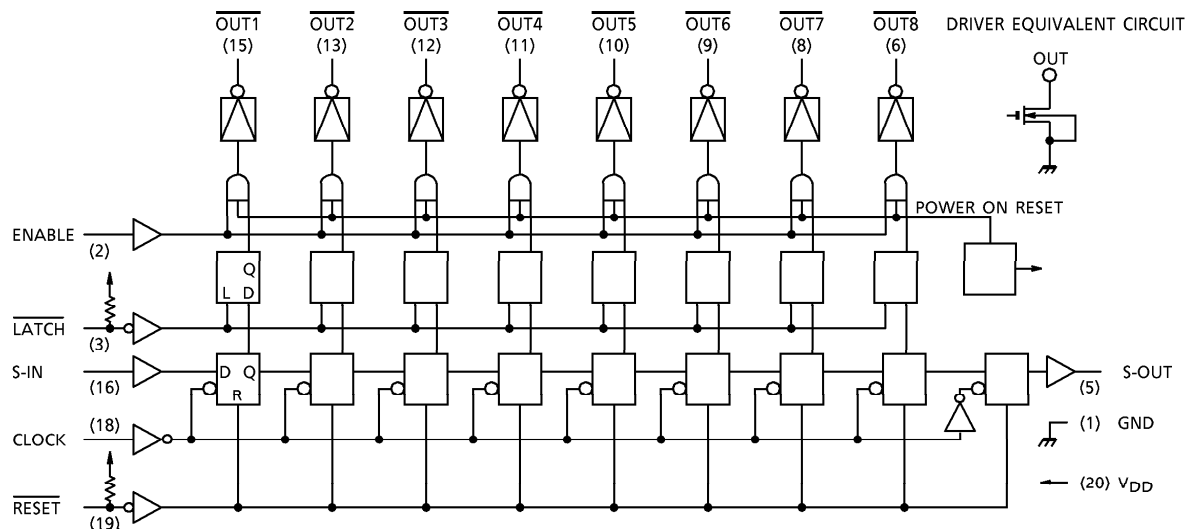


Weight : 0.79g (Typ.)

FEATURES

- Serial input and 8-stage parallel/serial output
- Serial output allows cascade expansion.
- $\overline{\text{ENABLE}}$ input for output control
- Large output current : 100mA (Max.)
- High output withstand voltage : 80V (Max.)
- Power detection circuit incorporated : The output is disabled when $V_{DD} < 3V$ (Typ).

BLOCK DIAGRAM AND PIN LAYOUT



961001EBA2

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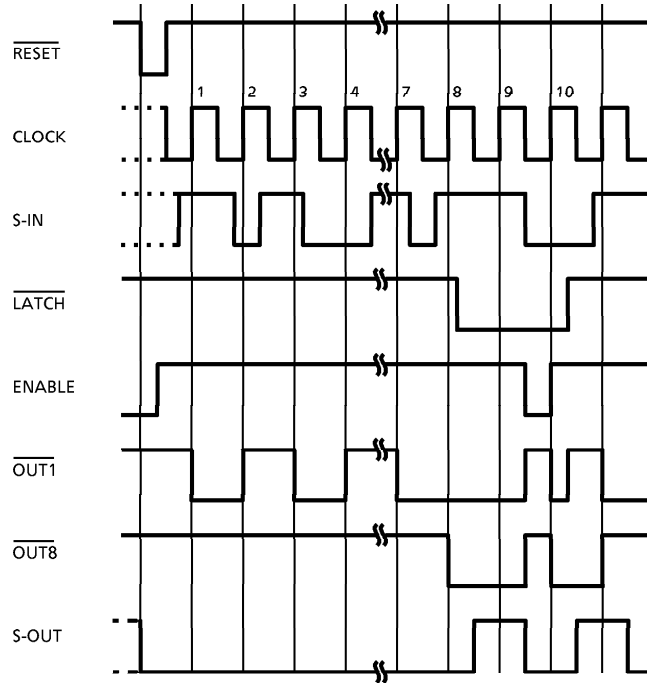
PIN DESCRIPTION

PIN No.	SYMBOL	DESCRIPTION
1	GND	Grounded. Must be connected to the FIN pin.
2	ENABLE	Data is output when this signal is high ; all output buffers turn off when the signal goes low.
3	$\overline{\text{LATCH}}$	Data is held when this signal is low ; data is rewritten when the signal goes high. When the pin is open, the signal is high.
5	S-OUT	Serial output pin allowing easy bit addition. To prevent malfunction, this pin has a function for a half-bit delay output.
6 ~15	$\overline{\text{OUT8}}$ $\sim\text{OUT1}$	Supplies shift register data or latch data. The signal is an N-channel MOS open-drain output.
16	S-IN	Serial data input pin.
18	CLOCK	Clock input pin for shift registers. The register acts at the leading edge of the clock.
19	$\overline{\text{RESET}}$	Clears data in the shift registers. The shift registers do not change when this signal is high ; they are reset when the signal goes low. When the pin is open, the signal is high.
20	V _{DD}	Power supply pin.
4, 7, 14, 17	NC	Not connected.
FIN	GND	Ground pin serving also as a heat sink. This pin must be connected to pin 1.

TRUTH TABLE

CK	E	$\overline{\text{R}}$	$\overline{\text{LATCH}}$	S-IN	OUT		S-OUT	CK = CLOCK E = ENABLE $\overline{\text{R}}$ = $\overline{\text{RESET}}$ S-IN = SERIAL IN OUT-PARALLEL OUT S-OUT = SERIAL OUT * = DON'T CARE
					Q1	Qn		
	H	H	H	L	OFF	$\overline{\text{Qn-1}}$	Q7	
	H	H	H	H	ON	$\overline{\text{Qn-1}}$	Q7	
	H	H	L	*	NC	NC	Q7	
	L	H	*	*	NC	NC	Q7	
	*	*	*	*	NC	NC	Q7	
*	*	L	H	*	OFF	OFF	L	
*	H		L	*	NC	NC	L	

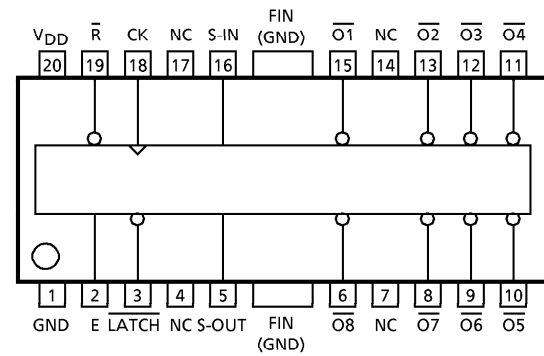
TIMING CHART



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	-0.3~7	V
Input Voltage	V _{IN}	-0.3~V _{DD} +0.3	V
Output Voltage	V _{OUT1} (Note 1)	-0.3~V _{DD} +0.3	V
	V _{OUT2} (Note 2)	-0.3~80	
Output Current	I _{OUT}	100	mA
Power Dissipation	P _D	1.0	W
Storage Temperature	T _{stg}	-55~150	°C
Lead Temperature-time	T _{sol}	260 (10s)	°C

PIN CONFIGURATION



(Note 1) S-OUT
 (Note 2) $\overline{O}UT1 \sim \overline{O}UT8$

RECOMMENDED OPERATING CONDITIONS (Ta = -40~105°C)

CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage			V _{DD}	—	—	4	5.0	6	V
Input Voltage			V _{IN}	—	—	0	—	V _{DD}	V
Output Current	High	S-OUT	I _{OH}	—	—	0	—	-1.0	mA
Output Voltage	High	\overline{Qn}	V _{OH}	—	—	0	—	60	V
Output Current	Low	S-OUT	I _{OL}	—	—	0	—	1.0	mA
		\overline{Qn}	I _{OL}	—	—	0	—	70	mA
Clock Frequency			f clock	—	—	0	—	1.0	MHz
Clock Pulse Width			tw clock	—	—	500	—	—	ns
Data Setup Time			t _{setup}	—	—	500	—	—	ns
Data Hold Time			t _{hold}	—	—	500	—	—	ns
Maximum Clock Time	Rise Time	t _r	—	—	—	—	—	70	μs
	Fall Time	t _f	—	—	—	—	—	70	μs

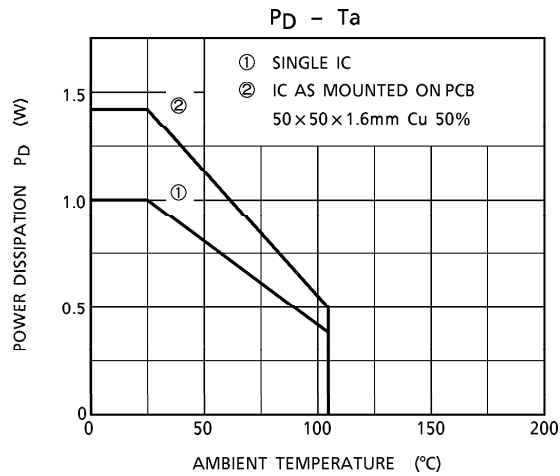
ELECTRICAL CHARACTERISTICS (Ta = -40~105°C, V_{DD} = 4~6V)

CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	High	V _{IH}	—	—	0.8 × V _{DD}	—	—	—	V
	Low	V _{IL}	—	—	—	—	0.2 × V _{DD}	—	
Input Current	\overline{R} , \overline{LATCH}	I _{IN}	—	V _{IN} = 0~V _{DD}	—	—	±100	μA	
	CK, S-IN, E	I _{IN}	—	V _{IN} = 0~V _{DD}	—	—	±1		
Output Voltage	High	S-OUT	V _{OH}	—	I _{OH} = -1mA	V _{DD} -0.4	—	—	V
Output Current	High	\overline{Qn}	I _{OH}	—	V _{OH} = 80V	—	—	100	μA
Output Voltage	Low	S-OUT	V _{OL}	—	I _{OL} = 1mA	—	—	0.4	V
		\overline{Qn}	V _{OL}	—	Ta = 25°C, I _{OL} = 100mA	—	—	1.2	V
Static Current Consumption			I _{DD} (1)	—	V _{DD} = 5V, f = 0Hz	—	—	1	mA
Dynamic Current Consumption			I _{DD} (2)	—	V _{DD} = 5V, f = 1MHz	—	—	5	mA

SWITCHING CHARACTERISTICS (Ta = -40~105°C, VDD = 4~6V)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Delay Time	High	CK-S-OUT	—	RL S-OUT = 2kΩ RL Qn = 150Ω CL = 15pF VIH = 3.0V, VIL = 0V Duty = 50%	—	0.1	0.5	μs
		CK-Qn			—	0.5	2.5	
	Low	CK-S-OUT			—	0.1	0.5	
		CK-Qn			—	0.3	1.5	
Maximum Clock Frequency		fmax	—	—	10	—	MHz	
Maximum Data Setup Time		tsetup	—	—	5	25	ns	
Minimum Data Hold Time		t hold	—	—	5	25	ns	
Maximum Clock Time	Rise Time	tr	—	—	70	—	μs	
	Fall Time	tf	—	—	70	—		

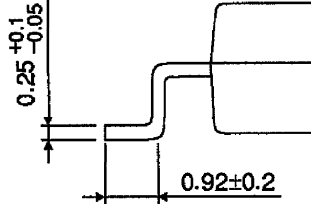
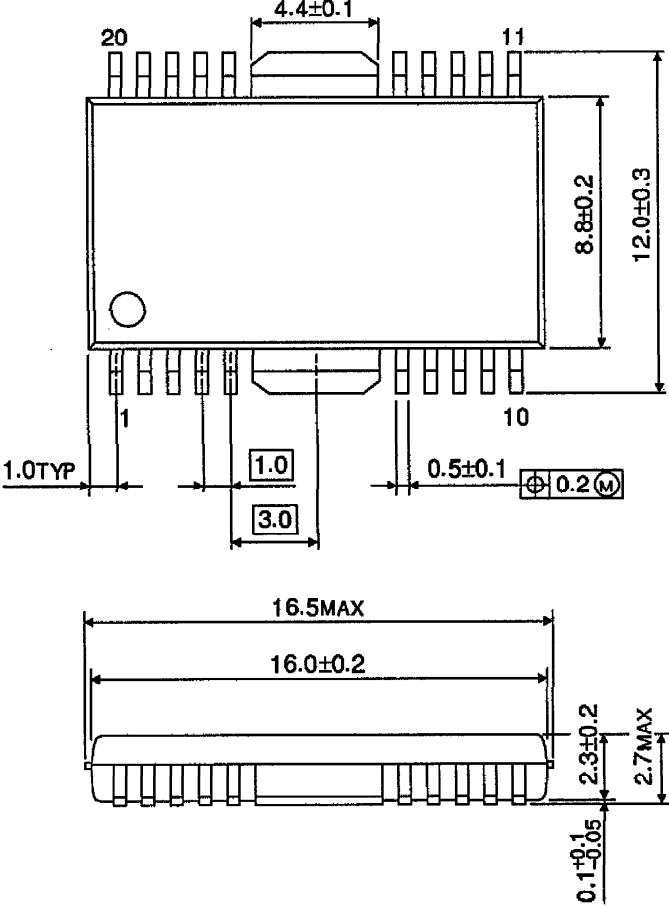
CL : Includes the capacitances of the measuring instrument and probe.



OUTLINE DRAWING

HSOP20-P-450-1.00

Unit : mm



Weight : 0.79g (Typ.)