International
IOR Rectifier

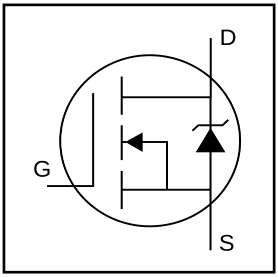
PD - 9.1015

PRELIMINARY

IRFBC30S/L

HEXFET® Power MOSFET

- Surface Mount (IRFBC30S)
- Low-profile through-hole (IRFBC30L)
- Available in Tape & Reel (IRFBC30S)
- Dynamic dv/dt Rating
- 150°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 600V

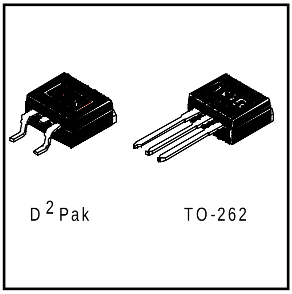
$R_{DS(on)}$ = 2.2Ω

I_D = 3.6A

Description

Third generation HEXFETs from international Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²Pak is a surface mount power package capable ofthe accommodatingdie sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRFBC30L) is available for low-profile applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V⑤	3.6	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V⑤	2.3	
I_{DM}	Pulsed Drain Current ①⑤	14	
P_D @T_A = 25°C	Power Dissipation	3.1	W
P_D @T_C = 25°C	Power Dissipation	74	W
	Linear Derating Factor	0.59	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	290	mJ
I_{AR}	Avalanche Current①	3.6	A
E_{AR}	Repetitive Avalanche Energy①	7.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	3.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

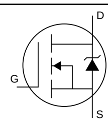
	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case	——	1.7	°C/W
$R_{θJA}$	Junction-to-Ambient (PCB Mounted,steady-state)**	——	40	

7/22/97

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.62	——	V/°C	Reference to 25°C, I_D =1mA⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	2.2	Ω	V_{GS} =10V, I_D =2.2A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	2.5	——	——	S	V_{DS} = 50V, I_D = 2.2A⑤
I_{DSS}	Drain-to-Source Leakage Current	——	——	100	µA	V_{DS} = 600V, V_{GS} = 0V
		——	——	500		V_{DS} = 480V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total Gate Charge	——	——	31	nC	I_D = 3.6A
Q_{gs}	Gate-to-Source Charge	——	——	4.6		V_{DS} = 360V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	17		V_{GS} = 10V, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	——	11	——	ns	V_{DD} = 300V
t_r	Rise Time	——	13	——		I_D = 3.6A
$t_{d(off)}$	Turn-Off Delay Time	——	35	——		R_G = 12Ω
t_f	Fall Time	——	14	——		R_D =82Ω, See Fig. 10 ④⑤
L_S	Internal Source Inductance	——	7.5	——	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	——	660	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	86	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	19	——		f = 1.0MHz, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	3.6	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	14		
V_{SD}	Diode Forward Voltage	——	——	1.6	V	T_J = 25°C, I_S =3.6A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	370	810	ns	T_J = 25°C, I_F =3.6A
Q_{rr}	Reverse Recovery Charge	——	2.0	4.2	µC	di/dt = 100A/µs ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} =50V, starting T_J = 25°C, L =41mH R_G = 25Ω, I_{AS} = 3.6A. (See Figure 12)

③ $I_{SD} \leq$ 3.6A, di/dt $\leq$ 60A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C

④ Pulse width ≤ 3000µs; duty cycle ≤ 2%.

⑤ Uses IRFBC30 data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

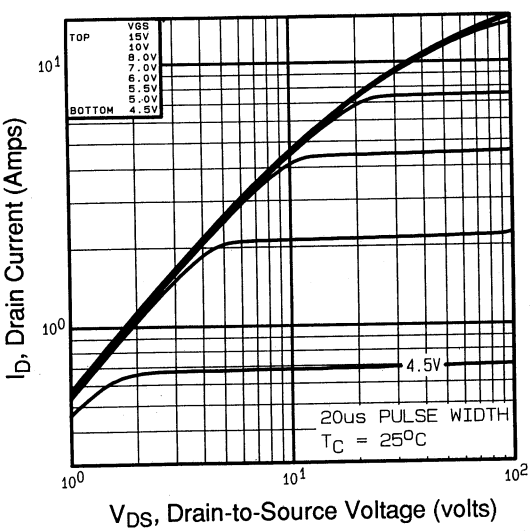


Fig 1. Typical Output Characteristics,

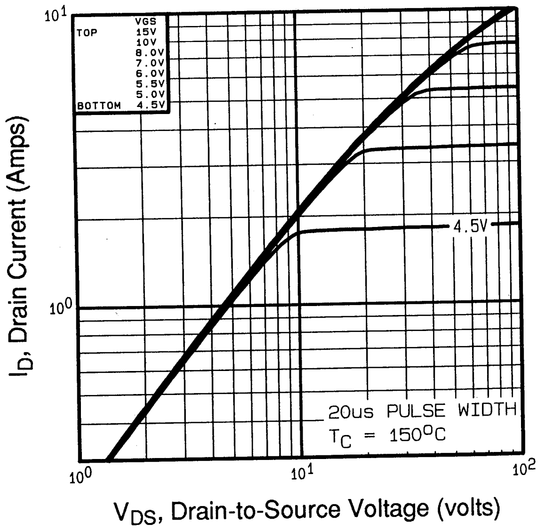


Fig 2. Typical Output Characteristics,

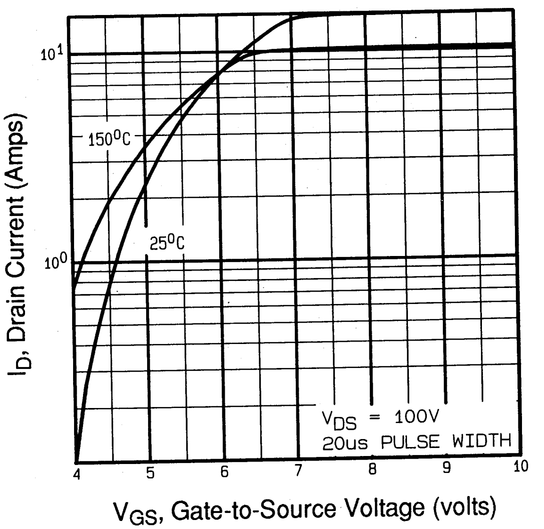


Fig 3. Typical Transfer Characteristics

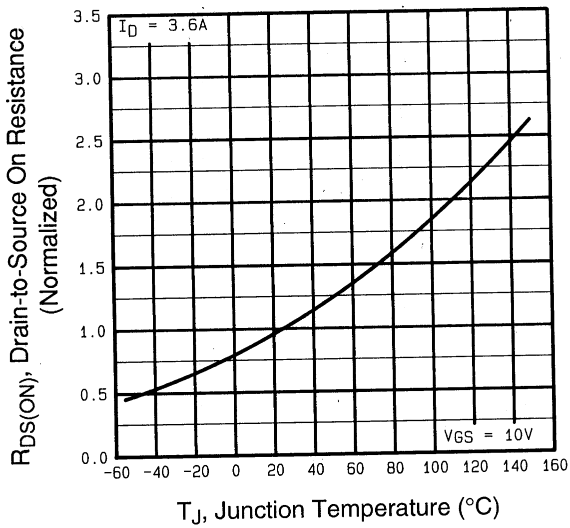


Fig 4. Normalized On-Resistance Vs. Temperature

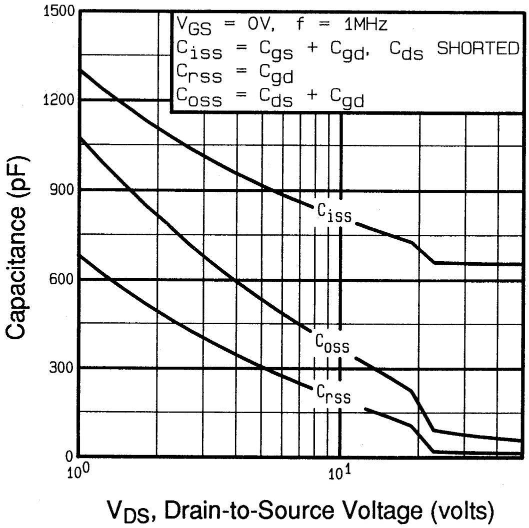


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

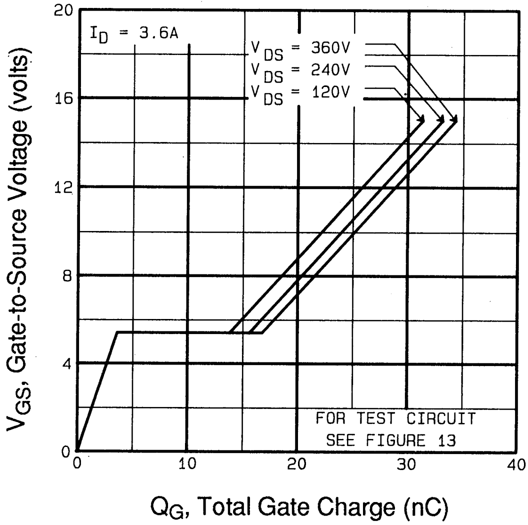


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

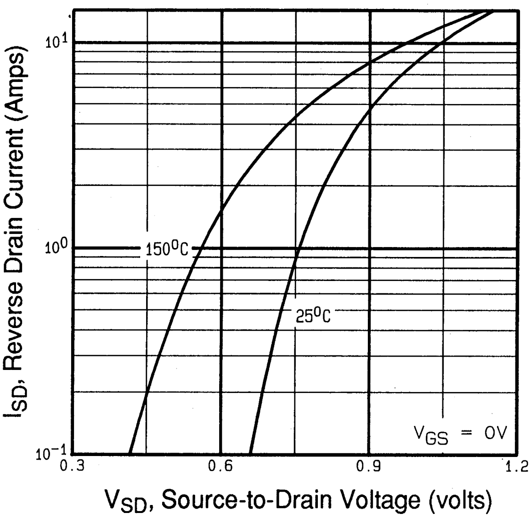


Fig 7. Typical Source-Drain Diode Forward Voltage

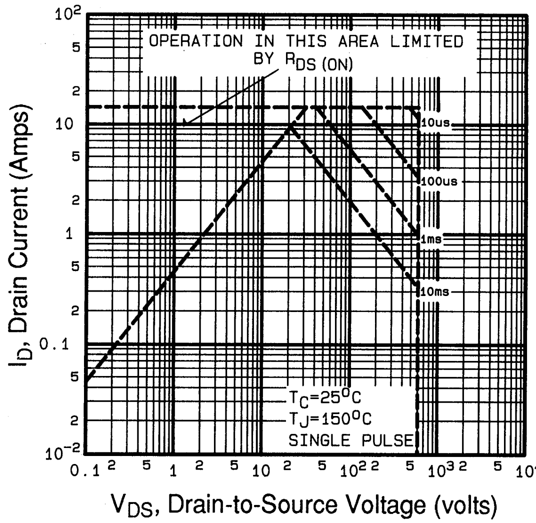


Fig 8. Maximum Safe Operating Area

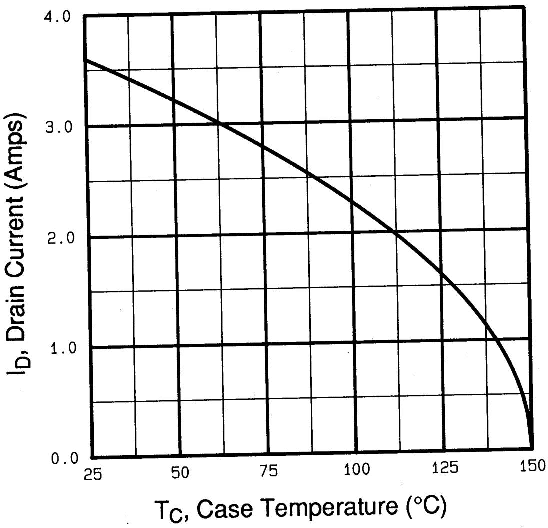


Fig 9. Maximum Drain Current Vs. Case Temperature

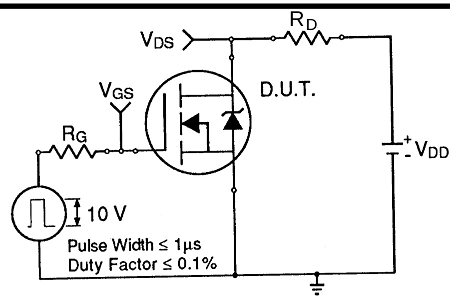


Fig 10a. Switching Time Test Circuit

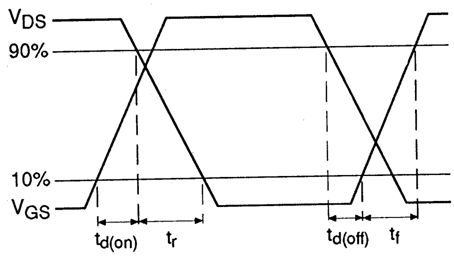


Fig 10b. Switching Time Waveforms

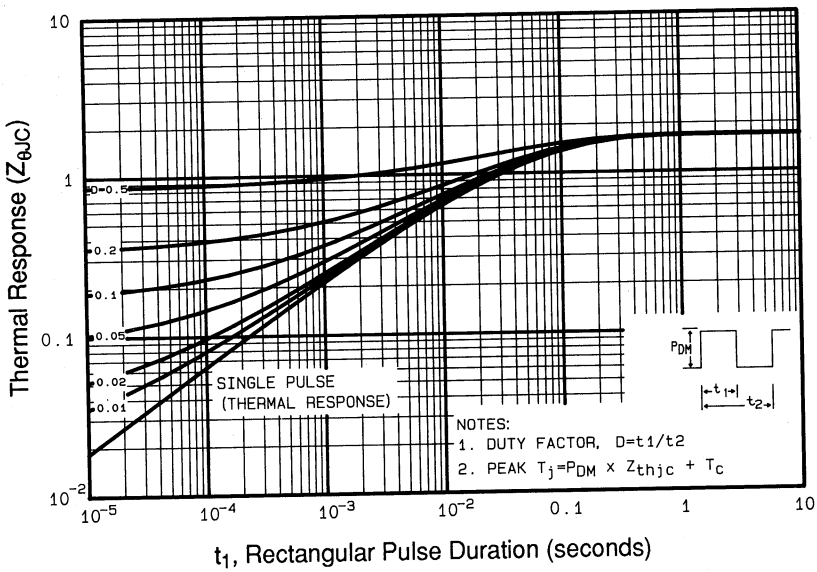


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

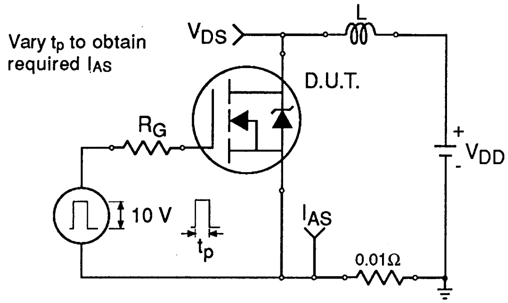


Fig 12a. Unclamped Inductive Test Circuit

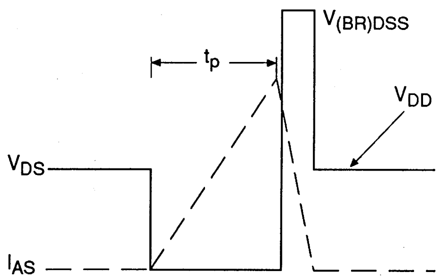


Fig 12b. Unclamped Inductive Waveforms

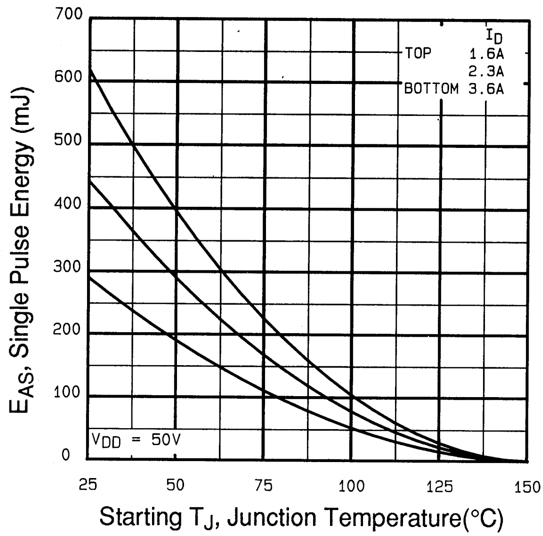


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

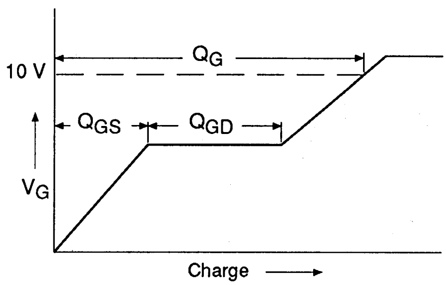


Fig 13a. Basic Gate Charge Waveform

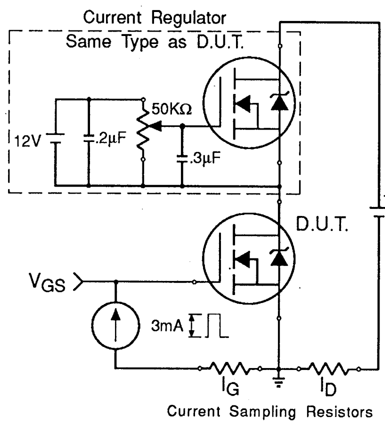
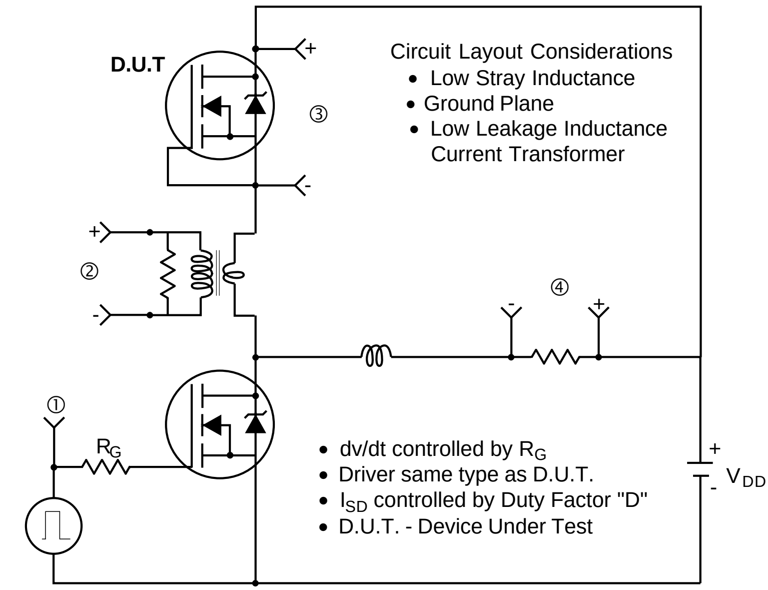
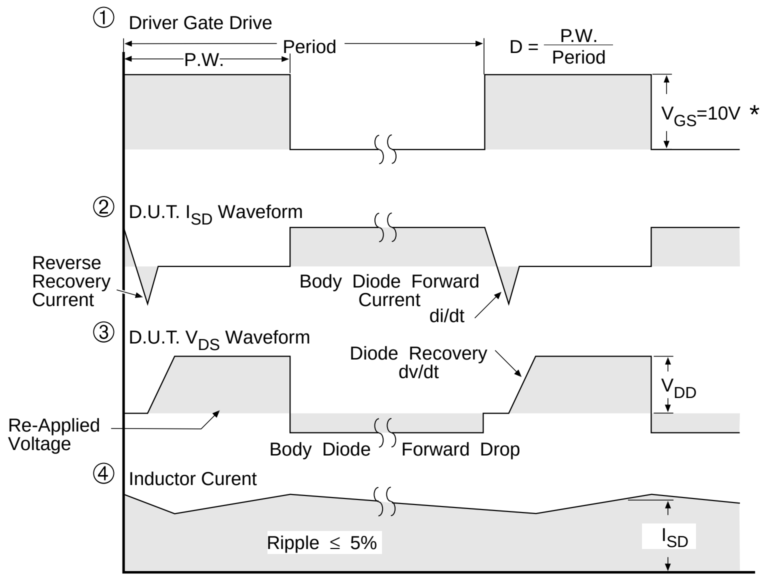


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

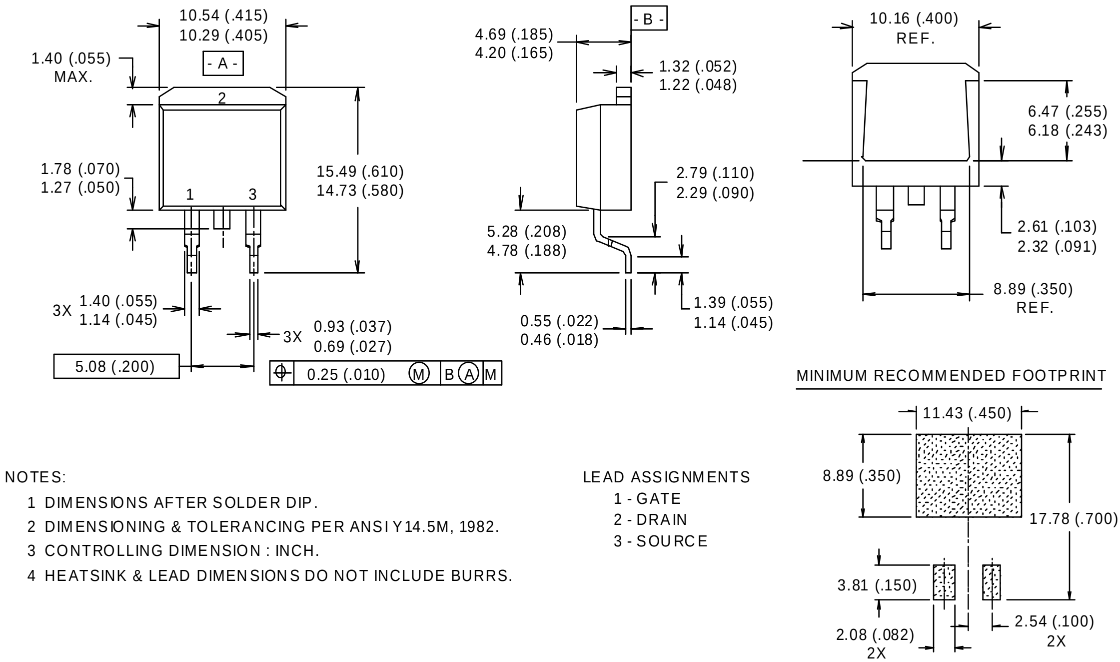




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

D²Pak Package Outline



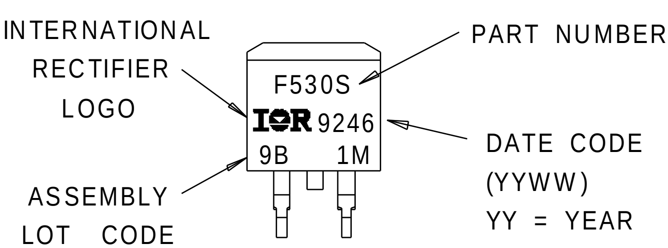
NOTES:

1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

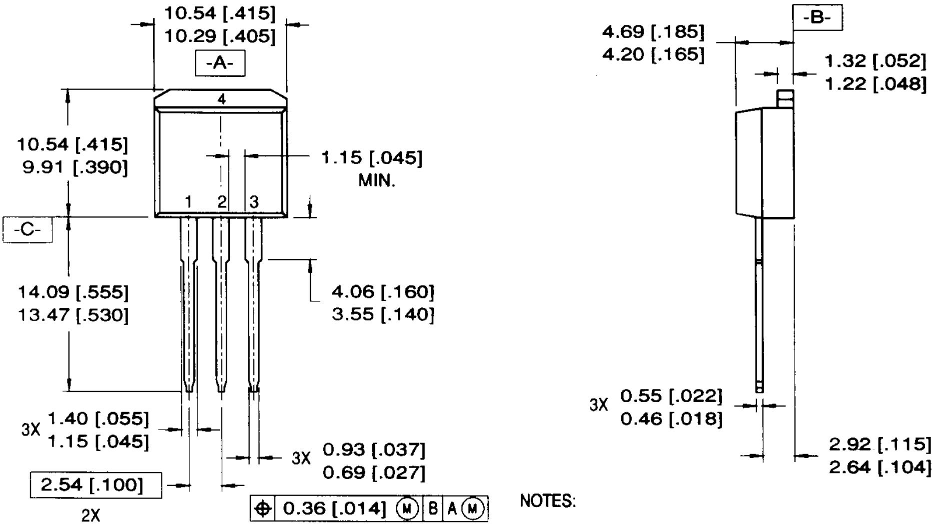
Part Marking Information

D²Pak



Package Outline

TO-262 Outline



LEAD ASSIGNMENTS

1 = GATE
2 = DRAIN
3 = SOURCE
4 = DRAIN

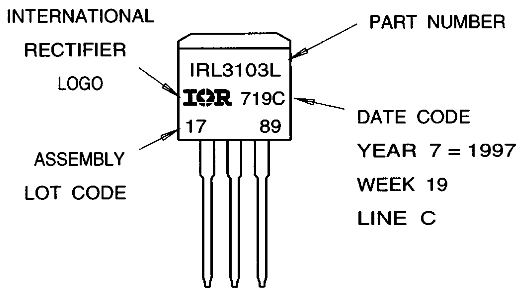
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

Part Marking Information

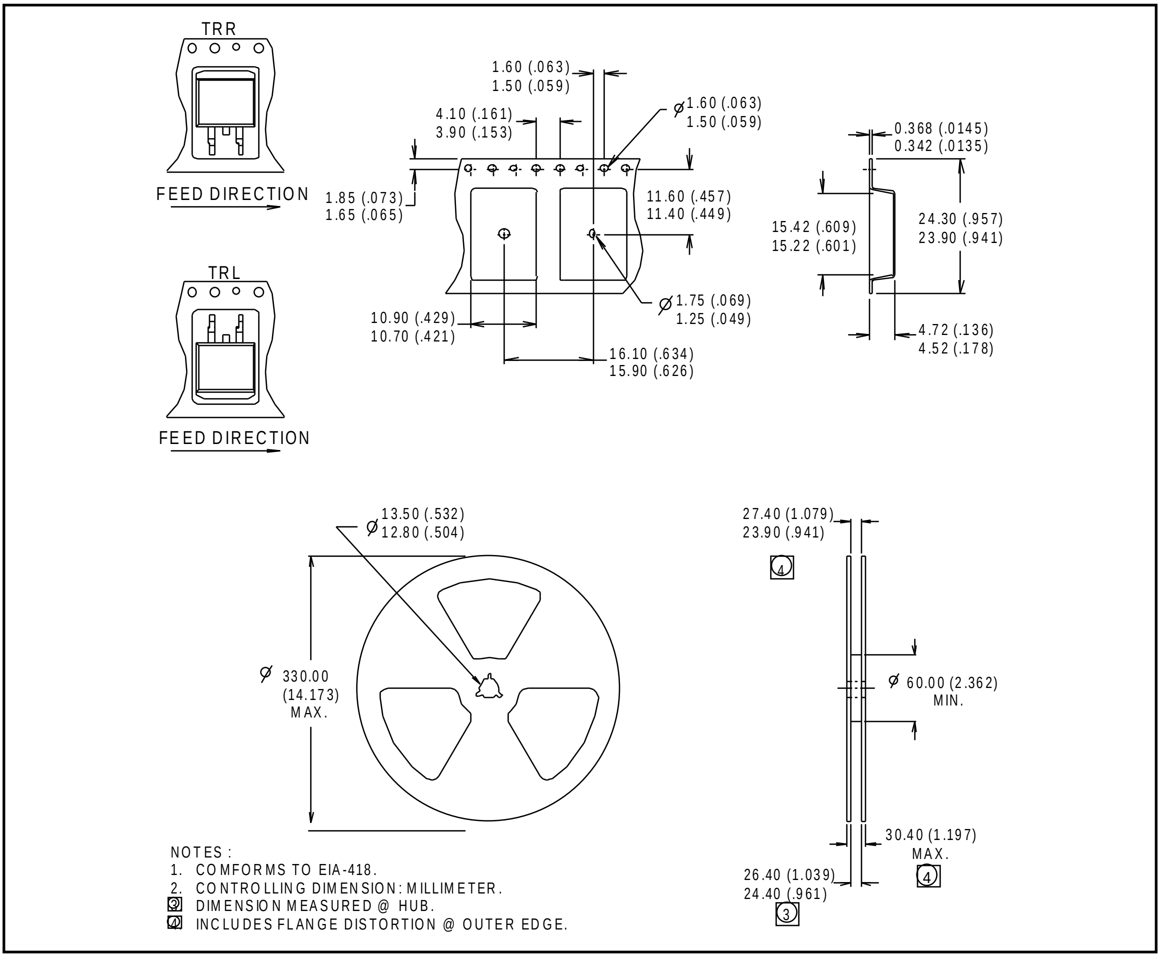
TO-262

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Tape & Reel Information

D²Pak



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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
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