LXT334

Quad Short-Haul Transceiver with Clock Recovery

Datasheet

The LXT334 is a quad, short-haul, PCM transceiver for 2.048 MHz or 1.544 MHz transmission systems. Its low impedance transmit output drivers provide constant line impedance whether transmitting marks or spaces. The output pulse amplitudes are also constant, stabilized against supply voltage variations.

The LXT334 can be configured for balanced 100/120 Ω or unbalanced 75 Ω systems and exceeds the latest ETSI return loss recommendations. An on-chip pulse shaping circuit generates accurate transmit pulses independent of the transmit clock duty cycle. All transmitters and receivers incorporate a power down mode with output tri-stating.

The LXT334 features differential receiver architecture with high noise interference margin. It uses peak detection with a variable threshold for reliable recovery of data as low as 500 mV (up to 12 dB of cable attenuation).

The fully digital clock recovery system uses a low frequency master clock of 2.048 MHz or 1.544 MHz as its reference. Each receiver incorporates a combination analog/digital Loss Of Signal (LOS) processor that meets the latest ITU G.775 standard. The LXT334 features a driver failure monitoring circuit in parallel to TTIP and TRING that reports driver shorts.

Applications

- High density line cards using digital backend ASICs

Product Features

- Fully integrated quad, short-haul PCM transceiver for G.703 2.048 Mbps or 1.544 Mbps operation
- Single rail supply voltage of 5 V (typical)
- Low power consumption of 410 mW (typical)
- Programmable G.703 transmit pulse shaping for G.703 75 Ω, 100 Ω and 120 Ω systems
- High performance line drivers with constant low impedance for 20 dB return loss (typical)
  exceeds ETSI 300 166
- On-chip band gap voltage reference for stabilized, constant output amplitude
- High-performance receivers recover data with up to 12 dB cable attenuation
- Low frequency 1.544 or 2.048 MHz reference clock
- On-chip clock recovery function
- Programmable unipolar and bipolar PCM interface
- On-chip AMI and HDB3 encoder/decoder
- On-chip Driver Failure Monitoring circuit
- Local and remote loopback testing function
- Independent Loss of Signal processor for each channel conforms to ITU G.775 recommendation
- Small-footprint 64-pin QFP

As of January 15, 2001, this document replaces the Level One document *LXT334 — Quad Short-Haul Transceiver with Clock Recovery*.

Order Number: 249077-001
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Datasheet

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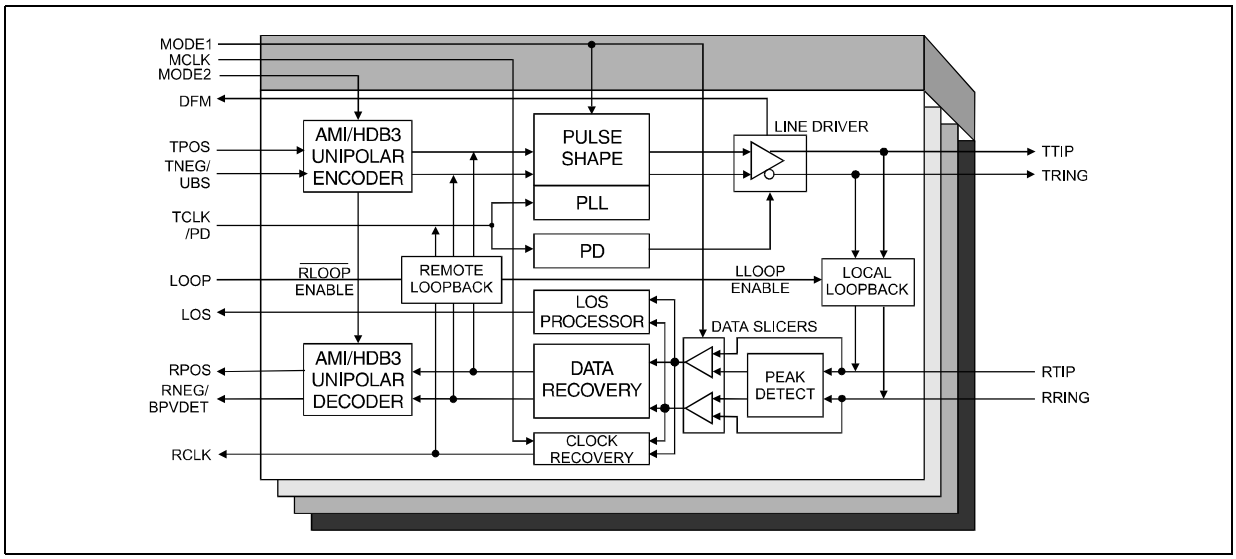
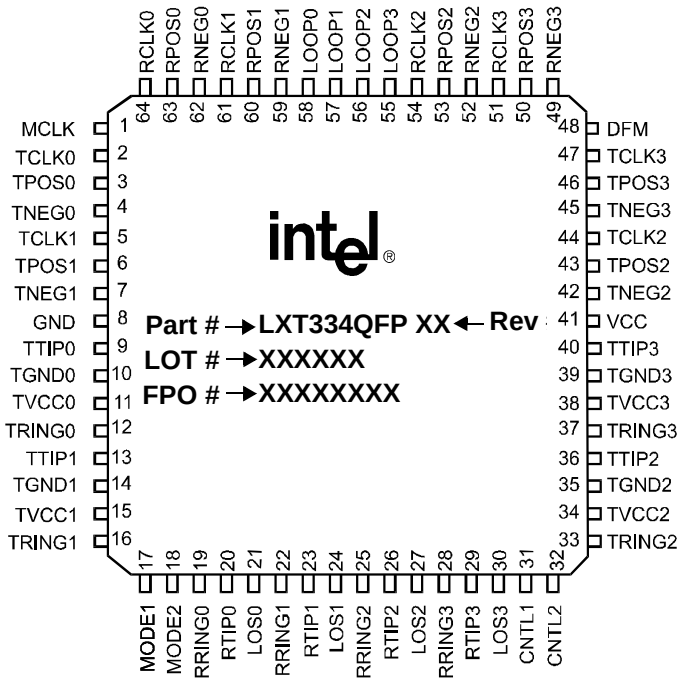
Figure 1. LXT334 Block Diagram



1.0 Pin Assignments & Signal Descriptions

Figure 2. LXT334 64 Pin Assignments and Markings



Package Topside Markings

Marking	Definition
Part #	Unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1. LXT334 Pin Descriptions

Pin #	Sym	I/O[1]	Description
1	MCLK	DI	**Master Clock Input.** An independent and free-running 2.048 or 1.544 MHz clock input generates the internal reference clocks for all transceivers. On Loss of Signal (LOS), the LXT334 derives RCLKx from this master clock. With MCLK asserted High, the LXT334 disables the PLL clock recovery circuits. The transceiver then feeds RPOSx and RNEGx to an internal XOR gate that performs logically-exclusive ORs for both data signals and connects this output to RCLKx for external clock recovery. In this mode, the LXT334 operates as a data recovery circuit. With MCLK asserted Low, the LXT334 powers down its clock and data recovery circuits and switches the output pins RCLKx, RPOSx and RNEGx to tri-state mode. Driving both MCLK and TCLKx Low powers the device down. MCLK — Operating Mode Clocked — Data/Clock Recovery L — Power Down H — Data Recovery
2	TCLK0	DI	**Transmit Clock/Transmit Power Down Input–Port 0.** All TCLKx pins are identical. The LXT334 samples TPOSx and TNEGx on the falling edge of TCLKx. With TCLKx asserted Low, the total transmit path, including the output drivers, enters a low-power, high-Z mode with all analog and digital circuitry powered down. With TCLKx asserted High for more than 16 clock cycles, the TPOSx and TNEGx duty cycles determine the transmit output pulse widths. In this mode, the LXT334 operates as a line driver. TCLK*x* — Operating Mode Clocked — Transmitter H — Line Driver (or TAOS if MCLK is Clocked) L — Power Down MCLK active with TCLK*x* High sets TAOS (Transmit All Ones) Mode.
3	TPOS0/ TDATA0	DI	**Transmit Positive Data/Transmit Data Input–Port 0.** All TPOSx/TDATAx pins are identical. In bipolar mode this pin (TPOSx) acts as active High input for the positive pulse to be transmitted. In unipolar mode this pin (TDATAx) acts as active High input for the data to be transmitted on the line.
4	TNEG0/ UBS0	DI	**Transmit Negative Data/Unipolar-Bipolar Select Input–Port 0.** All TNEGx/UBSx pins are identical. In bipolar mode, this pin acts as input for the negative pulse to be transmitted. If this pin is asserted High for more than 16 TCLK cycles, the LXT334 switches to unipolar mode. The device immediately returns to bipolar mode once this pin goes Low. UBS*x* — Operating Mode L — Bipolar Mode H — Unipolar Mode
5	TCLK1	DI	**Transmit Clock/Transmit Power Down Input–Port 1.** See TCLK0, pin 2.
6	TPOS1/ TDATA1	DI	**Transmit Positive Data/Transmit Data Input–Port 1.** See TPOS0/TDATA0, pin 3.
7	TNEG1/ UBS1	DI	**Transmit Negative Data/Unipolar-Bipolar Select Input–Port 1.** See TNEG0/UBS0, pin 4.
8	GND	S	**Ground.**
9	TTIP0	AO	**Transmit Tip Output–Port 0.** All pin pairs TTIPx/TRINGx are identical. Pin pairs TTIPx/TRINGx are differential line driver outputs designed to drive 75Ω unbalanced or 100 Ω/120 Ω balanced cables using transformer coupling.
10	TGND0	S	**Transmit Ground–Port 0.** Ground return for transmit driver 0.
11	TVCC0	S	**Transmit Positive Supply–Port 0.** +5 VDC power supply input for transmit driver 0.
12	TRING0	AO	**Transmit Ring Output–Port 0.** All pin pairs TTIPx/TRINGx are identical. Pin pairs TTIPx/TRINGx are differential line driver outputs designed to drive 75 Ω unbalanced or 100 Ω/120 Ω balanced cables using transformer coupling. See TTIP0, pin 9.
13	TTIP1	AO	**Transmit Tip Output–Port 1.** See TTIP0, pin 9.

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply. **Note**: Do not leave digital inputs floating, with the exception of pins 17, 18, and 55-58.

Table 1. LXT334 Pin Descriptions (Continued)

Pin #	Sym	I/O[1]	Description
14	TGND1	S	**Transmit Ground–Port 1.** Ground return for transmit driver 1.
15	TVCC1	S	**Transmit Positive Supply–Port 1.** +5 VDC power supply input for transmit driver 1.
16	TRING1	AO	**Transmit Ring Output–Port 1.** See TRING0, pin 12.
17	MODE1	DI	**Mode 1 Select Input.** While CNTL1 is Low, and if this pin is asserted Low, all the LXT334 drivers are configured for low power mode with a typical peak pulse output voltage of 3 V. If this pin is asserted High, the LXT334 configures its line drivers for matched line drive mode with a typical peak pulse output voltage of 4 V. Both the driver and the receivers are set to drive transformers. MODE1 Operating Mode L Low Power Mode (See Figure 4 and Figure 7) H Matched Line Drive Mode (See Figure 5 and Figure 6) If CNTL1 is High, MODE1 controls the load-matching circuitry in the transceiver: MODE1 Load H 75 Ω L 120 Ω
18	MODE2	DI	**Mode 2 Select Input.** If this pin is pulled Low, all transceivers operate in E1 mode using AMI encoding. With this pin pulled High, all transceivers enter E1 mode using HDB3 encoding if operated in Unipolar Mode. With this pin left open the LXT334 enters T1 mode according to Recommendation G.703. MODE2 Operating Mode L E1 Mode with AMI Encoding H E1 Mode with HDB3 Encoding Open T1 Mode with AMI Encoding
19 20	RRING0 RTIP0	AI AI	**Receive Ring Input–Port 0/Receive TIP Input–Port 0.** These pins are the inputs of the fully differential line receiver.
21	LOS0	DO	**Loss of Signal Output–Port 0.** All LOSx pins are identical. This output is High when the incoming signal has no transitions, i.e., when it is more than 22 dB below the nominal 0 dB level for more than 32 consecutive pulse intervals. The LOS condition is cleared and the output pin returns Low when the incoming signal has transitions (i.e., when the signal level is equal to or greater than 21 dB below the nominal 0 dB level and the average ones density reaches 12.5%.). In data receiver mode, LOSx is a pure analog energy detector. In case of a driver fail condition (DFM = High) this pin acts as a Driver Fail Monitor change of status output to identify the specific driver with the problem.
22 23	RRING1R TIP1	AI AI	**Receive Ring Input–Port 1/Receive TIP Input–Port 1.** See RRING0, pin 19; RTIP0, pin 20.
24	LOS1	DO	**Loss of Signal Output–Port 1.** See LOS0, pin 21.
25 26	RRING2R TIP2	AI AI	**Receive Ring Input–Port 2/Receive TIP Input–Port 2.** See RRING0, pin 19; RTIP0, pin 20.
27	LOS2	DO	**Loss of Signal Output–Port 2.** See LOS0, pin 21.
28 29	RRING3R TIP3	AI AI	**Receive Ring Input–Port 3/Receive TIP Input–Port 3.** See RRING0, pin 19; RTIP0, pin 20.
30	LOS3	DO	**Loss of Signal Output–Port 3.** See LOS0, pin 21.

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply. **Note**: Do not leave digital inputs floating, with the exception of pins 17, 18, and 55-58.

Table 1. LXT334 Pin Descriptions (Continued)

Pin #	Sym	I/O[1]	Description
31 32	CNTL1 CNTL2	DI DI	**Control 1/Control 2.** Settings CNTL1 CNTL2 Result L L RPOS, RNEG valid on falling edge of RCLK L H RPOS, RNEG valid on rising edge of RCLK H L RPOS, RNEG valid on falling edge of RCLK; 120 Ω, 75 Ω load matching selected by MODE1 pin. H H *reserved–do not use this setting.*
33	TRING2	AO	**Transmit Ring Output–Port 2.** See TRING0, pin 12; TTIP0, pin 9.
34	TVCC2	S	**Transmit Power Supply–Port 2.** +5 VDC power supply input for transmit driver 2.
35	TGND2	S	**Transmit Ground–Port 2.** Ground return for transmit driver 2.
36	TTIP2	AO	**Transmit Tip Output–Port 2.** See TTIP0, pin 9.
37	TRING3	AO	**Transmit Ring Output–Port 3.** See TRING0, pin 12; TTIP0, pin 9.
38	TVCC3	S	**Transmit Power Supply–Port 3.** +5 VDC power supply input for transmit driver 3.
39	TGND3	S	**Transmit Ground–Port 3.** Ground return for transmit driver 3.
40	TTIP3	AO	**Transmit Tip Output–Port 3.** See TTIP0, pin 9.
41	VCC	S	**Positive Supply.**
42	TNEG2/ UBS2	DI	**Transmit Negative Data/Unipolar-Bipolar Select Input–Port 2.** See TNEG0/UBS0, pin 4.
43	TPOS2/ TDATA2	DI	**Transmit Positive Data/Transmit Data Input–Port 2.** See TPOS0/TDATA0, pin 3.
44	TCLK2	DI	**Transmit Clock/Transmit Power Down Input–Port 2.** See TCLK0, pin 2.
45	TNEG3/ UBS3	DI	**Transmit Negative Data/Unipolar-Bipolar Select Input–Port 3.** See TNEG0/UBS0, pin 4.
46	TPOS3/ TDATA3	DI	**Transmit Positive Data/Transmit Data Input–Port 3.** See TPOS0/TDATA0, pin 3.
47	TCLK3	DI	**Transmit Clock/Transmit Power Down Input–Port 3.** See TCLK0, pin 2.
48	DFM	DO	**Driver Failure Monitor Output.** When High, indicates a driver short in one of the output drivers. The LOSx output identifies the specific failing driver in this case.
49	RNEG3/ BPV3	DO	**Receive Negative Data/Bipolar Violation Indication Output–Port 3.** All RNEGx/BPVx pins are identical. In bipolar mode these pins act as active High bipolar non-return-to-zero (NRZ) receive signal outputs. A High signal on RNEGx corresponds to receipt of a negative pulse on RTIPx/RRINGx. A High signal on RPOSx corresponds to receipt of a positive pulse on RTIPx/RRINGx. Both signals are valid on the same edge of RCLKx, as determined by CNTL1 and CNTL2. In unipolar mode, the LXT334 asserts the BPV*x* pin High any time it senses an In-Service Line Code violation. (*In data recovery mode, this pin is active Low.*) See RPOS3/RDATA3, pin 50; and Functional Description.
50	RPOS3/ RDATA3	DO	**Receive Positive Data/Receive Data Output–Port 3.** A High signal on RPOSx corresponds to receipt of a positive pulse on RTIPx/RRINGx. This signal is valid on the edge of RCLKx determined by CNTL1 and CNTL2. In unipolar mode (selected by pulling TNEG*x* High for more than 16 TCLK*x* periods) the LXT334 asserts RDATA*x* High when a mark has been received and is valid on the falling edge of RCLK*x*. RDATA*x* is an NRZ receive data output. (*In Data Recovery mode, this pin is active Low.*) See RNEG3/BPV3, pin 49.

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply. **Note**: Do not leave digital inputs floating, with the exception of pins 17, 18, and 55-58.

Table 1. LXT334 Pin Descriptions (Continued)

Pin #	Sym	I/O[1]	Description
51	RCLK3	DO	**Receive Clock Output–Port 3.** All RCLKx pins are identical. This pin provides the recovered clock from the signal received at RTIPx and RRINGx. In loss of signal conditions the LXT334 connects MCLK to this pin through internal circuitry. Asserting the MCLK pin High disables the clock recovery circuit and internally connects RPOS*x* and RNEG*x* to an XOR that is fed to the RCLK*x* output for external clock recovery applications.
52	RNEG2/ BPV2	DO	**Receive Negative Data/Violation Indication Output–Port 2.** See RNEG3/BPV3, pin 49; RPOS3/RDATA3, pin 50.
53	RPOS2/ RDATA2	DO	**Receive Positive Data/Receive Data Output–Port 2.** *(In Data Recovery Mode, this signal is active Low.)* See RPOS3/RDATA3, pin 50; RNEG3/BPV3, pin 49.
54	RCLK2	DO	**Receive Clock Output–Port 2.** See RCLK3, pin 51.
55	LOOP3	DI	**Loopback Mode Select Input–Port 3.** All LOOPx pins are identical. Driving this pin Low selects Remote Digital Loopback which causes the LXT334 to ignore any incoming data on TPOSx and TNEGx. It then retransmits data from RTIPx and RRINGx back to TTIPx and TRINGx at the RCLKx rate. Driving this pin High selects Local Loopback which causes the LXT334 to ignore data received on RTIP*x* and RRING*x* and loop data internally from TTIP*x* and TRING*x* back around to the receive inputs. Leaving this pin open selects normal operation mode. LOOP1 Operating Mode L Remote Loopback H Local Loopback Open Normal Operation Mode
56	LOOP2	DI	**Loopback Mode Select Input–Port 2.** See LOOP3, pin 55.
57	LOOP1	DI	**Loopback Mode Select Input–Port 1.** See LOOP3, pin 55.
58	LOOP0	DI	**Loopback Mode Select Input–Port 0.** See LOOP3, pin 55.
59	RNEG1/ BPV1	DO	**Receive Negative Data/Bipolar Violation Indication Output–Port 1.** See RNEG3/BPV3, pin 49; RPOS3/RDATA3, pin 50.
60	RPOS1/ RDATA1	DO	**Receive Positive Data/Receive Data Output–Port 1.** *(In Data Recovery Mode, this signal is active Low.)* See RPOS3/RDATA3, pin 50; RNEG3/BPV3, pin 49.
61	RCLK1	DO	**Receive Clock Output–Port 1.** See RCLK3, pin 51.
62	RNEG0/ BPV0	DO	**Receive Negative Data/Bipolar Violation Indication Output–Port 0.** See RNEG3/BPV3, pin 49; RPOS3/RDATA3, pin 50.
63	RPOS0/ RDATA0	DO	**Receive Positive Data/Receive Data Output–Port 0.** *(In Data Recovery Mode, this signal is active Low.)* See RPOS3/RDATA3, pin 50; RNEG3/BPV3, pin 49.
64	RCLK0	DO	**Receive Clock Output–Port 0.** See RCLK3, pin 51.

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply. **Note**: Do not leave digital inputs floating, with the exception of pins 17, 18, and 55-58.

2.0 Functional Description

The LXT334 is a fully integrated, quad line interface unit (QLIU) with four complete, independent transceivers. It supports G.703 applications at both 2.048 Mbps and 1.544 Mbps. All transceivers operate at the same frequency, determined by the MCLK input. Refer to the LXT334 block diagram on page 1.

The front end of each transceiver interfaces with four lines, one pair for transmit, and one pair for receive. Each transmit/receive line set constitutes a digital data loop for full duplex transmission.

Each transceiver also interfaces with back-end processors through bipolar or unipolar data I/O channels, and allows control by hardwired pins for stand-alone operation.

2.1 Receiver

The four receivers in the LXT334 are identical. The following paragraphs describe the operation of a single receiver.

The LXT334 receives the input signal at RTIP/RRING via a 1:1 transformer.

Data slicers and a peak detector process the received signal. The peak detector samples the received signal and determines its maximum value. A data-rate dependent percentage of peak value goes to the data slicers as a threshold level to ensure an optimum signal-to-noise ratio.

The receiver accurately recovers signals with up to -12 dB of cable loss. The minimum receiver sensitivity signal level is approximately 500 mV. Regardless of the received signal level, the LXT334 holds its peak detectors above a minimum level (0.225 V) to provide immunity from impulse noise.

After the data slicers process the received signal, it is fed to the data and timing recovery section, and to the receive monitor. The data and timing recovery circuits provide an input jitter tolerance significantly better than required by G.823 as shown in the Test Specifications section.

The recovered clock is output at RCLK in both bipolar and unipolar modes.

In bipolar mode, recovered data is active High and output at RPOS and RNEG; in unipolar mode recovered data is active High and output at RDATA.

If CNTL2 is Low, RPOS and RNEG outputs are valid on the falling edge of RCLK. IF CNTL1 is Low and CNTL2 is High, RPOS and RNEG outputs are valid on the rising edge of RCLK.

Asserting MCLK High disables the clock recovery function and switches all receivers to data recovery mode. In data recovery mode the RPOS/RNEG outputs are active Low. Asserting MCLK Low powers all receivers down and holds RPOS/RNEG and RCLK in a high impedance state.

2.1.1 Loss Of Signal Detector

2.1.1.1 LOS Detection at 2.048 MHz

During 2.048 MHz operation, the Loss of Signal (LOS) detector uses a combination analog and digital detection scheme and complies with the ITU G.775 recommendation.

The receiver monitor loads a digital counter at the RCLK frequency. The monitor increments the counter with each received 0, and resets it to 0 with each received 1 (mark). Any signal ~21 dB below the nominal 0 dB signal for 32 consecutive pulse intervals generates a LOS condition.

The LXT334 sets the LOS flag, and replaces the recovered clock with MCLK at the RCLK output in a smooth transition. (Receive operation requires MCLK.) LOS is cleared again when the signal level rises above ~21 dB (typical) below the minimum 0 dB level and the average 1s density reaches 12.5% (4 marks in a 32-bit window). Another smooth transition replaces MCLK with the recovered clock at RCLK. During LOS conditions, received data is output on RPOS/RNEG (or RDATA in unipolar I/O mode).

In data recovery mode, the LOS detector uses an analog detection scheme and complies with G.775. During LOS conditions, received data is output on RPOS/RNEG. Any signal 22 dB (typical) below the nominal 0 dB signal for more than approximately 16 µs generates a LOS condition. LOS is cleared when the signal level of the first 1 rises to more than 21 dB (typical) below the minimum 0 dB level.

2.1.1.2 LOS Detection at 1.544 MHz

During 1.544 MHz operation, the LXT334 asserts LOS if it receives 175 consecutive zeros, and deasserts LOS when the signal reaches 12.5% ones density (16 marks in a 128-bit window with no more than 99 consecutive zeros).

2.1.1.3 In-Service Code Violation Monitoring

In unipolar AMI I/O Mode, the LXT334 reports bipolar violations using an active High output for one RCLK cycle on the BPV output. A bipolar violation in AMI encoding mode is two consecutive marks of the same polarity. With the HDB3 detector enabled (pulling MODE2 High), the decoder will detect AMI code violations that are not part of a zero substitution code.

HDB3 code violations omit sequences of zeros that violate the coding rules. If an HDB3 code violation occurs, the decoder asserts the BPV output for one RCLK cycle during the period of the violating bit. In the event the decoder input receives a sequence of four or more zeros, it asserts the BPV output during the entire sequence of violating data bits.

2.2 Transmitter

The four low-power transmitters in the LXT334 are identical. The following paragraphs describe the operation of a single transmitter. The LXT334 has separate power supply (TVCC*x*/TGND*x*) for each output driver.

The LXT334 clocks transmit data from the back end serially into the device at TPOS/TNEG in the bipolar mode, or at TDATA in the unipolar mode.

The transmit clock (TCLK) supplies input synchronization. The LXT334 samples the TPOS/TNEG or TDATA input on the falling edge of TCLK. With no TCLK, the transmitter remains powered down and the TTIP/TRING outputs stay in their high-Z state.

Current limiters on the output drivers provide short circuit protection. (Refer to the Test Specifications section.) The LXT334 transmits data as a 50% AMI line code as shown in Figure 3. Pulling TCLK High with no MCLK input bypasses the transmitter PLL. In this case, TPOS and TNEG control the pulse width and polarity on TTIP and TRING.

The line driver provides a constant low output impedance of <3 Ω (typical), regardless of whether it is driving marks or spaces. This well-controlled impedance provides excellent return loss when used with external precision resistors (±1% accuracy) in series with the transformer.

The Application Information section lists recommended transformer specifications and ratios, and series resistor (Rt) values.

2.2.1 Line Protection

In the receive side, the 1 KΩ series resistors protect the receiver against current surges coupled into the device. Due to the high receiver impedance (40 kΩ typ.) the resistors do not affect the receiver sensitivity.

In the transmit side, the Schottky diodes D1-D4 protect the output driver.

While not mandatory for normal operation, these protection elements are strongly recommended to improve the design robustness.

2.2.2 Transmit All Ones Mode

Pulling TCLK High for more than 16 MCLK cycles activates Transmit All Ones Mode (TAOS) Mode. In TAOS Mode, the LXT334 ignores the TPOS and TNEG inputs and transmits marks continuously at the MCLK frequency.

2.2.3 Pulse Shape

The LXT334 generates transmit pulse shapes internally using a high-speed PLL and digital-to-analog converters and applies them to the AMI line driver for transmission onto the line at TTIP and TRING.

2.2.4 Driver Failure Monitor

In the event of a short circuit on any transmit line, the Driver Failure Monitor (DFM, common to all transceivers) goes High. The LOS pin (LOS*x*) for that specific port changes its indication status to flag a driver short condition.

DFM is in parallel with TTIP and TRING. The LXT334 uses a capacitor, charged by a measure of the driver output current and discharged by a measure of the maximum allowable current, to detect driver failure.

Shorted lines draw excessive current, overcharging the capacitor. When the capacitor charge is outside the nominal charge window, the LXT334 reports a driver short circuit failure. During a long string of spaces, this short-induced overcharge eventually bleeds off, clearing the DFM flag.

Figure 3. 50% AMI Pulse Form

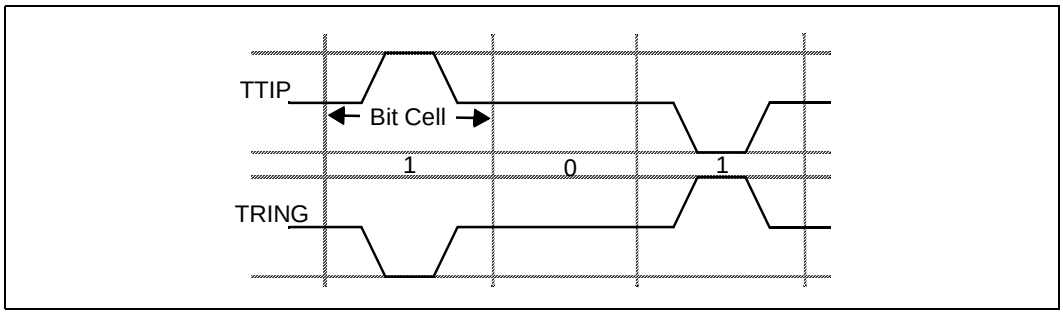
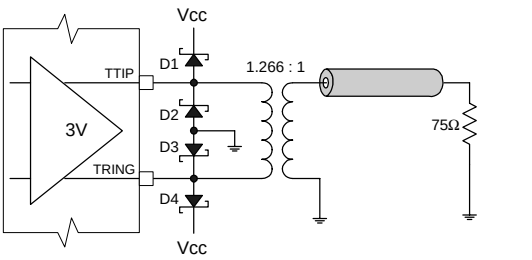


Table 2. Operating Mode Summary

MCLK	TCLK	LOOP	Receive Mode	Transmitter Mode	Loop
clocked	clocked	Open	Data/Clock Recovery	Normal	No Loopback
clocked	clocked	L	Data/Clock Recovery	Normal	Remote Loopback
clocked	clocked	H	Data/Clock Recovery	Normal	Local Loopback
L	clocked	Open	Power Down	Normal	No Loopback
L	clocked	L	Power Down	Normal	No Remote Loopback
L	clocked	H	Power Down	Normal	No Effect on Operation
L	H	Open	Power Down	Line Driver	No Loopback
L	H	L	Power Down	Line Driver	No Remote Loopback
L	H	H	Power Down	Line Driver	No Effect on Operation
L	L	X	Power Down	Power Down	No Loopback
H	clocked	Open	Data Recovery	Normal	No Loopback
H	clocked	L	Data Recovery	Line Driver	Remote Loopback
H	clocked	H	Data Recovery	Normal	Local Loopback
H	L	Open	Data Recovery	Power Down	No Loopback
H	L	L	Data Recovery	Power Down	No Effect on Operation
H	L	H	Data Recovery	Power Down	No Local Loopback
H	H	Open	Data Recovery	Line Driver	No Loopback
H	H	L	Data Recovery	Line Driver	Remote Loopback
H	H	H	Data Recovery	Line Driver	Local Loopback
clocked	L	Open	Data/Clock Recovery	Power Down	No Loopback
clocked	L	L	Data/Clock Recovery	Power Down	No Effect on Operation
clocked	L	H	Data/Clock Recovery	Power Down	No Local Loopback
clocked	H	Open	Data/Clock Recovery	Transmit All Ones	No Loopback
clocked	H	L	Data/Clock Recovery	Normal	Remote Loopback
clocked	H	H	Data/Clock Recovery	Transmit All Ones	Local Loopback

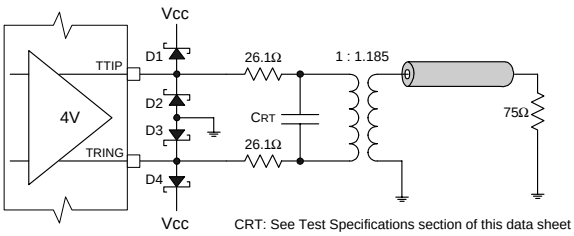
3.0 Application Information

Figure 4. E1 Low Power Tx I/F for Coax Cables



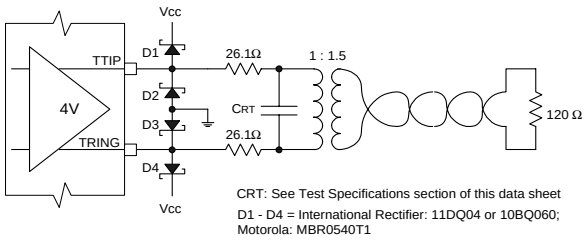
D1 - D4 = International Rectifier: 11DQ04 or 10BQ060; Motorola: MBR0540T1

Figure 5. E1 Matched Line Tx I/F for Coax Cables for High Return Loss



CRT: See Test Specifications section of this data sheet
D1 - D4 = International Rectifier: 11DQ04 or 10BQ060;
Motorola: MBR0540T1

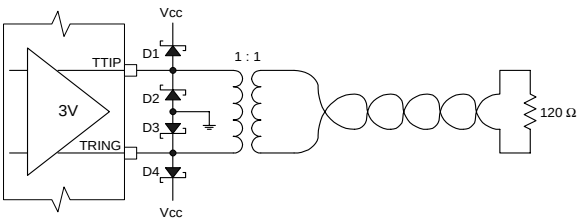
Figure 6. E1 Matched Line Tx I/F for Twisted-Pair Lines for High Return Loss



CRT: See Test Specifications section of this data sheet

D1 - D4 = International Rectifier: 11DQ04 or 10BQ060; Motorola: MBR0540T1

Figure 7. E1 Low Power Tx I/F for Twisted-Pair Lines



D1 - D4 = International Rectifier: 11DQ04 or 10BQ060; Motorola: MBR0540T1

Figure 8. E1 Rx I/F for Coax Cables

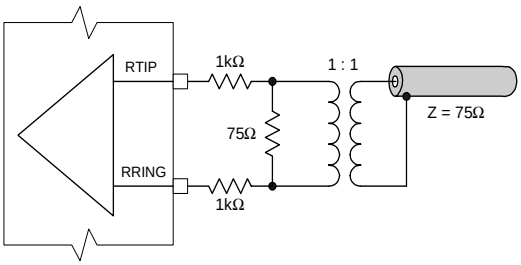


Figure 9. E1 Rx I/F for Twisted-Pair Lines

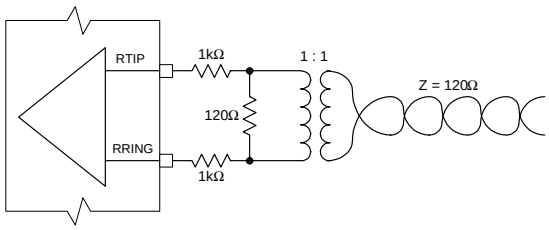
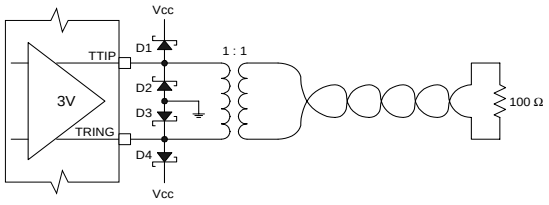


Figure 10. T1 Low Power Tx I/F for Twisted-Pair Lines



D1 - D4 = International Rectifier: 11DQ04 or 10BQ060; Motorola: MBR0540T1

Figure 11. T1 Matched Line Tx I/F for Twisted-Pair Lines

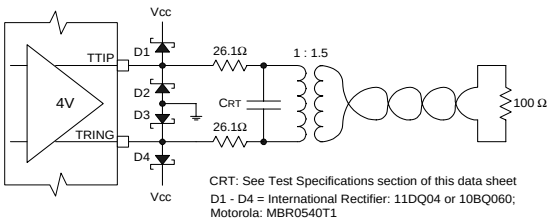


Figure 12. T1 Rx I/F for Twisted-Pair Lines

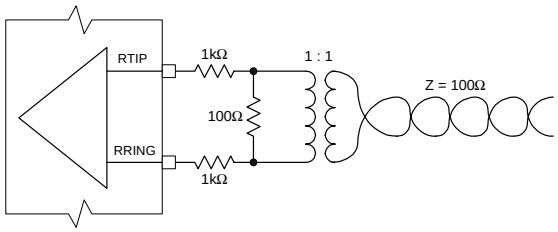


Table 3. Transformer Selection Guide[1]

Manufacturer	Transmit Side		Receive side (1:1 Ratio) (20 dB Return Loss)
	Part Number	Transformer Turns Ratio	Type
Pulse Engineering	PE-65586	1:1.36	Quad
	PE-65766	1:1.266	Dual
	PE-68789	1:1.5	Dual
	PE-65762	1:1.36	Dual
	PE-65861	1:2	Dual
	PE-65861	1:1	Dual
	PE-68789	1:1.185	Single
	PE-65389	1.266:1	Single
HALO	TG27-1505NX	1:1.36	Octal
	TD64-1205D	1:1.26	Dual
	TG29-1205NX	1:2	Octal
Bel-Fuse	0553-0013	1:1.36	Dual
	5006-1C	1:2	Dual

1. As of the publication date, Intel, has tested the transformers listed in this table. However, part numbers and specifications change without notice. Design engineers should validate components before committing to their use.

Table 3. Transformer Selection Guide[1]

Manufacturer	Transmit Side		Receive side (1:1 Ratio) (20 dB Return Loss)
	Part Number	Transformer Turns Ratio	Type
Schott Corp	67129300	1:2	Single
Valor	ST 5078	1:1.36	Dual
	ST 5170T	1:1.36	Octal

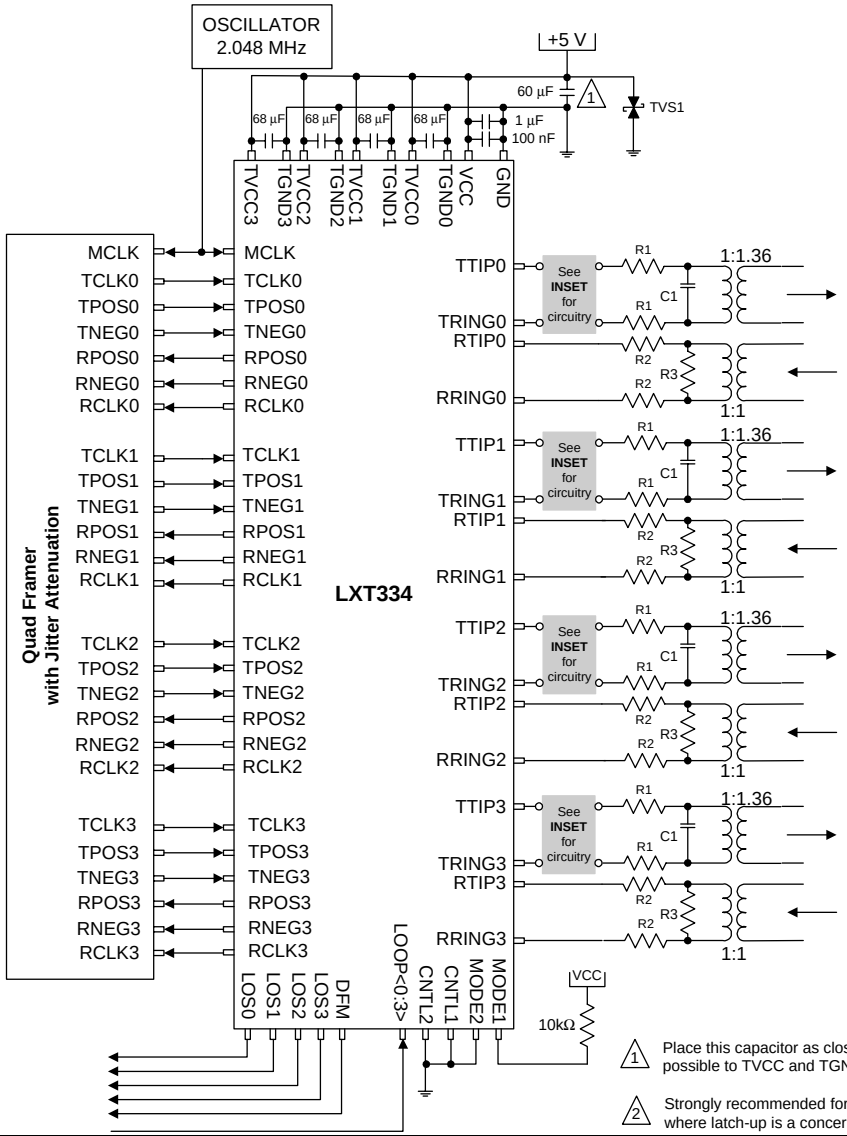
1. As of the publication date, Intel, has tested the transformers listed in this table. However, part numbers and specifications change without notice. Design engineers should validate components before committing to their use.

Table 4. Transmit Transformer and Resistor Combinations

Transformer	Resistor	Return Loss[1]	CNTL1	MODE1	Impedance
1.266:1	0 Ω	< 1 dB	Low	Low	75 Ω
1:1	0 Ω	< 1 dB	Low	Low	120 Ω
1:1.185	26.1 Ω	20 dB	Low	High	75 Ω
1:1.5	26.1 Ω	20 dB	Low	High	120 Ω
1:1.36	25 Ω	18 dB	Low	High	75 Ω
1:1.36	25 Ω	18 dB	Low	High	120 Ω
1:2	15 Ω	≥ 8 dB	High	High	75 Ω
1:2	15 Ω	≥ 8 dB	High	Low	120 Ω

1. Typical values 51 kHz - 3.078 MHz

Figure 13. E1 120 Ω and 75 Ω Matched Line Applications



Component	Application	
	120 Ω	75 Ω
R1. Transmit resistor	25 Ω	25 Ω
R2. Receive resistor	1 kΩ	1 kΩ
R3. Receive terminating resistor	120 Ω	75 Ω
C1. Transmit capacitor (typical)	180 pF	180 pF
D1 - D4. Protection diodes (Schottky)	International Rectifier: 11DQ04 or 10BQ060 Motorola: MBR0540T1	
TVS1. Transient Voltage Suppressor	Semtech: SMCJ5.0AC or equivalent	

4.0 Test Specifications

Note: The minimum and maximum values in Table 5 through Table 14 and Figure 14 through Figure 19 represent the performance specifications of the LXT334 and are guaranteed by test except, where noted, by design or other correlation methods.

Table 5. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Unit
DC supply voltage	RVCC, RGND	-0.3	6.0	V
Input voltage on any pin[1]	VIN	GND -0.3	RVCC + 0.3	V
Input voltage on RTIP/RRING	VIN	-6	RVCC + 0.3	V
Transient latchup current on any pin[2]	IIN	–	100	mA
Input current on any digital pin[3]	IIN	-10	10	mA
DC input current on TTIP, TRING[3]	IIN	–	±100	mA
DC input current on RTIP, RRING[3]	IIN	–	±20	mA
Storage temperature	TSTOR	-65	+150	°C
Total package power dissipation	–	–	1	W

Caution: Exceeding these values may cause permanent damage to the device. Operation is not guaranteed under these conditions. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.

1. Referenced to ground.
2. Exceeding these values will cause SCR latch-up.
3. Constant input current.

Table 6. Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Unit	Test Condition
DC supply voltage[1]	V+	4.75	5.0	5.25	V	
Ambient operating temperature	TA	-40	25	+85	° C	

1. TVcc must not differ from RVCC by more than ± 0.3 V.

Table 7. DC Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Digital I/O pins	High level input voltage	VIH	2.0	–	–	V	
	Low level input voltage	VIL	—	–	0.8	V	
	High level output voltage[2]	VOH	3.5	–	–	V	IOUT= -400µA
	Low level output voltage[2]	VOL	—	–	0.4	V	IOUT= 1.6 mA

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Output Drivers will output CMOS logic levels into CMOS loads.
3. 100% 1s density. Power dissipation including device load while driving a matched line over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
4. 50% 1s density. Power dissipation including device load while driving a line without matching resistors over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
5. Applies to the following pins: 9, 12, 13, 16, 33, 36, 37, 40, 49-54, 59-64.

Table 7. DC Characteristics (over recommended range) (Continued)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Input leakage current (digital input pins)		IIL	-10	–	+10	µA	
Tristate leakage current[5]		IHZ	-10		+10	µA	
Driver short circuit current	E1	–	–	–	50	mA	See Figure 5 and Figure 6
	T1	–	–	–	150	mA	See Figure 10
MODE input pins	Low level input voltage	VINL	–	–	1.5	V	pins 17, 18, 55, 56, 57, 58
	High level input voltage	VINH	3.5	–	–	V	
	Midrange input voltage	VINM	2.3	2.5	2.7	V	
	Low level input current	IINL	–	–	50	µA	
	High level input current	IINH	–	–	50	µA	
Total power dissipation [3]	75 Ω system (MODE1=H)	PD	–	660	750	mW	Figure 5
	120 Ω system (MODE1=H)	PD	–	660	750	mW	Figure 6
	100 Ω system (MODE1=H; MODE2=Open)	–	–	680	895	mW	Figure 11
Total power dissipation[4]	75 Ω system (MODE1=L)	PD	–	410	470	mW	Figure 4
	120 Ω system (MODE1=L)	PD	–	410	470	mW	Figure 7
	100 Ω system (MODE1=L; MODE2=Open)	–	–	370	500	mW	Figure 10
Power down current		ICCO	–	–	10	mA	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Output Drivers will output CMOS logic levels into CMOS loads.
3. 100% 1s density. Power dissipation including device load while driving a matched line over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
4. 50% 1s density. Power dissipation including device load while driving a line without matching resistors over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
5. Applies to the following pins: 9, 12, 13, 16, 33, 36, 37, 40, 49-54, 59-64.

Table 8. 2.048 MHz Transmit Characteristics in Transformer Coupling Mode (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Output pulse amplitude	75 Ω	–	2.13	2.37	2.61	V	Tested at the line side.
	120 Ω	–	2.7	3.0	3.3	V	Tested at the line side.
Peak voltage of a space	75 Ω	–	-0.237	0	0.237	V	
	120 Ω	–	-0.3	0	0.3	V	
Positive to negative pulse imbalance		–	0.95	–	1.05	–	
Transmit amplitude variation with supply		–	–	1	–	%	
Driver output impedance[4]		–	–	3	–	W	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Per ITU I.431 recommendation (4.1.2.3.) for a window of 17 consecutive bits.
3. With no jitter at the input used for synchronization or when using an externally supplied jitter free master clock the peak to peak jitter will not exceed the specified value.
4. Guaranteed by design and other correlation methods.

Table 8. 2.048 MHz Transmit Characteristics in Transformer Coupling Mode (over recommended range) (Continued)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Difference between pulse sequences[2, 4]		–	–	–	200	mV	
Transmit output jitter	20 Hz to 100 kHz[3]	–	–	–	0.04	U.I.	peak to peak
Output jitter in loopback mode[4]	20 Hz to 100 kHz	–	–	–	0.09	U.I.	peak to peak
Pulse width ratio of the positive and negative pulses		–	0.95	–	1.05	–	At the nominal half amplitude.
Transmit return loss[4]	51 kHz to 102 kHz	–	20	–	–	dB	See Application Information, Figure 5 & Figure 6.
	102 kHz to 2.048 MHz	–	20	–	–	dB	
	2.048 MHz to 3.072 MHz	–	20	–	–	dB	
Transmit load capacitance		CRT	–	180	–	pF	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Per ITU I.431 recommendation (4.1.2.3.) for a window of 17 consecutive bits.
3. With no jitter at the input used for synchronization or when using an externally supplied jitter free master clock the peak to peak jitter will not exceed the specified value.
4. Guaranteed by design and other correlation methods.

Table 9. 1.544 MHz Transmit Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Output pulse amplitude		–	2.4	3.0	3.6	V	Z_L = 100 Ω.
Peak voltage of a space		–	-0.15	0	0.15	V	Z_L = 100 Ω.
Transmit amplitude variation with supply		–	–	1	–	%	
Driver output impedance[4]		–	–	3	–	Ω	
Positive to negative pulse imbalance		–	–	–	0.5	dB	
Transmit output jitter [2]	10 Hz to 8 kHz[4]	–	–	–	0.02	U.I	peak to peak
	8 kHz to 40 kHz[4]	–	–	–	0.025	U.I.	
	10 Hz to 40 kHz[4]	–	–	–	0.025	U.I.	
	Broad Band	–	–	–	0.05	U.I.	
Output power level	772 kHz[3, 4]	–	12	–	19	dB	
Output power	1544 kHz relative to power at 772 kHz[4]	–	-29	–	–	dB	
Ratio of the pulse widths of the positive and negative pulses at the nominal half amplitude		–	0.95	–	1.05	–	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. With no jitter at the input used for synchronization or when using an externally supplied jitter free master clock the peak to peak jitter will not exceed the specified value.
3. The signal level is the power level measured in a 3 kHz bandwidth at the point where the signal arrives at the distribution frame for an all 1s pattern transmitted.
4. Guaranteed by design and other correlation methods.

Table 9. 1.544 MHz Transmit Characteristics (over recommended range) (Continued)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Transmit return loss [4]	51 kHz to 102 kHz	–	18	–	–	dB	See Applications Information section Figure 11.
	102 kHz to 2.048 MHz	–	18	–	–	dB	
	2.048 MHz to 3.072 MHz	–	18	–	–	dB	
Transmit load capacitance		CRT	–	180	–	pF	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. With no jitter at the input used for synchronization or when using an externally supplied jitter free master clock the peak to peak jitter will not exceed the specified value.
3. The signal level is the power level measured in a 3 kHz bandwidth at the point where the signal arrives at the distribution frame for an all 1s pattern transmitted.
4. Guaranteed by design and other correlation methods.

Table 10. 2.048 MHz Receive Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Permissible cable attenuation[2]		–	–	–	12	dB	@1024 kHz
Receiver dynamic range		DR	0.5	–	4.2	Vp	
Signal to noise interference margin [2, 6]		S/I	-15	–	–	dB	Per G.703, O.151, 6 dB of cable.
Signal to single tone interference margin		S/X	-14	–	–	dB	O.151, 6 dB of cable
Data decision threshold		SRE	43	50	57	%	Relative to peak input voltage.
Analog loss of signal threshold		–	–	225[5]	–	mV	
Loss of signal threshold hysteresis		–	–	2.5	–	dB	
Consecutive zeros before loss of signal		–	–	32	–		G.775 recommendation
Low limit input jitter tolerance [3]	1.2E-5 Hz to 20 Hz[6]	–	36	–	–	U.I.	G.735 recommendation See Note 1.
	20 Hz to 2.4 kHz[4]	–	1.5	–	–	U.I.	
	8 kHz to 100 kHz	–	0.2	–	–	U.I.	
RCLK output jitter[4, 6]	0 Hz to100 kHz	–	–	0.01	–	U.I.	peak to peak
Clock recovery PLL 3 dB bandwidth		–	–	10	–	kHz	
PLL peaking[6]		–	–	–	0	dB	
Receiver input impedance		–	–	40	–	kΩ	@1024 kHz RTIP to RRING

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. No errors shall occur when the combined signal attenuated by the maximum specified interconnecting cable loss is applied to the input port. See ITU O.151 recommendation for further details.
3. Sine wave jitter and wander with a peak to peak amplitude that corresponds at least to what is specified in Figure 18 shall not cause either a bit error or loss of frame alignment. As test signal an HDB3-coded digital signal with an electrical characteristic that complies with what is set forth in ITU G.703 shall be used. Test sequence is pseudo-random 2^{15}-1. See also ITU O.151.
4. If the LXT334 is configured as data receiver only and if a jitter free signal is applied to RTIP and RRING the added jitter must not exceed the specified value.
5. Equal to 22 dB below the nominal 0 dB level in 120 Ω systems.
6. Guaranteed by design and other correlation methods.

Table 10. 2.048 MHz Receive Characteristics (over recommended range) (Continued)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Receiver Return loss[6]	51 kHz–102 kHz	–	20	–	–	dB	See Application Information section, Figure 8 & Figure 9.
	102–2048 kHz	–	20	–	–	dB	
	2048 kHz–3072 kHz	–	20	–	–	dB	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. No errors shall occur when the combined signal attenuated by the maximum specified interconnecting cable loss is applied to the input port. See ITU O.151 recommendation for further details.
3. Sine wave jitter and wander with a peak to peak amplitude that corresponds at least to what is specified in Figure 18 shall not cause either a bit error or loss of frame alignment. As test signal an HDB3-coded digital signal with an electrical characteristic that complies with what is set forth in ITU G.703 shall be used. Test sequence is pseudo-random 2^{15}-1. See also ITU O.151.
4. If the LXT334 is configured as data receiver only and if a jitter free signal is applied to RTIP and RRING the added jitter must not exceed the specified value.
5. Equal to 22 dB below the nominal 0 dB level in 120 Ω systems.
6. Guaranteed by design and other correlation methods.

Table 11. 1.544 MHz Receive Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Permissible cable attenuation		–	–	–	12	dB	@772 kHz
Receiver dynamic range		DR	0.5	–	4.2	Vp	
Undershoot		US	–	–	62	%	
Data decision threshold		SRT	63	70	77	%	Relative to peak input voltage.
Loss of signal threshold		–	–	0.225	–	V	
Allowable consecutive 0s before LOS		–	–	175	–		
Low limit input jitter tolerance	18 kHz to 100 kHz	–	0.430	–	–	U.I.	G.735 recommendation
Clock recovery PLL 3 dB bandwidth		–	–	10	–	kHz	
PLL peaking[2]		–	–	–	0	dB	
Receiver input impedance		–	–	40	–	kΩ	RTIP to RRING @ 772 kHz
Input return loss[2]	51 kHz–102 kHz	–	20	–	–	dB	See Application Information section, Figure 12.
	102–2048 kHz	–	20	–	–	dB	
	2048 kHz–3072 kHz	–	20	–	–	dB	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.

Table 12. Transmit Timing Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Condition
Master clock frequency	E1	MCLK	–	2.048	–	MHz	
	T1	MCLK	–	1.544	–	MHz	
Master clock tolerance		MCLKt	–	±50	–	ppm	
Master clock duty cycle		–	40	–	60	%	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 12. Transmit Timing Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Condition
Output pulse width	E1	tPW	219	244	269	ns	
	T1	tPW	274	324	374	ns	
Transmit clock frequency	E1	TCLK	–	2.048	–	MHz	
	T1	TCLK	–	1.544	–	MHz	
Transmit clock tolerance		TCLKt	–	±50	–	ppm	
Transmit clock duty cycle		TCLKd	10	–	90	%	Normal Mode
TPOS/TNEG duty cycle		TPNd	48.4	–	51.6	%	Line Driver Mode
TPOS/TNEG to TCLK setup time		tSUT	25	–	–	ns	
TCLK to TPOS/TNEG hold time		tHT	25	–	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 14. LXT334 Transmit Timing Diagram

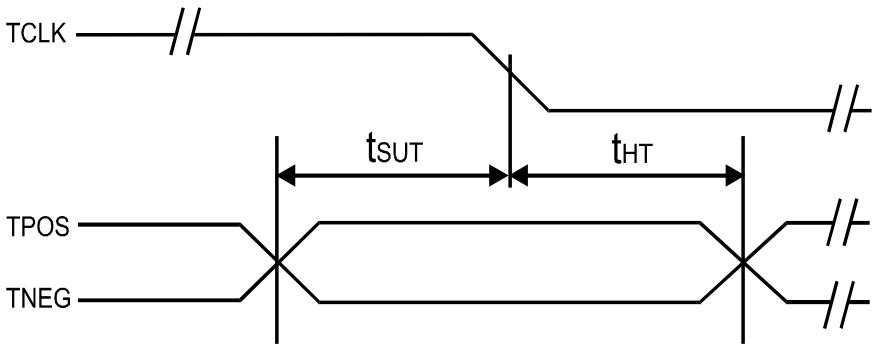


Table 13. Receive Timing Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Receive clock capture range		–	–	±80	–	ppm	
Receive clock duty cycle [2]		RLCKd	40	50	60	%	
Receive clock pulse width [2]	E1	tPW	447	488	529	ns	
	T1	tPW	594	648	702	ns	
Receive clock pulse width low time	E1	tPWL	203	244	285	ns	
	T1	tPWL	270	324	378	ns	
Receive clock pulse width high time	E1	tPWH	–	244	–	ns	
	T1	tPWH	–	324	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCLK duty cycles are for worst case jitter conditions (0.2 U.I. displacement for E1 and 0.4 U.I. for T1 operation).
3. This mode disables clock recovery.
4. If MCLK is High, the PLL clock recovery circuits are disabled. RPOSx and RNEGx are fed to an internal XOR gate that connects this output to RCLKx for external clock recovery.

Table 13. Receive Timing Characteristics (over recommended range) (Continued)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
RPOS/RNEG data low time (MCLK=H) [3,4]		tPWD1	200	244	300	ns	
RPOS/RNEG to RCLK rising setup time	E1	tSUR	50	203	–	ns	
	T1	tSUR	50	270	–	ns	
RCLK rising to RPOS/RNEG hold time	E1	tHR	50	203	–	ns	
	T1	tHR	50	270	–	ns	
Delay time between RPOS/RNEG and RCLK		–	–	5	–	ns	MCLK = H

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCLK duty cycles are for worst case jitter conditions (0.2 U.I. displacement for E1 and 0.4 U.I. for T1 operation).
3. This mode disables clock recovery.
4. If MCLK is High, the PLL clock recovery circuits are disabled. RPOSx and RNEGx are fed to an internal XOR gate that connects this output to RCLKx for external clock recovery.

Figure 15. LXT334 Receive Timing Diagram

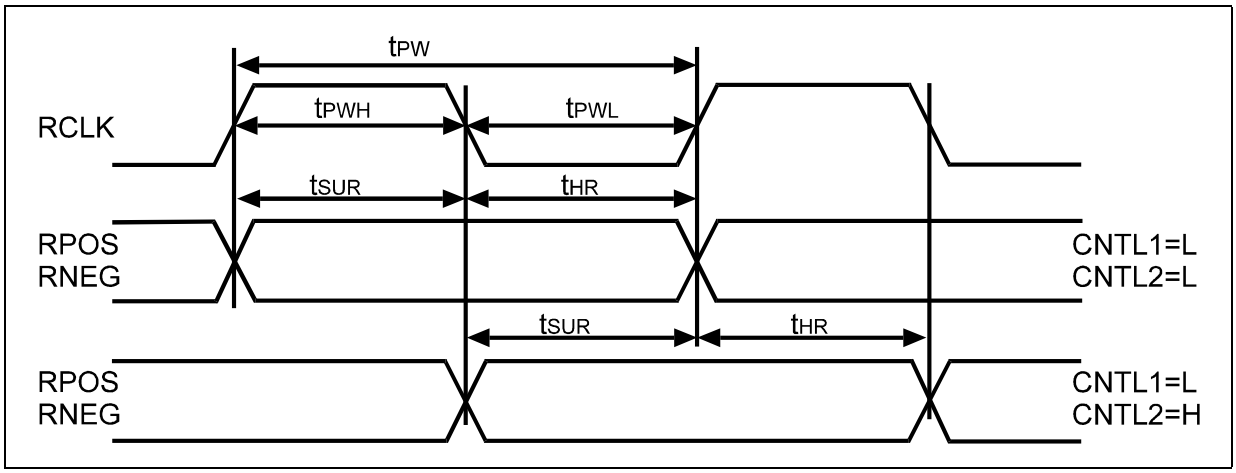


Figure 16. 2.048 MHz Pulse Mask G.703

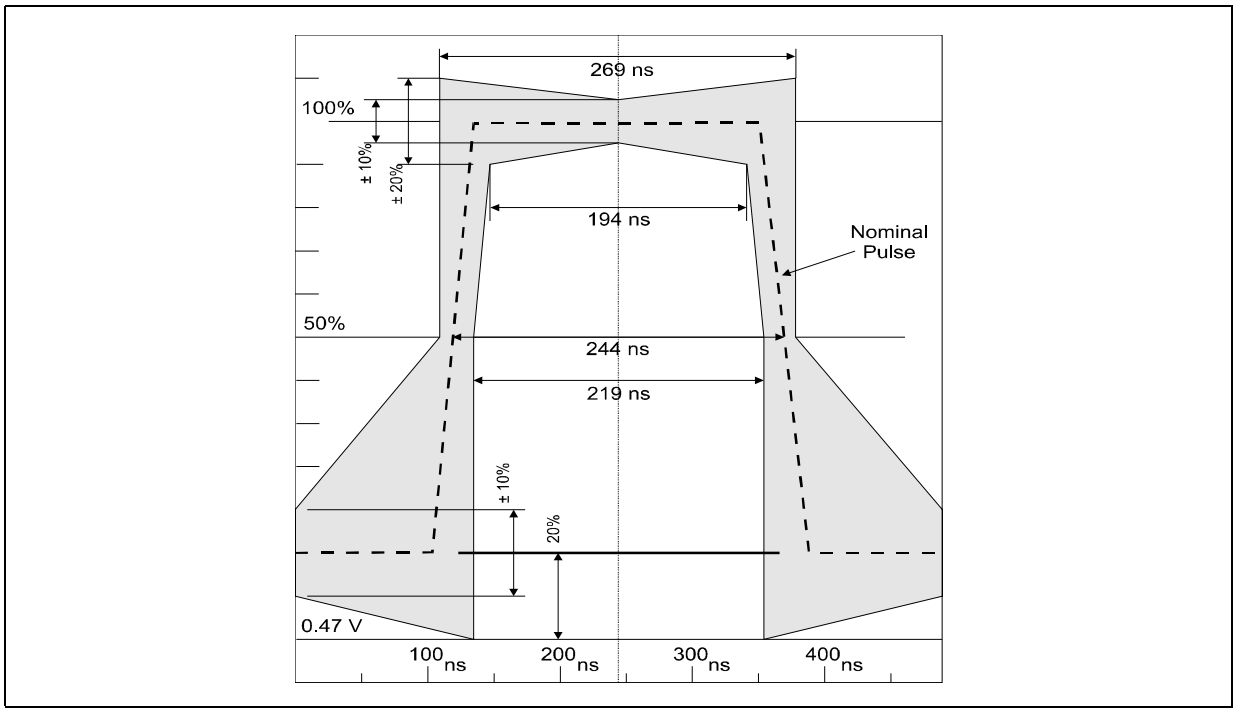


Figure 17. 1.544 MHz Pulse Mask, G.703

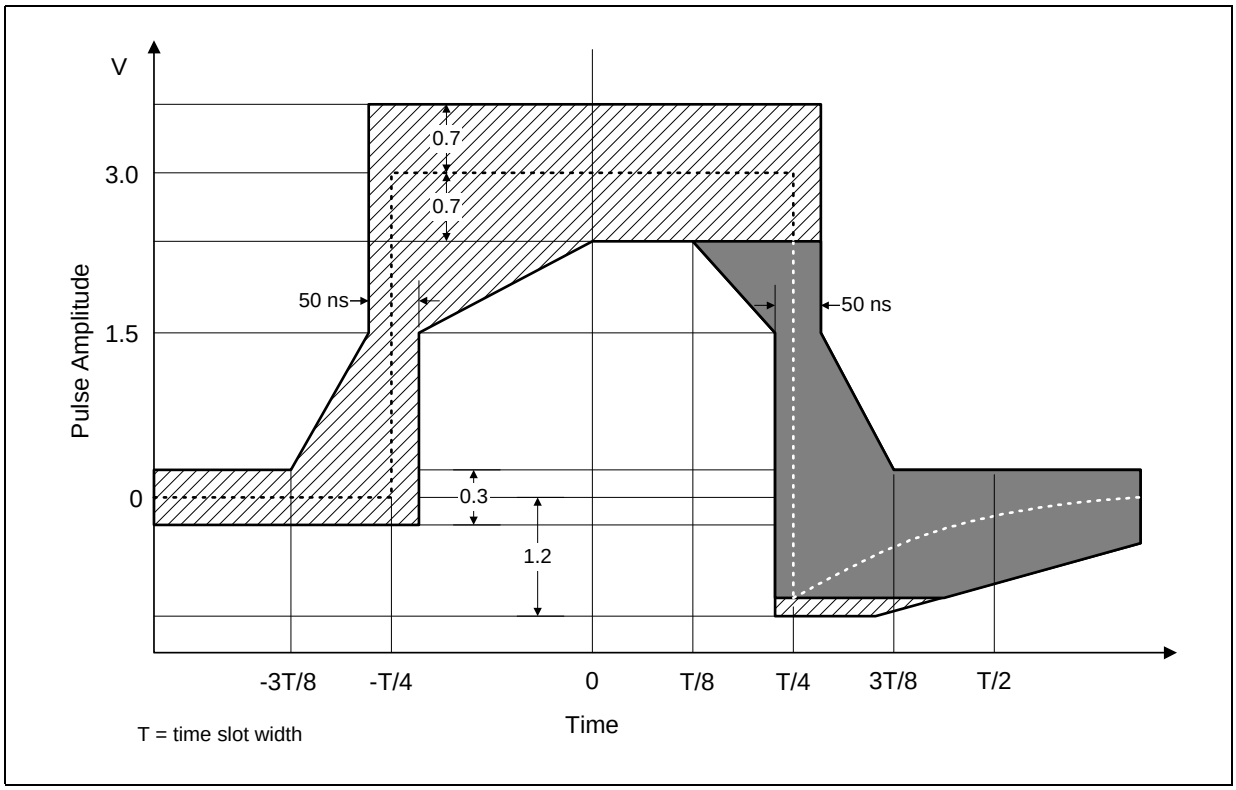


Figure 18. Jitter Tolerance—G.823

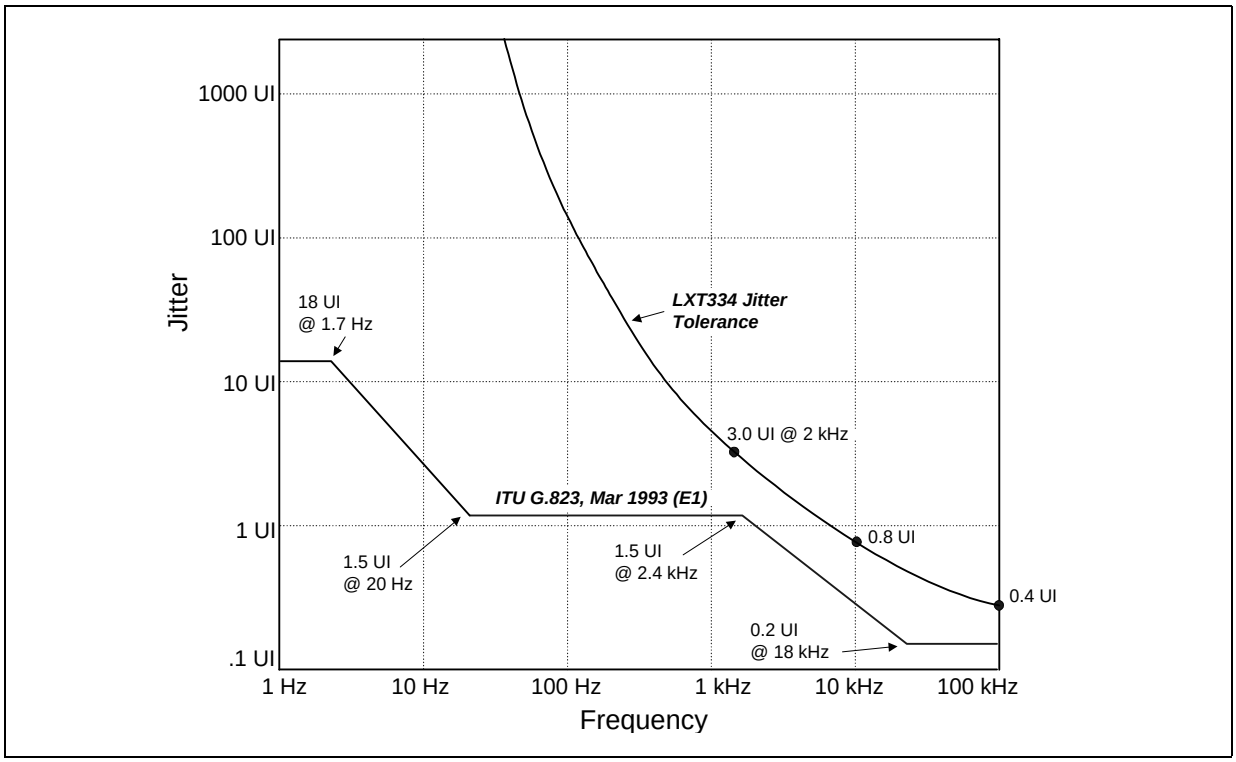


Figure 19. Jitter Attenuation—G.735

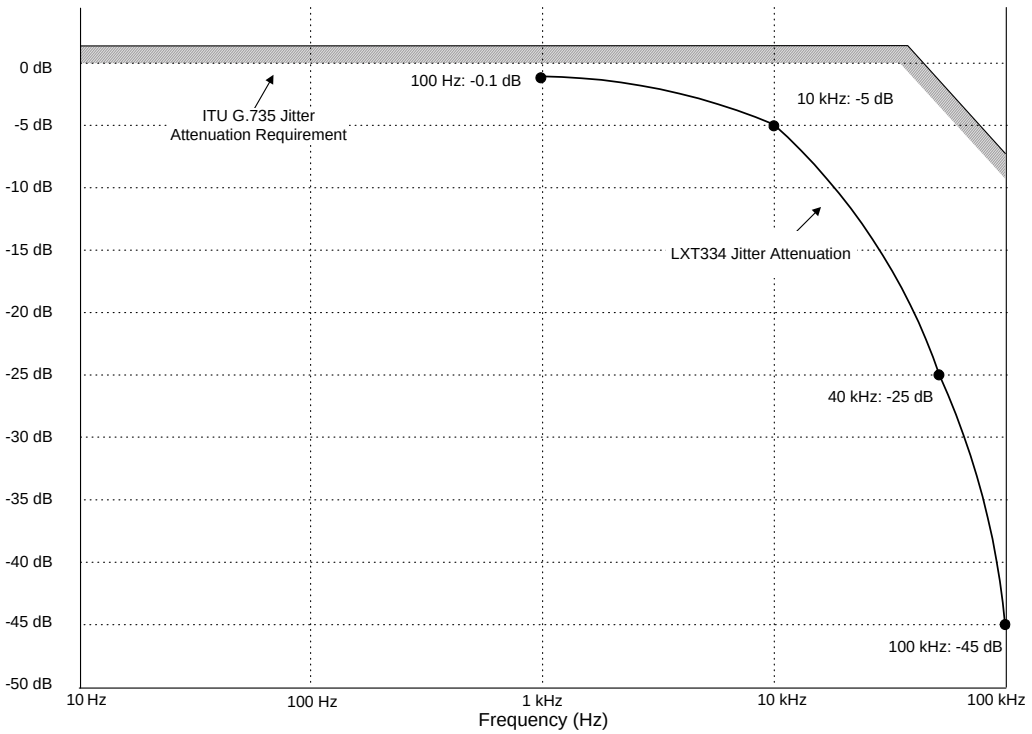


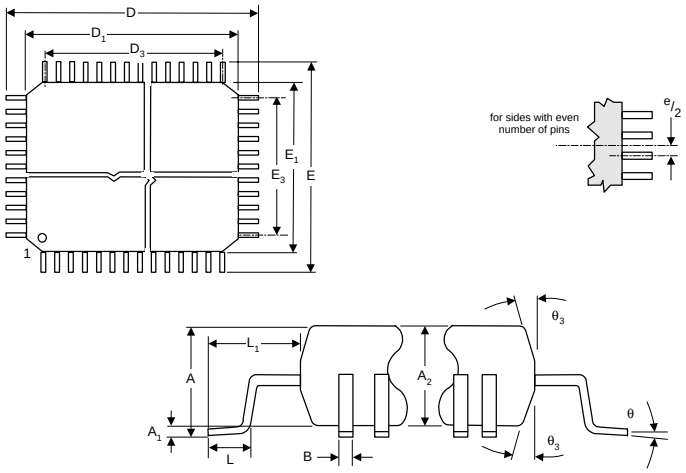
Table 14. Relevant Recommendations

Recommendation	Description
ITU	
G.703	Physical/electrical characteristics of hierarchical digital interfaces
G.704	Functional characteristics of interfaces associated with network nodes
G.735	Characteristics of Primary PCM multiple equipment operating at 2048 kbit/s and offering digital access at 384 kbit/s and/or synchronous digital access at 64 kbit/s
G.736	Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s
G.775	Loss of signal (LOS) and alarm indication (AIS) defect detection and clearance criteria
G.823	The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy
O.151	Specification of instruments to measure error performance in digital systems
I.431	ISDN Primary Rate: user network interface layer 1 specification
ETSI	
ETS 300 166	Transmission and Multiplexing (TM); Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2.048 kbp/s-based plesiochronous or synchronous digital hierarchies

5.0 Mechanical Specifications

Figure 20. Package Specifications

- Part Number: LXT334QE
- 64-pin Quad Flat Pack
- Extended Temperature Range -40°C - +85°C



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.130	–	3.30
A_1	0.000	0.010	0.00	0.25
A_2	0.100	0.120	2.55	3.05
b	0.012	0.018	0.30	0.45
D	0.695	0.715	17.65	18.15
D_1	0.549	0.553	13.95	14.05
D_3	0.472 REF		12.00 REF	
E	0.695	0.715	17.65	18.15
E_1	0.549	0.553	13.95	14.05
E_3	0.472 REF		12.00 REF	
e	0.031 BSC		0.80 BSC	
L	0.029	0.041	0.73	1.03
L_1	0.077 REF		1.95 REF	
q_3	5 °	16 °	5 °	16 °
q	0 °	7 °	0 °	7 °
1. BSC: Basic Spacing Between Centers				