Preliminary Information

Single Intelligent High-Current Self-Protected Silicon High-Side Switch (2.0 mΩ)

The 33982 is a self-protected silicon 2.0 mΩ high-side switch used to replace electromechanical relays, fuses, and discrete devices in power management applications. The 33982 is designed for harsh environments, and it includes self-recovery features. The device is suitable for loads with high inrush current, as well as motors and all types of resistive and inductive loads.

Programming, control, and diagnostics are implemented via the Serial Peripheral Interface (SPI). A dedicated parallel input is available for alternate and pulse width modulation (PWM) control of the output. SPI programmable fault trip thresholds allow the device to be adjusted for optimal performance in the application.

The 33982 is packaged in a power-enhanced 12 x 12 PQFN package with exposed tabs.

Features

- Single 2.0 mΩ Max High-Side Switch with Parallel Input or SPI Control
- 6.0 V to 27 V Operating Voltage with Standby Currents < 5.0 μA
- Output Current Monitoring Output with Two SPI-Selectable Current Ratios
- SPI Control of Overcurrent Limit, Overcurrent Fault Blanking Time, Output-OFF Open Load Detection, Output ON/OFF Control, Watchdog Timeout, Slew Rates, and Fault Status Reporting
- SPI Status Reporting of Overcurrent, Open and Shorted Loads, Overtemperature Shutdown, Undervoltage and Overvoltage Shutdown, Fail-Safe Terminal Status, and Program Status
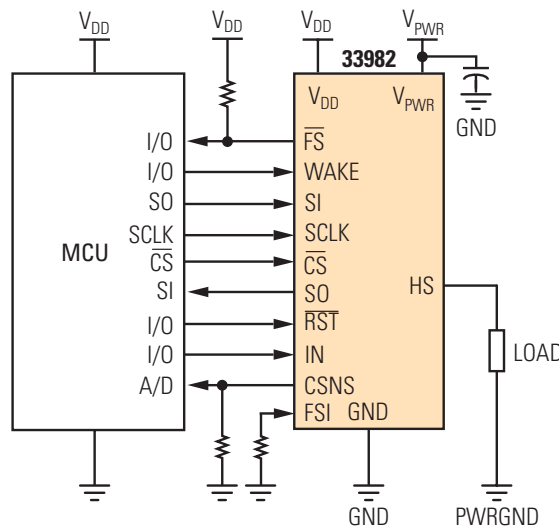- Enhanced 16 V Reverse Polarity V_{PWR} Protection

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33982

**SINGLE HIGH-SIDE SWITCH
2.0 mΩ**

**PNA SUFFIX
CASE 1402-02
16-TERMINAL PQFN**
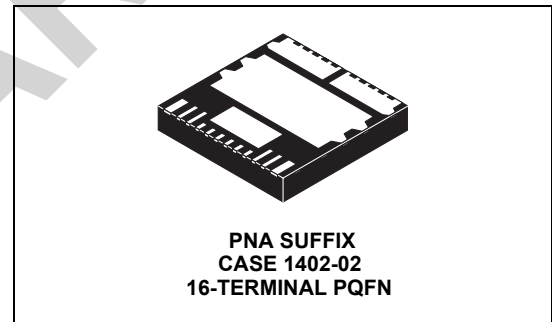
ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33982PNA/R2	-40°C to 125°C	16 PQFN

33982 Simplified Application Diagram

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.
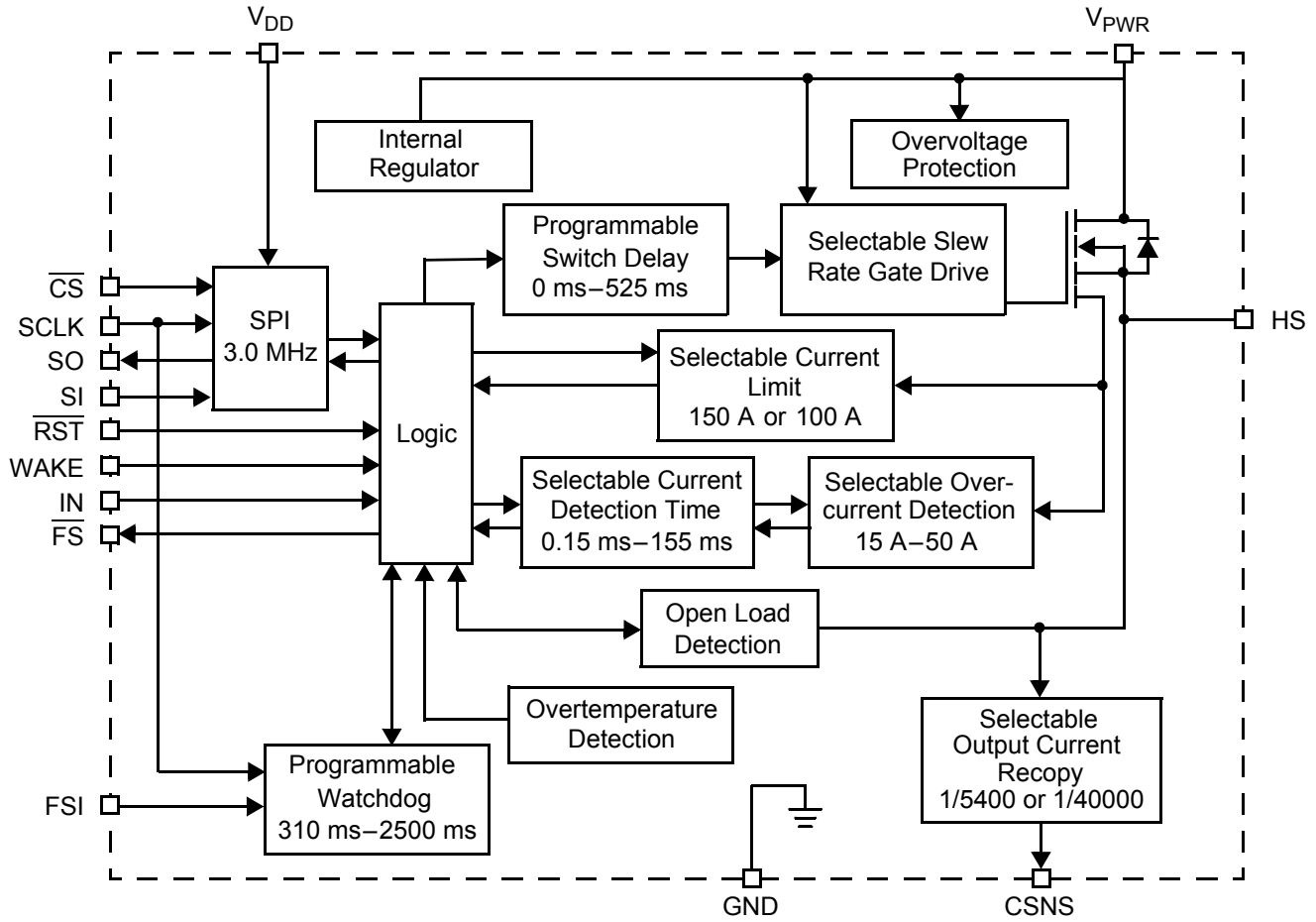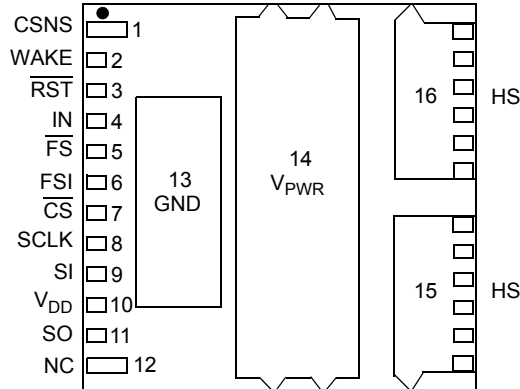
Figure 1. 33982 Simplified Internal Block Diagram

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Transparent Top View of Package

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CSNS  ▢ 1        ┌───────┐  ┌───────┐
WAKE  ▢ 2        │       │  │ ▢     │
RST   ▢ 3        │       │  │ ▢   16│ ▢   HS
IN    ▢ 4        │       │  │ ▢     │
FS    ▢ 5        │   14  │  │ ▢     │
FSI   ▢ 6  │ 13 │  VPWR  │  └───────┘
CS    ▢ 7  │GND │        │  ┌───────┐
SCLK  ▢ 8  │    │        │  │ ▢     │
SI    ▢ 9        │       │  │ ▢   15│ ▢   HS
VDD   ▢ 10       │       │  │ ▢     │
SO    ▢ 11       │       │  │ ▢     │
NC    ▢ 12       └───────┘  └───────┘
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TERMINAL FUNCTION DESCRIPTION

Terminal	Terminal Name	Formal Name	Definition
1	CSNS	Output Current Monitoring	This terminal is used to output a current proportional to the high-side output current and used externally to generate a ground-referenced voltage for the microcontroller to monitor output current.
2	WAKE	Wake	This terminal is used to input a logic [1] signal in order to enable the watchdog timer function. An internal clamp protects this terminal from high damaging voltages when the output is current limited with an external resistor. This input has an internal passive pull-down.
3	$\overline{RST}$	Reset (Active Low)	This input terminal is used to initialize the device configuration and fault registers, as well as place the device in a low current sleep mode. The terminal also starts the watchdog timer when transitioning from logic LOW to logic HIGH. This terminal should not be allowed to be logic HIGH until V_{DD} is in regulation. This terminal has an internal passive pull-down.
4	IN	Serial Input	The Input terminal is used to directly control the output. This input has an internal active pull-down and requires CMOS logic levels. This input may be configured via SPI.
5	$\overline{FS}$	Fault Status (Active Low)	This is an open drain configured output requiring an external pull-up resistor to V_{DD} for fault reporting. When a device fault condition is detected, this terminal is active LOW. Specific device diagnostic faults are reported via the SPI SO terminal.
6	FSI	Fail-Safe Input	The value of the resistance connected between this terminal and ground determines the state of the output after a watchdog timeout occurs. Depending on the resistance value, either the output is OFF or ON. When the FSI terminal is connected to GND, the watchdog circuit and fail-safe operation are disabled. This terminal incorporates an active internal pull-up.
7	$\overline{CS}$	Chip Select (Active Low)	This is an input terminal connected to a chip select output of a master microcontroller (MCU). The MCU determines which device is addressed (selected) to receive data by pulling the $\overline{CS}$ terminal of the selected device logic LOW, enabling SPI communication with the device. Other *unselected* devices on the serial link having their $\overline{CS}$ terminals pulled up logic HIGH disregard the SPI communication data sent.
8	SCLK	Serial Clock	This input terminal is connected to the MCU providing the required bit shift clock for SPI communication. It transitions one time per bit transferred at an operating frequency, f_{SPI}, defined by the communication interface. The 50 percent duty cycle CMOS-level serial clock signal is idle between command transfers. The signal is used to shift data into and out of the device.

TERMINAL FUNCTION DESCRIPTION (continued)

Terminal	Terminal Name	Formal Name	Definition
9	SI	Serial Input	This is a command data input terminal connected to the SPI Serial Data Output of the MCU or to the SO terminal of the previous device in a daisy chain of devices. The input requires CMOS logic level signals and incorporates an internal active pull-down. Device control is facilitated by the input's receiving the MSB first of a serial 8-bit control command. The MCU ensures data is available upon the falling edge of SCLK. The logic state of SI present upon the rising edge of SCLK loads that bit command into the internal command shift register.
10	V_{DD}	Digital Drain Voltage (Power)	This is an external voltage input terminal used to supply power to the SPI circuit. In the event V_{DD} is lost, an internal supply provides power to a portion of the logic, ensuring limited functionality of the device.
11	SO	Serial Output	This is an output terminal connected to the SPI Serial Data Input terminal of the MCU or to the SI terminal of the next device in a daisy chain of devices. This output will remain tri-stated (high impedance OFF condition) so long as the $\overline{CS}$ terminal of the device is logic HIGH. SO is only active when the $\overline{CS}$ terminal of the device is asserted logic LOW. The generated SO output signals are CMOS logic levels. SO output data is available on the falling edge of SCLK and transitions immediately on the rising edge of SCLK.
12	NC	No Connect	This terminal may not be connected.
13	GND	Ground	This terminal is the ground for the logic and analog circuitry of the device.
14	V_{PWR}	Positive Power Supply	This terminal connects to the positive power supply and is the source input of operational power for the device. The V_{PWR} terminal is a backside surface mount tab of the package.
15, 16	HS	High-Side Output	Protected high-side power output to the load. Output terminals must be connected in parallel for operation.

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MAXIMUM RATINGS
All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Operating Voltage Range Steady-State	V_{PWR}	-16 to 41	V
V_{DD} Supply Voltage	V_{DD}	0 to 5.5	V
Input/Output Voltage (Note 1)	V_{IN}, $\overline{RST}$, FSI, CSNS, SI, SCLK, $\overline{CS}$, $\overline{FS}$	-0.3 to 7.0	V
SO Output Voltage (Note 1)	V_{SO}	-0.3 to V_{DD} + 0.3	V
WAKE Input Clamp Current	$I_{CL(WAKE)}$	2.5	mA
CSNS Input Clamp Current	$I_{CL(CSNS)}$	10	mA
Output Current (Note 2)	I_{OUT}	60	A
Output Clamp Energy (Note 3)	E_{CL}	1.5	J
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Junction Temperature	T_J	-40 to 150	°C

Thermal Resistance (Note 4)
    Junction to Case
    Junction to Ambient
	
	$R_{\theta JC}$
	$R_{\theta JA}$
		
		<1.0
		20
			°C/W

ESD Voltage
    Human Body Model (Note 5)
    Machine Model (Note 6)
	
	V_{ESD1}
	V_{ESD2}
		
		±2000
		±200
			V

Terminal Soldering Temperature (Note 7)	T_{SOLDER}	240	°C

Notes
1. Exceeding voltage limits on IN, $\overline{RST}$, FSI, CSNS, SI, SO, SCLK, $\overline{CS}$, or $\overline{FS}$ terminals may cause a malfunction or permanent damage to the device.
2. Continuous high-side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
3. Active clamp energy using single-pulse method (L = 16 mH, R_L = 0, V_{PWR} = 12 V, T_J = 150°C).
4. Device mounted on a 2s2p test board according to JEDEC JESD51-2.
5. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
6. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω) and in accordance with the system module specification with a capacitor > 0.01 μF connected from HS to GND.
7. Terminal soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

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STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 4.5 V $\leq V_{DD} \leq$ 5.5 V, 6.0 V $\leq V_{PWR} \leq$ 27 V, -40°C $\leq T_J \leq$ 150°C unless otherwise noted.
Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Battery Supply Voltage Range Full Operational	V_{PWR}	6.0	–	27	V
V_{PWR} Operating Supply Current Output ON, I_{OUT} = 0 A	$I_{PWR(ON)}$	–	–	20	mA

V_{PWR} Supply Current
    Output OFF, Open Load Detection Disabled, WAKE > 0.7 V_{DD},
    $\overline{RST}$ = $V_{LOGIC\ HIGH}$
	$I_{PWR(SBY)}$	–	–	5.0	mA

Sleep State Supply Current (V_{PWR} < 14 V, $\overline{RST}$ < 0.5 V, WAKE < 0.5 V)
    T_J = 25°C
    T_J = 85°C
	$I_{PWR(SLEEP)}$	–
		–
			–
			–
				10
				50
					μA

V_{DD} Supply Voltage	$V_{DD(ON)}$	4.5	5.0	5.5	V

V_{DD} Supply Current
    No SPI Communication
    3.0 MHz SPI Communication
	$I_{DD(ON)}$	–
		–
			–
			–
				1.0
				5.0
					mA

V_{DD} Sleep State Current	$I_{DD(SLEEP)}$	–	–	5.0	μA
Overvoltage Shutdown	$V_{PWR(ON)}$	28	32	36	V
Overvoltage Shutdown Hysteresis	$V_{PWR(OVHYS)}$	0.2	0.8	1.5	V
Undervoltage Output Shutdown (Note 8)	$V_{PWR(UV)}$	5.0	5.5	6.0	V
Undervoltage Hysteresis (Note 9)	$V_{PWR(UVHYS)}$	–	0.25	–	V
Undervoltage Power-ON Reset	$V_{PWR(UVPOR)}$	–	–	5.0	V

Notes
8. Output will automatically recover to instructed state when V_{PWR} voltage is restored to normal so long as the V_{PWR} degradation level did not go below the undervoltage power-ON reset threshold. This applies to all internal device logic that is supplied by V_{PWR} and assumes that the external V_{DD} supply is within specification.
9. This applies when the undervoltage fault is not latched (IN = 0).

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V $\leq V_{DD} \leq$ 5.5 V, 6.0 V $\leq V_{PWR} \leq$ 27 V, -40°C $\leq T_J \leq$ 150°C unless otherwise noted.
Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT					
Output Drain-to-Source ON Resistance (I_{OUT} = 30 A, T_J = 25°C)	$R_{DS(ON)25}$				mΩ
$\quad V_{PWR}$ = 6.0 V		–	–	3.0	
$\quad V_{PWR}$ = 10 V		–	–	2.0	
$\quad V_{PWRR}$ = 13 V		–	–	2.0	
Output Drain-to-Source ON Resistance (I_{OUT} = 30 A, T_J = 150°C)	$R_{DS(ON)150}$				mΩ
$\quad V_{PWR}$ = 6.0 V		–	–	5.1	
$\quad V_{PWR}$ = 10 V		–	–	3.4	
$\quad V_{PWR}$ = 13 V		–	–	3.4	
Output Source-to-Drain ON Resistance (I_{OUT} = 30 A, T_J = 25°C) (Note 10)	$R_{DS(ON)}$				mΩ
$\quad V_{PWR}$ = -12 V		–	2.0	4.0	
Output Overcurrent High Detection Levels (9.0 V $\leq V_{PWR} \leq$ 16 V)					A
$\quad$ SOCH = 0	I_{OCH0}	120	150	180	
$\quad$ SOCH = 1	I_{OCH1}	80	100	120	
Overcurrent Low Detection Levels (SOCL[2:0])					A
$\quad$ 000	I_{OCL0}	41	50	59	
$\quad$ 001	I_{OCL1}	36	45	54	
$\quad$ 010	I_{OCL2}	32	40	48	
$\quad$ 011	I_{OCL3}	29	35	41	
$\quad$ 100	I_{OCL4}	25	30	35	
$\quad$ 101	I_{OCL5}	20	25	30	
$\quad$ 110	I_{OCL6}	16	20	24	
$\quad$ 111	I_{OCL7}	12	15	18	
Current Sense Ratio (9.0 V $\leq V_{PWR} \leq$ 16 V, CSNS $\leq$ 4.5 V)					
$\quad$ DICR D2 = 0	C_{SR0}	–	1/5400	–	
$\quad$ DICR D2 = 1	C_{SR1}	–	1/40000	–	
Current Sense Ratio (C_{SR0}) Accuracy	C_{SR0_ACC}				%
Output Current					
$\quad$ 10 A		-20	–	20	
$\quad$ 20 A		-14	–	14	
$\quad$ 25 A		-13	–	13	
$\quad$ 30 A		-12	–	12	
$\quad$ 40 A		-13	–	13	
$\quad$ 50 A		-13	–	13	

Notes
10. Source-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{PWR}.

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STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, 6.0 V $\leq$ V$_{PWR}$ $\leq$ 27 V, -40°C $\leq$ T$_J$ $\leq$ 150°C unless otherwise noted.

Typical values noted reflect the approximate parameter mean at T$_A$ = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (continued)					

Current Sense Ratio (C$_{SR1}$) Accuracy
Output Current
  10 A
  20 A
  25 A
  30 A
  40 A
  50 A
	C$_{SR1\_ACC}$	
		
		-25
		-19
		-18
		-17
		-18
		-18
			
			–
			–
			–
			–
			–
			–
				
				25
				19
				18
				17
				18
				18
					%

Maximum Current Sense Clamp Voltage I$_{CSNS}$ = 15 mA	V$_{CL(MAXCSNS)}$	4.5	6.0	7.0	V
Open Load Detection Current (Note 11)	I$_{OLDC}$	30	–	100	µA
Output Fault Detection Threshold Output Programmed OFF	V$_{OLD(THRES)}$	2.0	3.0	4.0	V
Output Negative Clamp Voltage 0.5 A $\leq$ = I$_{OUT}$ $\leq$ = 2.0 A, Output OFF	V$_{CL}$	-20	–	–	V
Overtemperature Shutdown (Note 12) T$_A$ = 125°C, Output OFF	T$_{SD}$	160	175	190	°C
Overtemperature Shutdown Hysteresis (Note 12)	T$_{SD(HYS)}$	5.0	–	20	°C

Notes

11. Output OFF Open Load Detection Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded OFF.
12. Guaranteed by process monitoring. Not production tested.

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STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, 6.0 V $\leq$ V$_{PWR}$ $\leq$ 27 V, -40°C $\leq$ T$_J$ $\leq$ 150°C unless otherwise noted.
Typical values noted reflect the approximate parameter mean at T$_A$ = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL INTERFACE					
Input Logic High Voltage (Note 13)	V$_{IH}$	0.7V$_{DD}$	–	–	V
Input Logic Low Voltage (Note 13)	V$_{IL}$	–	–	0.2V$_{DD}$	V
Input Logic Voltage Hysteresis (Note 14)	V$_{IN(HYS)}$	100	350	750	mV
Input Logic Pull-Down Current (SCLK, IN, SI)	I$_{DWN}$	5.0	–	20	μA
$\overline{RST}$ Input Voltage Range	V$_{RST}$	4.5	5.0	5.5	V
SO, $\overline{FS}$ Tri-State Capacitance (Note 15)	C$_{SO}$	–	–	20	pF
Input Logic Pull-Down Resistor ($\overline{RST}$) and WAKE	I$_{DWN}$	100	200	400	kΩ
Input Capacitance (Note 15)	C$_{IN}$	–	4.0	12	pF
WAKE Input Clamp Voltage (Note 16) I$_{CL(WAKE)}$ < 2.5 mA	V$_{CL(WAKE)}$	7.0	–	14	V
WAKE Input Forward Voltage I$_{CL(WAKE)}$ = -2.5 mA	V$_{F(WAKE)}$	-2.0	–	-0.3	V
SO High-State Output Voltage I$_{OH}$ = 1.0 mA	V$_{SOH}$	0.8V$_{DD}$	–	–	V
$\overline{FS}$, SO Low-State Output Voltage I$_{OL}$ = -1.6 mA	V$_{SOL}$	–	0.2	0.4	V
SO Tri-State Leakage Current $\overline{CS}$ $\geq$ 0.7 V$_{DD}$	I$_{SO(LEAK)}$	-5.0	0	5.0	μA
Input Logic Pull-Up Current (Note 17) $\overline{CS}$, V$_{IN}$ > 0.7V$_{DD}$	I$_{UP}$	5.0	–	20	μA
FSI Input Pin External Pull-Down Resistance	RFS				kΩ
FSI Disabled, HS Indeterminate	RFSdis	–	0	1.0	
FSI Enabled, HS OFF	RFSoff	6.0	10	14	
FSI Enabled, HS ON	RFSon	30	–	–	

Notes
13. Upper and lower logic threshold voltage range applies to SI, $\overline{CS}$, SCLK, $\overline{RST}$, IN, and WAKE input signals. The WAKE and $\overline{RST}$ signals may be supplied by a derived voltage reference to V$_{PWR}$.
14. Parameter is guaranteed by process monitoring but is not production tested.
15. Input capacitance of SI, $\overline{CS}$, SCLK, $\overline{RST}$, and WAKE. This parameter is guaranteed by process monitoring but is not production tested.
16. The current must be limited by a series resistance when using voltages > 7.0 V.
17. Pull-up current is with $\overline{CS}$ OPEN. $\overline{CS}$ has an active internal pull-up to V$_{DD}$.

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DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 4.5 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, 6.0 V $\leq$ V$_{PWR}$ $\leq$ 27 V, -40°C $\leq$ T$_J$ $\leq$ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T$_A$ = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING					
Output Rising Slow Slew Rate A (DICR D3 = 0) (Note 18) 9.0 V < V$_{PWR}$ < 16 V	SR$_{RA\_SLOW}$	0.2	0.6	1.2	V/μs
Output Rising Slow Slew Rate B (DICR D3 = 0) (Note 19) 9.0 V < V$_{PWR}$ < 16 V	SR$_{RB\_SLOW}$	0.03	0.1	0.3	V/μs
Output Rising Fast Slew Rate A (DICR D3 = 1) (Note 18) 9.0 V < V$_{PWR}$ < 16 V	SR$_{RA\_FAST}$	0.4	1.0	4.0	V/μs
Output Rising Fast Slew Rate B (DICR D3 = 1) (Note 19) 9.0 V < V$_{PWR}$ < 16 V	SR$_{RB\_FAST}$	0.03	0.1	1.2	V/μs
Output Falling Slow Slew Rate A (DICR D3 = 0) (Note 18) 9.0 V < V$_{PWR}$ < 16 V	SR$_{FA\_SLOW}$	0.2	0.6	1.2	V/μs
Output Falling Slow Slew Rate B (DICR D3 = 0) (Note 19) 9.0 V < V$_{PWR}$ < 16 V	SR$_{FB\_SLOW}$	0.03	0.1	0.3	V/μs
Output Falling Fast Slew Rate A (DICR D3 = 1) (Note 18) 9.0 V < V$_{PWR}$ < 16 V	SR$_{FA\_FAST}$	0.8	2.0	4.0	V/μs
Output Falling Fast Slew Rate B (DICR D3 = 1) (Note 19) 9.0 V < V$_{PWR}$ < 16 V	SR$_{FB\_FAST}$	0.1	0.35	1.2	V/μs

Notes
18. Rise and Fall Slew Rates A measured across a 5.0 Ω resistive load at high-side output = 0.5 V to V$_{PWR}$-3.5 V. These parameters are guaranteed by process monitoring.
19. Rise and Fall Slow Slew Rates B measured across a 5.0 Ω resistive load at high-side output = 0.5 V to V$_{PWR}$-3.5 V. These parameters are guaranteed by process monitoring.

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V $\leq V_{DD} \leq$ 5.5 V, 6.0 V $\leq V_{PWR} \leq$ 27 V, -40°C $\leq T_J \leq$ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING (continued)					
Output Turn-ON Delay Time in Fast/Slow Slew Rate (Note 20) DICR = 0, DICR = 1	$t_{DLY(ON)}$	1.0	18	100	µs
Output Turn-OFF Delay Time in Slow Slew Rate Mode (Note 21) DICR = 0	$t_{DLY\_SLOW(OFF)}$	20	230	500	µs
Output Turn-OFF Delay Time in Fast Slew Rate Mode (Note 21) DICR = 1	$t_{DLY\_FAST(OFF)}$	10	60	200	µs
Direct Input Switching Frequency (DICR D3 = 0)	f_{PWM}	–	300	–	Hz
Overcurrent Detection Blanking Time (OCLT[1:0]) 00 01 10 11	t_{OCL0} t_{OCL1} t_{OCL2} t_{OCL3}	108 7.0 0.8 0.08	155 10 1.2 0.15	202 13 1.6 0.25	ms
Overcurrent High Detection Blanking Time	t_{OCH}	1.0	10	20	µs
$\overline{CS}$ to CSNS Valid Time (Note 22)	CNS_{VAL}	–	–	10	µs
Output Switching Delay Time (OSD[2:0]) 000 001 010 011 100 101 110 111	t_{OSD0} t_{OSD1} t_{OSD2} t_{OSD3} t_{OSD4} t_{OSD5} t_{OSD6} t_{OSD7}	– 52 105 157 210 262 315 367	0 75 150 225 300 375 450 525	– 95 195 293 390 488 585 683	ms
Watchdog Timeout (WD[1:0]) (Note 23) 00 01 10 11	t_{WDTO0} t_{WDTO1} t_{WDTO2} t_{WDTO3}	434 207 1750 875	620 310 2500 1250	806 403 3250 1625	ms

Notes
20. Turn-ON delay time measured from rising edge of any signal (IN, SCLK, $\overline{CS}$) that would turn the output ON to V_{OUT} = 0.5 V with R_L = 5.0 Ω resistive load.
21. Turn-OFF delay time measured from falling edge of any signal (IN, SCLK, $\overline{CS}$) that would turn the output OFF to V_{OUT} = V_{PWR}-0.5 V with R_L = 5.0 Ω resistive load.
22. Time necessary for the CSNS to be within ±5% of the targeted value.
23. Watchdog timeout delay measured from the rising edge of WAKE to $\overline{RST}$ from a sleep state condition to output turn-ON with the output driven OFF and FSI floating. The values shown are for WDR setting of [00]. The accuracy of t_{WDTO} is consistent for all configured watchdog timeouts.

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DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, 6.0 V $\leq$ V$_{PWR}$ $\leq$ 27 V, -40°C $\leq$ T$_J$ $\leq$ 150°C unless otherwise noted.
Typical values noted reflect the approximate parameter mean at T$_A$ = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE CHARACTERISTICS					
Recommended Frequency of SPI Operation	f_{SPI}	–	–	3.0	MHz
Required Low State Duration for $\overline{RST}$ (Note 24)	$t_{W\overline{RST}}$	–	50	167	ns
Rising Edge of $\overline{CS}$ to Falling Edge of $\overline{CS}$ (Required Setup Time) (Note 25)	$t_{\overline{CS}}$	–	–	300	ns
Rising Edge of $\overline{RST}$ to Falling Edge of $\overline{CS}$ (Required Setup Time) (Note 25)	t_{ENBL}	–	–	5.0	μs
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time) (Note 25)	t_{LEAD}	–	50	167	ns
Required High State Duration of SCLK (Required Setup Time) (Note 25)	t_{WSCLKh}	–	–	167	ns
Required Low State Duration of SCLK (Required Setup Time) (Note 25)	t_{WSCLKl}	–	–	167	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time) (Note 25)	t_{LAG}	–	50	167	ns
SI to Falling Edge of SCLK (Required Setup Time) (Note 26)	$t_{SI(SU)}$	–	25	83	ns
Falling Edge of SCLK to SI (Required Setup Time) (Note 26)	$t_{SI(HOLD)}$	–	25	83	ns
SO Rise Time C$_L$ = 200 pF	t_{RSO}	–	25	50	ns
SO Fall Time C$_L$ = 200 pF	t_{FSO}	–	25	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Rise Time (Note 26)	t_{RSI}	–	–	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Fall Time (Note 26)	t_{FSI}	–	–	50	ns
Time from Falling Edge of $\overline{CS}$ to SO Low Impedance (Note 27)	$t_{SO(EN)}$	–	–	145	ns
Time from Rising Edge of $\overline{CS}$ to SO High Impedance (Note 28)	$t_{SO(DIS)}$	–	65	145	ns
Time from Rising Edge of SCLK to SO Data Valid (Note 29) 0.2 V$_{DD}$ $\leq$ SO $\geq$ 0.8 V$_{DD}$, C$_L$ = 200 pF	t_{VALID}	–	65	105	ns

Notes
24. $\overline{RST}$ low duration measured with outputs enabled and going to OFF or disabled condition.
25. Maximum setup time required for the 33982 is the minimum guaranteed time needed from the microcontroller.
26. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
27. Time required for output status data to be available for use at SO. 1.0 kΩ on pull-up on $\overline{CS}$.
28. Time required for output status data to be terminated at SO. 1.0 kΩ on pull-up on $\overline{CS}$.
29. Time required to obtain valid data out from SO following the rise of SCLK.

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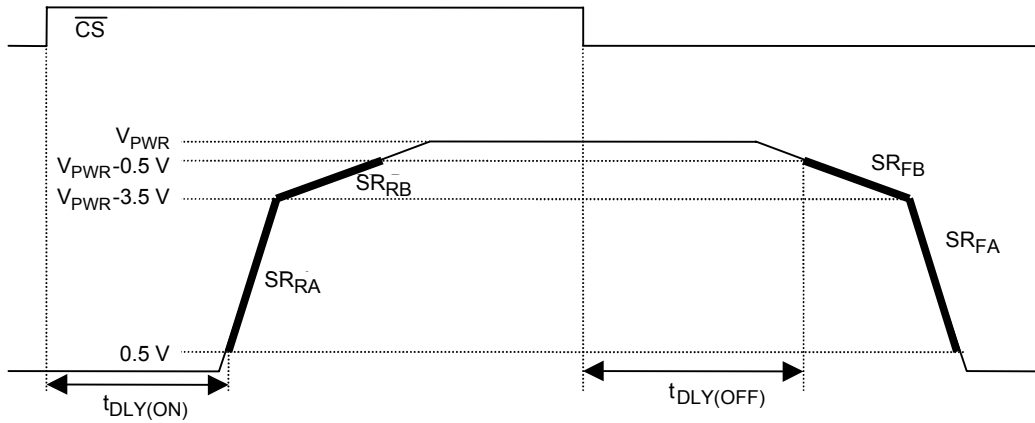
Timing Diagrams

Figure 2. Output Slew Rate and Time Delays
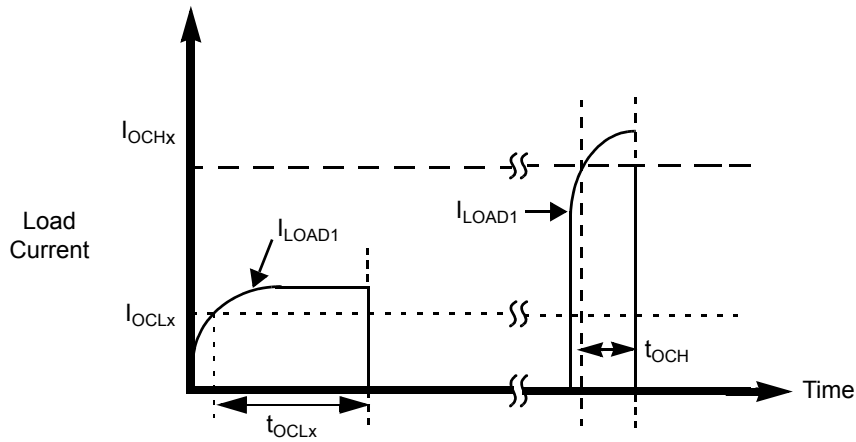
Figure 3. Overcurrent Shutdown
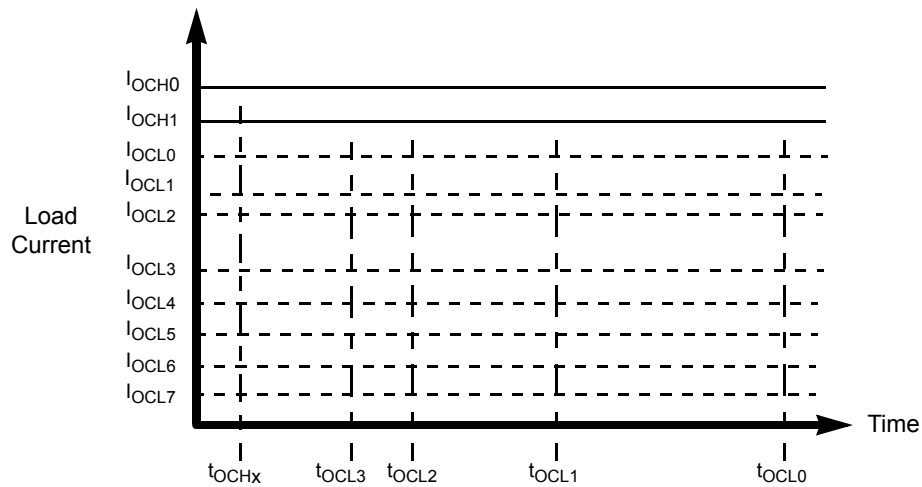
Figure 4. Overcurrent Low and High Detection

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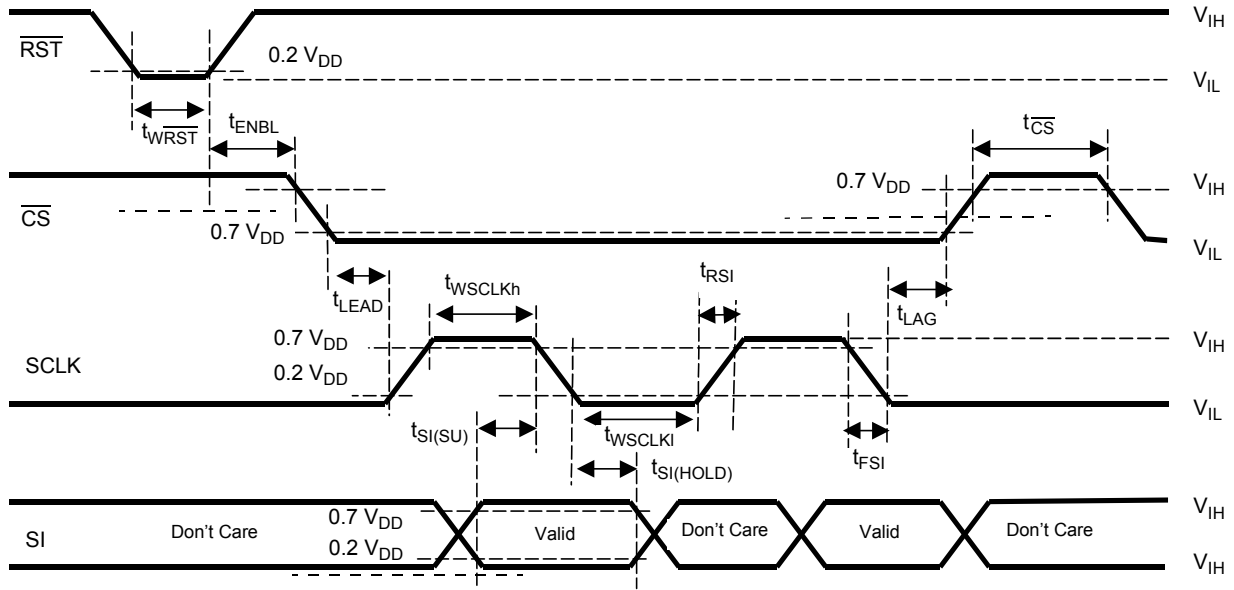

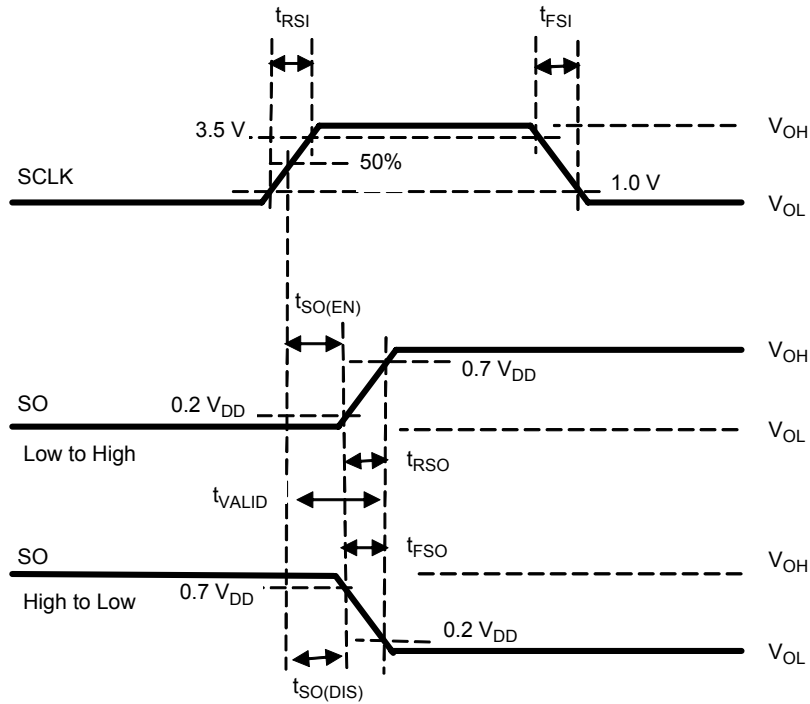**Figure 5. Input Timing Switching Characteristics**

Figure 6. SCLK Waveform and Valid SO Data Delay Time

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 33982 is a self-protected silicon 2.0 mΩ high-side switch used to replace electromechanical relays, fuses, and discrete devices in power management applications. The 33982 is designed for harsh environments, and it includes self-recovery features. The device is suitable for loads with high inrush current, as well as motors and all types of resistive and inductive loads.

Programming, control, and diagnostics are implemented via the Serial Peripheral Interface (SPI). A dedicated parallel input is available for alternate and pulse width modulation (PWM) control of the output. SPI programmable fault trip thresholds allow the device to be adjusted for optimal performance in the application.

The 33982 is packaged in a power-enhanced 12 x 12 PQFN package with exposed tabs.

FUNCTIONAL DESCRIPTION

SPI Protocol Description

The SPI interface has a full duplex, three-wire synchronous data transfer with four I/O lines associated with it: Serial Clock (SCLK), Serial Input (SI), Serial Output (SO), and Chip Select ($\overline{CS}$).

The SI/SO terminals of the 33982 follow a first-in first-out (D7/D0) protocol with both input and output words transferring the most significant bit (MSB) first. All inputs are compatible with 5.0 V CMOS logic levels.

The SPI lines perform the following functions:

Serial Clock (SCLK)

The SCLK terminal clocks the internal shift registers of the 33982 device. The serial input terminal (SI) accepts data into the input shift register on the falling edge of the SCLK signal while the serial output terminal (SO) shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important that the SCLK terminal be in a logic LOW state whenever $\overline{CS}$ makes any transition. For this reason, it is recommended that the SCLK terminal be in a logic [0] state whenever the device is not accessed ($\overline{CS}$ logic [1] state). SCLK has an internal pull-down, I_{DWN}. When $\overline{CS}$ is logic [1], signals at the SCLK and SI terminals are ignored and SO is tri-stated (high impedance). (See Figure 7 and Figure 8 on page 16.)

Serial Interface (SI)

This is a serial interface (SI) command data input terminal. SI instruction is read on the falling edge of SCLK. An 8-bit stream of serial data is required on the SI terminal, starting with D7 to D0. The internal registers of the 33982 are configured and controlled using a 4-bit addressing scheme, as shown in Table 1, page 16. Register addressing and configuration are described in Table 2, page 17. The SI input has an internal pull-down, I_{DWN}.

Serial Output (SO)

The SO terminal is a tri-stateable output from the shift register. The SO terminal remains in a high-impedance state until the $\overline{CS}$ terminal is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, and the state of the key inputs. The SO terminal changes states on the rising edge of SCLK and reads out on the falling edge of SCLK. Fault and input status descriptions are provided in Table 8, page 19.

Chip Select ($\overline{CS}$)

The $\overline{CS}$ terminal enables communication with the master microcontroller (MCU). When this terminal is in a logic [0] state, the device is capable of transferring information to and receiving information from the MCU. The 33982 latches in data from the input shift registers to the addressed registers on the rising edge of $\overline{CS}$. The device transfers status information from the power output to the shift register on the falling edge of $\overline{CS}$. The SO output driver is enabled when $\overline{CS}$ is logic [0]. $\overline{CS}$ should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. $\overline{CS}$ has an internal pull-up, I_{UP}.
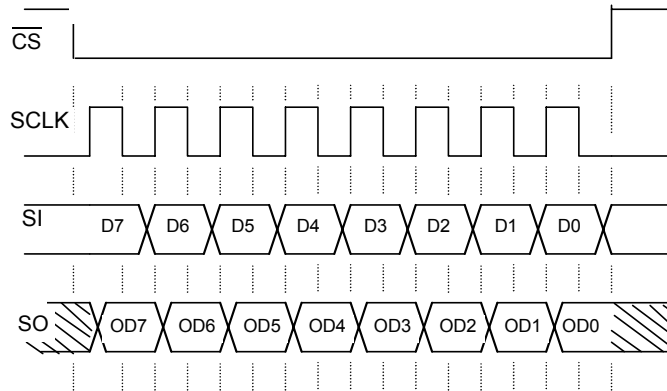
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Notes 1. $\overline{RST}$ is a logic [1] state during the above operation.
2. D7−D0 relate to the most recent ordered entry of data into the device.
3. OD7−OD0 relate to the first 8 bits of ordered fault and status data out of the device.

Figure 7. Single 8-Bit Word SPI Communication
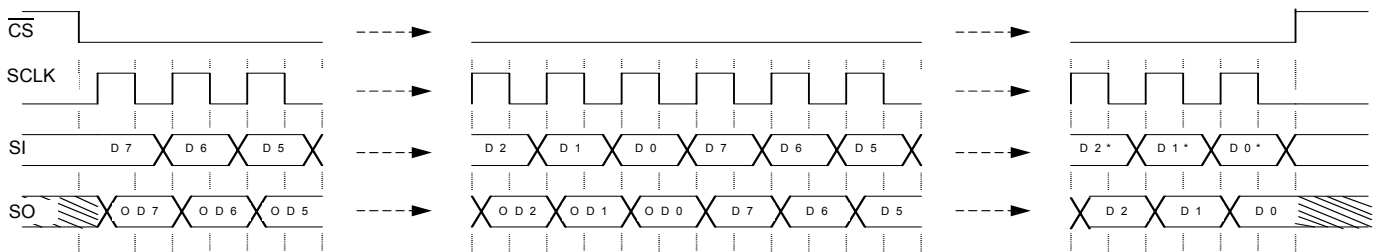
Notes 1. $\overline{RST}$ is a logic [1] state during the above operation.
2. D7−D0 relate to the most recent ordered entry of data into the device.
3. D7*−D0* relate to the previous 8 bits (last command word) of data that was previously shifted into the device.
4. OD7−OD0 relate to the first 8 bits of ordered fault and status data out of the device.

Figure 8. Multiple 8-Bit Word SPI Communication

Serial Input Communication

SPI communication is accomplished using 8-bit messages. A message is transmitted by the MCU starting with the MSB, D7, and ending with the LSB, D0 (Table 1). Each incoming command message on the SI terminal can be interpreted using the following bit assignments: the MSB (D7) is the watchdog bit and in some cases a register address bit; the next three bits, D6−D4, are used to select the command register; and the remaining four bits, D3−D0, are used to configure and control the output and its protection features.

Multiple messages can be transmitted in succession to accommodate those applications where daisy chaining is desirable or to confirm transmitted data as long as the messages are all multiples of eight bits. Any attempt made to latch in a message that is not eight bits will be ignored.

The 33982 has defined registers, which are used to configure the device and to control the state of the output. Table 2, page 17, summarizes the SI registers. The registers are addressed via D6−D4 of the incoming SPI word (Table 1).

Table 1. SI Message Bit Assignment

Bit Sig	SI Msg Bit	Message Bit Description
MSB	D7	Watchdog in: toggled to satisfy watchdog requirements; also used as a register address bit.
	D6−D4	Register address bits.
	D3−D1	Used to configure the inputs, outputs, and the device protection features and SO status content.
LSB	D0	Used to configure the inputs, outputs, and the device protection features and SO status content.

MOTOROLA ANALOG INTEGRATED CIRCUIT DEVICE DATA

Table 2. Serial Input Address and Configuration Bit Map

SI Register	Serial Input Data							
	D7	D6	D5	D4	D3	D2	D1	D0
STATR	x	0	0	0	0	SOA2	SOA1	SOA0
OCR	x	0	0	1	0	0	CSNS $\overline{EN}$	IN_SPI
SOCHLR	x	0	1	0	SOCH	SOCL2	SOCL1	SOCL0
CDTOLR	x	0	1	1	OL dis	CD dis	OCLT1	OCLT0
DICR	x	1	0	0	FAST SR	CSNS high	IN dis	A/O
OSDR	0	1	0	1	0	OSD2	OSD1	OSD0
WDR	1	1	0	1	0	0	WD1	WD0
NAR	0	1	1	0	0	0	0	0
UOVR	1	1	1	0	0	0	UV_dis	OV_dis
TEST	x	1	1	1	Motorola Internal Use (Test)			

x = Don't care.

Device Register Addressing

The following section describes the possible register addresses and their impact on device operation.

Address x000—Status Register (STATR)

The STATR register is used to read the device status and the various configuration register contents without disrupting the device operation or the register contents. The register bits D2, D1, and D0 determine the content of the first eight bits of SO data. In addition to the device status, this feature provides the ability to read the content of the OCR, SOCHLR, CDTOLR, DICR, OSDR, WDR, NAR, and UOVR registers. (Refer to the section entitled Serial Output Communication (Device Status Return Data) beginning on page 18.)

Address x001—Output Control Register (OCR)

The OCR register allows the MCU to control the output through the SPI. Incoming message bit D0 (IN_SPI) reflects the desired states of the high-side output: a logic [1] enables the output switch and a logic [0] turns it OFF. A logic [1] on message bit D1 enables the Current Sense (CSNS) terminal. Bits D2 and D3 must be logic [0]. Bit D7 is used to feed the watchdog if enabled.

Address x010—Select Overcurrent High and Low Register (SOCHLR)

The SOCHLR register allows the MCU to configure the output overcurrent low and high detection levels, respectively. In addition to protecting the device, this slow blow fuse emulation feature can be used to optimize the load requirements to match system characteristics. Bits D2–D0 are used to set the overcurrent low detection level to one of eight possible levels are shown in Table 3. Bit D3 is used to set the overcurrent high detection level to one of two levels as outlined in Table 4.

Table 3. Overcurrent Low Detection Levels

SOCL2 (D2)	SOCL1 (D1)	SOCL0 (D0)	Overcurrent Low Detection (Amperes)
0	0	0	50
0	0	1	45
0	1	0	40
0	1	1	35
1	0	0	30
1	0	1	25
1	1	0	20
1	1	1	15

Table 4. Overcurrent High Detection Levels

SOCH (D3)	Overcurrent High Detection (Amperes)
0	150
1	100

Address x011—Current Detection Time and Open Load Register (CDTOLR)

The CDTOLR register is used by the MCU to determine the amount of time the device will allow an overcurrent low condition before output latches OFF occurs. Bits D1 and D0 allow the MCU to select one of four fault blanking times defined in Table 5. Note that these timeouts apply only to the overcurrent low detection levels. If the selected overcurrent high level is reached, the device will latch off within 20 μs.

Table 5. Overcurrent Low Detection Blanking Time

OCLT[1:0]	Timing
00	155 ms
01	10 ms
10	1.2 ms
11	150 μs

A logic [1] on bit D2 disables the overcurrent low (CD dis) detection timeout feature. A logic [1] on bit D3 disables the open load (OL) detection feature.

Address x100—Direct Input Control Register (DICR)

The DICR register is used by the MCU to enable, disable, or configure the direct IN terminal control of the output. A logic [0] on bit D1 will enable the output for direct control by the IN terminal. A logic [1] on bit D1 will disable the output from direct control. While addressing this register, if the input was enabled for direct control, a logic [1] for the D0 bit will result in a Boolean AND of the IN terminal with its corresponding D0 message bit when addressing the OCR register. Similarly, a logic [0] on the D0 terminal will result in a Boolean OR of the IN terminal with

the corresponding message bits when addressing the OCR register.

The DICR register is useful if there is a need to independently turn on and off several loads that are PWM'd at the same frequency and duty cycle with only one PWM signal. This type of operation can be accomplished by connecting the pertinent direct IN terminals of several devices to a PWM output port from the MCU and configuring each of the outputs to be controlled via their respective direct IN terminal. The DICR is then used to Boolean AND the direct IN(s) of each of the outputs with the dedicated SPI bit that also controls the output. Each configured SPI bit can now be used to enable and disable the common PWM signal from controlling its assigned output.

A logic [1] on bit D2 is used to select the high ratio (C_{SR1}, 1/40000) on the CSNS terminal. The default value [0] is used to select the low ratio (C_{SR0}, 1/5400). A logic [1] on bit D3 is used to select the high-speed slew rate. The default value [0] corresponds to the low speed slew rate.

Address 0101—Output Switching Delay Register (OSDR)

The OSDR register is used to configure the device with a programmable time delay that is active during Output On transitions that are initiated via SPI (not via direct input). Whenever the input is commanded to transition from [0] to [1], the output will be held OFF for the time delay configured in the OSDR register.

The programming of the contents of this register has no effect on device Fail-Safe mode operation. The default value of the OSDR register is 000, equating to no delay, since the switching delay time is 0 ms. This feature allows the user a way to minimize inrush currents, or surges, thereby allowing loads to be synchronously switched ON with a single command.

Table 6 shows the eight selectable output switching delay times, which range from 0 ms to 525 ms.

Table 6. Switching Delay

OSD[2:0] (D2, D1, D0)	Timing (ms)
000	0
001	75
010	150
011	225
100	300
101	375
110	450
111	525

Address 1101—Watchdog Register (WDR)

The WDR register is used by the MCU to configure the watchdog timeout. Watchdog timeout is configured using bits D1 and D0 (Table 7). When bits D1and D0 are programmed for the desired watchdog timeout period, the WD bit (D7) should be

toggled as well to ensure that the new timeout period is programmed at the beginning of a new count sequence.

Table 7. Watchdog Timeout

WD[1:0] (D1, D0)	Timing (ms)
00	620
01	310
10	2500
11	1250

Address 0110—No Action Register (NAR)

The NAR register can be used to no-operation fill SPI data packets in a daisy chain SPI configuration. This allows devices to not be affected by commands being clocked over a daisy-chained SPI configuration, and by toggling the WD bit (D7) the watchdog circuitry will continue to be reset while no programming or data readback functions are being requested from the device.

Address 1110—Undervoltage/Overvoltage Register (UOVR)

The UOVR register can be used to disable or enable the overvoltage and/or undervoltage protection. By default ([0]), both protections are active. When disabled, an undervoltage or overvoltage condition fault will not be reported in bits D1 and D0 of the output fault register.

Address x111—TEST

The TEST register is reserved for test and is not accessible with SPI during normal operation.

Serial Output Communication (Device Status Return Data)

When the $\overline{CS}$ terminal is pulled low, the output status register is loaded. Meanwhile, the data is clocked out MSB- (OD7-) first as the new message data is clocked into the SI terminal. The first eight bits of data clocking out of the SO, and following a $\overline{CS}$ transition, are dependant upon the previously written SPI word.

Any bits clocked out of the SO terminal after the first eight will be representative of the initial message bits clocked into the SI terminal since the $\overline{CS}$ terminal first transitioned to a logic [0]. This feature is useful for daisy chaining devices as well as message verification.

A valid message length is determined following a $\overline{CS}$ transition of [0] to [1]. If there is a valid message length, the data is latched into the appropriate registers. A valid message length is a multiple of eight bits. At this time, the SO terminal is tri-stated and the fault status register is now able to accept new fault status information.

The output status register correctly reflects the status of the STATR-selected register data at the time the $\overline{CS}$ is pulled to a

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logic [0] during SPI communication and/or for the period of time since the last valid SPI communication, with the following exceptions:

- The previous SPI communication was determined to be invalid. In this case, the status will be reported as though the invalid SPI communication never occurred.
- Battery transients below 6.0 V resulting in an undervoltage shutdown of the outputs may result in incorrect data loaded into the status register. The SO data transmitted to the MCU during the first SPI communication following an undervoltage V_{PWR} condition should be ignored.

- The $\overline{RST}$ terminal transition from a logic [0] to [1] while the WAKE terminal is at logic [0] may result in incorrect data loaded into the status register. The SO data transmitted to the MCU during the first SPI communication following this condition should be ignored.

Serial Output Bit Assignment

The eight bits of serial output data depend on the previous serial input message, as explained in the following paragraphs. Table 8 summarizes the SO register content.

Table 8. Serial Output Bit Map Description

Previous STATR D7, D2, D1, D0				Serial Output Returned Data							
SOA3	SOA2	SOA1	SOA0	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
x	0	0	0	WDin	OTF	OCHF	OCLF	OLF	UVF	OVF	FAULT
x	0	0	1	WDin	0	0	1	0	0	CSNS $\overline{EN}$	IN_SPI
x	0	1	0	WDin	0	1	0	SOCH	SOCL2	SOCL1	SOCL0
x	0	1	1	WDin	0	1	1	OL dis	CD dis	OCLT1	OCLT0
x	1	0	0	WDin	1	0	0	Fast SR	CSNS high	IN dis	A/O
0	1	0	1	0	1	0	1	FSM_HS	OSD2	OSD1	OSD0
1	1	0	1	1	1	0	1	0	WDTO	WD1	WD0
0	1	1	0	0	1	1	0	0	IN Terminal	FSI Terminal	WAKE Terminal
1	1	1	0	1	1	1	0	0	0	UV_dis	OV_dis
x	1	1	1	WDin	–	–	–	–	–	–	–

x = Don't care.

Bit OD7 reflects the state of the watchdog bit (D7) addressed during the prior communication. The contents of bits OD[6:0] depend upon the bits D[2:0] from the most recent STATR command SOA[2:0].

Previous Address SOA[2:0]=000

If the previous three MSBs are 000, bits OD6–OD0 reflect the current state of the fault register (FLTR) (Table 9).

Previous Address SOA[2:0]=001

The data in bits OD1 and OD0 contain CSNS $\overline{EN}$ and IN_SPI programmed bits, respectively.

Previous Address SOA[2:0]=010

The data in bit OD3 contain the programmed overcurrent high detection level (refer to Table 4, page 17), and the data in bits OD2, OD1, and OD0 contain the programmed overcurrent low detection levels (refer to Table 3, page 17).

Table 9. Fault Register

OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
x	OTF	OCHF	OCLF	OLF	UVF	OVF	FAULT

OD7 (x) = Don't care.

OD6 (OTF) = Overtemperature Flag.

OD5 (OCHF) = Overcurrent High Flag. (This fault is latched.)

OD4 (OCLF) = Overcurrent Low Flag. (This fault is latched.)

OD3 (OLF) = Open Load Flag.

OD2 (UVF) = Undervoltage Flag. (This fault is latched or not latched.)

OD1 (OVF) = Overvoltage Flag.

OD0 (FAULT) = This flag reports a fault and is reset by a read operation.

Note The $\overline{FS}$ terminal reports a fault and is reset by a new Switch-ON command (via SPI or direct input IN).

Previous Address SOA[2:0]=011

The data returned in bits OD1 and OD0 are current values for the overcurrent fault blanking time, illustrated in Table 5, page 17. Bit OD2 reports when the overcurrent detection timeout feature is active. OD3 reports whether the open load circuitry is active.

Previous Address SOA[2:0]=100

The returned data contain the programmed values in the DICR.

Previous Address SOA[2:0]=101

- SOA3 = 0. The returned data contain the programmed values in the OSDR. Bit OD3 (FSM_HS) reflects the state of the output in the Fail-Safe mode after a watchdog timeout occurs.
- SOA3 = 1. The returned data contain the programmed values in the WDR. Bit OD2 (WDTO) reflects the status of the watchdog circuitry. If WDTO bit is [1], the watchdog has timed out and the device is in Fail-Safe mode. If WDTO is [0], the device is in Normal mode (assuming device is powered and not in the Sleep mode), with the watchdog either enabled or disabled.

Previous Address SOA[2:0]=110

- SOA3 = 0. OD2 to OD0 return the state of the IN, FSI, and WAKE terminals, respectively (Table 10).

Table 10. Terminal Register

OD2	OD1	OD0
IN Terminal	FSI Terminal	WAKE Terminal

- SOA3 = 1. The returned data contains the programmed values in the UOVR register. Bit OD1 reflects the state of the undervoltage protection, while bit OD0 reflects the state of the overvoltage protection (refer to Table 8, page 19).

Previous Address SOA[2:0]=111

Null Data. No previous register Read Back command received, so bits OD2, OD1, and OD0 are null, or 000.

MODES OF OPERATION

The 33982 has four operating modes. They are Sleep, Normal, Fault, and Fail-Safe. Table 11 summarizes details contained in succeeding paragraphs.

Table 11. Fail-Safe Operation and Transitions to Other 33982 Modes

Mode	$\overline{\text{FS}}$	WAKE	$\overline{\text{RST}}$	WDTO	Comments
Sleep	x	0	0	x	Device is in Sleep mode. All outputs are OFF.
Normal	1	x	1	No	Normal mode. Watchdog is active if enabled.
Fault	0	1	x	No	The device is currently in fault mode. The faulted output is OFF.
	0	x	1		
Fail-Safe	1	0	1	Yes	Watchdog has timed out and the device is in Fail-Safe mode. The output is as configured with the RFS resistor connected to FSI. $\overline{\text{RST}}$ and WAKE must be transitioned to logic [0] simultaneously to bring the device out of the Fail-Safe mode or momentarily tied the FSI terminal to ground.
	1	1	1		
	1	0	1		
	1	1	0		

x = Don't care.

Sleep Mode

The default mode of the 33982 is the Sleep mode. This is the state of the device after first applying battery voltage (V_{PWR}), prior to any I/O transitions. This is also the state of the device when the WAKE and $\overline{\text{RST}}$ are both logic [0]. In the Sleep mode, the output and all unused internal circuitry, such as the internal 5.0 V regulator, are off to minimize current draw. In addition, all SPI-configurable features of the device are as if set to logic [0]. The device will transition to the Normal or Fail-Safe operating modes based on the WAKE and $\overline{\text{RST}}$ inputs as defined in Table 11.

Normal Mode

The 33982 is in Normal mode when:

- V_{PWR} is within the normal voltage range.
- $\overline{\text{RST}}$ terminal is logic [1].
- No fault has occurred.

Fail-Safe Mode

Fail-Safe Mode and Watchdog

If the FSI input is not grounded, the watchdog timeout detection is active when either the WAKE or $\overline{\text{RST}}$ input terminal transitions from logic [0] to [1]. The WAKE input is capable of being pulled up to V_{PWR} with a series of limiting resistance that limits the internal clamp current.

The watchdog timeout is a multiple of an internal oscillator and is specified in Table 7, page 18. As long as the WD bit (D7) of an incoming SPI message is toggled within the minimum watchdog timeout period (WDTO), based on the programmed value of the WDR the device will operate normally. If an internal watchdog timeout occurs before the WD bit, the device will revert to a Fail-Safe mode until the device is reinitialized.

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During the Fail-Safe mode, the output will be ON or OFF depending upon the resistor RFS connected to the FSI terminal, regardless of the state of the various direct inputs and modes (Table 12). In this mode, the SPI register content is retained except for overcurrent high and low detection levels and timing, which are reset to their default value (SOCL, SOCH, OCLT). The watchdog, overvoltage, overtemperature, and overcurrent circuitry (with default value for this one) are fully operational.

Table 12. Output State During Fail-Safe Mode

RFS (kΩ)	High-Side State
0	Fail-Safe Mode Disabled
10	HS OFF
30	HS ON

The Fail-Safe mode can be detected by monitoring the WDTO bit D2 of the WDR register. This bit is logic [1] when the device is in Fail-Safe mode. The device can be brought out of the Fail-Safe mode by transitioning the WAKE and $\overline{RST}$ terminals from logic [1] to logic [0] or forcing the FSI terminal to logic [0]. Table 11, page 20, summarizes the various methods for resetting the device from the latched Fail-Safe mode.

If the FSI terminal is tied to GND, the Watchdog fail-safe operation is disabled.

Loss of V$_{DD}$

If the external 5.0 V supply is not within specification, or even disconnected, all register content is reset. The output can still be driven by the direct input IN. The 33982 uses the battery input to power the output MOSFET-related current sense circuitry and any other internal logic, providing fail-safe device operation with no V$_{DD}$ supplied. In this state, the watchdog, overvoltage, overtemperature, and overcurrent circuitry are fully operational with default values.

Fault Mode

The 33982 indicates the following faults as they occur by driving the $\overline{FS}$ terminal to [0]:

- Overtemperature fault
- Overvoltage and undervoltage fault
- Open load fault
- Overcurrent fault (high and low)

The $\overline{FS}$ terminal will automatically return to [1] when the fault condition is removed, except for overcurrent and in some cases undervoltage.

Fault information is retained in the fault register and is available (and reset) via the SO terminal during the first valid SPI communication (refer to Table 9, page 19).

Overtemperature Fault (Non-Latching)

The 33982 incorporates overtemperature detection and shutdown circuitry in the output structure. Overtemperature detection is enabled when the output is in the ON state.

For the output, an overtemperature fault (OTF) condition results in the faulted output turning OFF until the temperature falls below the T$_{SD(HYS)}$. This cycle will continue indefinitely until action is taken by the MCU to shut OFF the output, or until the offending load is removed.

When experiencing this fault, the OTF fault bit will be set in the status register and cleared after either a valid SPI read or a power reset of the device.

Overvoltage Fault (Non-Latching)

The 33982 shuts down the output during an overvoltage fault (OVF) condition on the V$_{PWR}$ terminal. The output remains in the OFF state until the overvoltage condition is removed. When experiencing this fault, the OVF fault bit is set in bit OD1 and cleared after either a valid SPI read or a power reset of the device.

The overvoltage protection and diagnostic can be disabled through SPI (bit OV_dis).

Undervoltage Shutdown (Latching or Non-Latching)

The output latches OFF at some battery voltage between 5.0 V and 6.0 V. As long as the V$_{DD}$ level stays within the normal specified range, the internal logic states within the device will be sustained. This ensures that when the battery level then returns above 6.0 V, the device can be returned to the state that it was in prior to the low V$_{PWR}$ excursion. Once the output latches OFF, the outputs must be turned OFF and ON again to re-enable them. In the case IN=0, this fault is non-latched.

The undervoltage protection and diagnostic can be disabled through SPI (bit UV_dis).

Open Load Fault (Non-Latching)

The 33982 incorporates open load detection circuitry on the output. Output open load fault (OLF) is detected and reported as a fault condition when the output is disabled (OFF). The open load fault is detected and latched into the status register after the internal gate voltage is pulled low enough to turn OFF the output. The OLF fault bit is set in the status register. If the open load fault is removed, the status register will be cleared after reading the register.

The open load protection can be disabled through SPI (bit OL_dis).

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Overcurrent Fault (Latching)

The 33982 has eight programmable overcurrent low detection levels (I_{OCL}) and two programmable overcurrent high detection levels (I_{OCH}) for maximum device protection. The two selectable, simultaneously active overcurrent detection levels, defined by I_{OCH} and I_{OCL}, are illustrated in Figure 4, page 13. The eight different overcurrent low detection levels (I_{OCL0}, I_{OCL1}, I_{OCL2}, I_{OCL3}, I_{OCL4}, I_{OCL5}, I_{OCL6}, and I_{OCL7}) are likewise illustrated in Figure 4.

If the load current level ever reaches the selected overcurrent low detection level and the overcurrent condition exceeds the programmed overcurrent time period (t_{OCx}), the device will latch the output OFF.

If at any time the current reaches the selected I_{OCH} level, then the device will immediately latch the fault and turn OFF the output, regardless of the selected t_{OCL} driver.

For both cases, the device output will stay off indefinitely until the device is commanded OFF and then ON again.

Reverse Battery

The output survives the application of reverse voltage as low as -16 V. Under these conditions, the output's gate is enhanced to keep the junction temperature less than 150°C. The ON resistance of the output is fairly similar to that in the Normal mode. No additional passive components are required.

Ground Disconnect Protection

In the event the 33982 ground is disconnected from load ground, the device protects itself and safely turns OFF the output regardless the state of the output at the time of disconnection.

PACKAGE DIMENSIONS

PNA SUFFIX
16-TERMINAL PQFN
NON-LEADED PACKAGE
CASE 1402-02
ISSUE B

PIN 1
INDEX AREA

PIN NUMBER
REF. ONLY

DETAIL G

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
4. COPLANARITY APPLIES TO LEADS AND CORNER LEADS.
5. MINIMUM METAL GAP SHOULD BE 0.25MM.

DETAIL G
VIEW ROTATED 90° CLOCKWISE

C SEATING PLANE

VIEW M-M

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MOTOROLA

For More Information On This Product,
Go to: www.freescale.com

MC33982/D