

MM74HC4020 • MM74HC4040

14-Stage Binary Counter • 12-Stage Binary Counter

General Description

The MM74HC4020, MM74HC4040, are high speed binary ripple carry counters. These counters are implemented utilizing advanced silicon-gate CMOS technology to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The MM74HC4020 is a 14 stage counter and the MM74HC4040 is a 12-stage counter. Both devices are incremented on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input.

These devices are pin equivalent to the CD4020 and CD4040 respectively. All inputs are protected from damage due to static discharge by protection diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μ A maximum
- Low quiescent current: 80 μ A maximum (74HC Series)
- Output drive capability: 10 LS-TTL loads

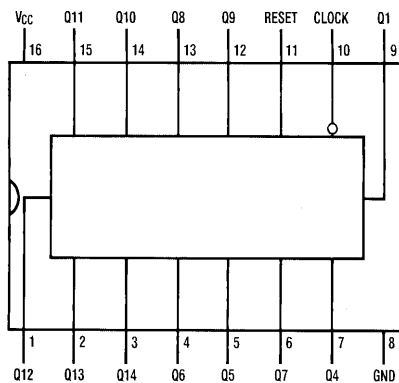
Ordering Code:

Order Number	Package Number	Package Description
MM74HC4020M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4020SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4020MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4020N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HC4040M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4040SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4040MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4040N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

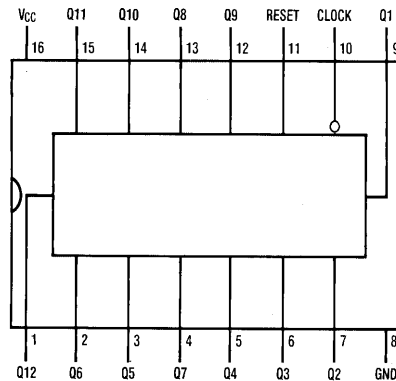
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

Pin Assignments for DIP, SOIC, SOP and TSSOP

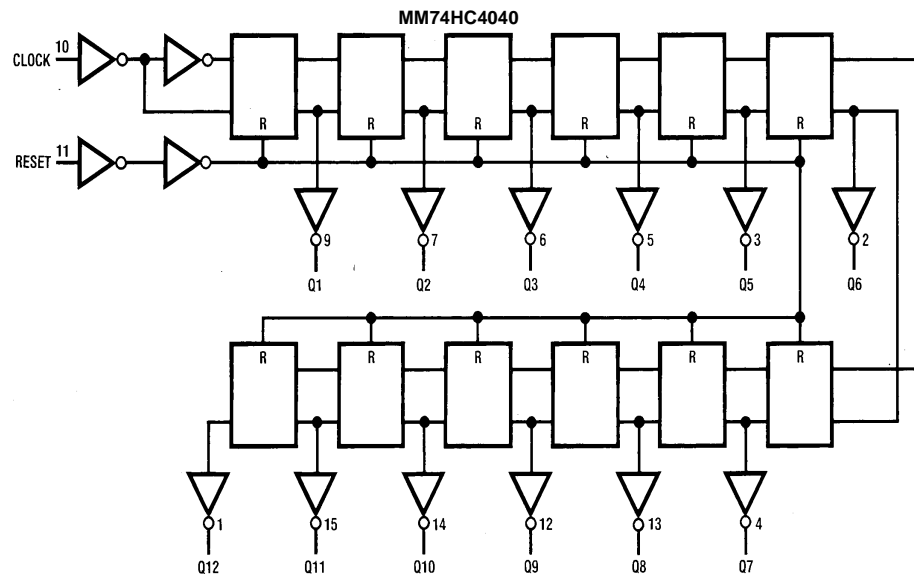
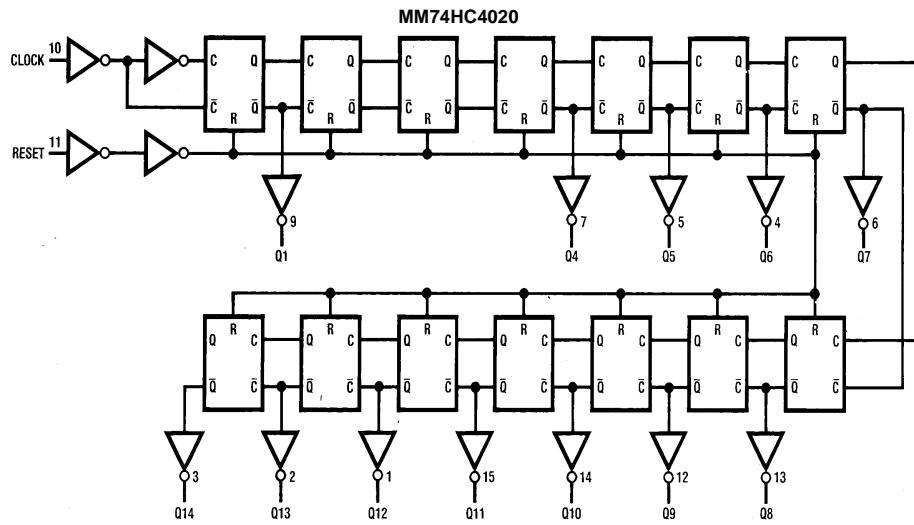


TOP VIEW
MM74HC4020



TOP VIEW
MM74HC4040

Logic Diagrams



AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL} , t_{PLH}	Maximum Propagation Delay Clock to Q	(Note 5)	17	35	ns
t_{PHL}	Maximum Propagation Delay Reset to any Q		16	40	ns
t_{REM}	Minimum Reset Removal Time		10	20	ns
t_W	Minimum Pulse Width		10	16	ns

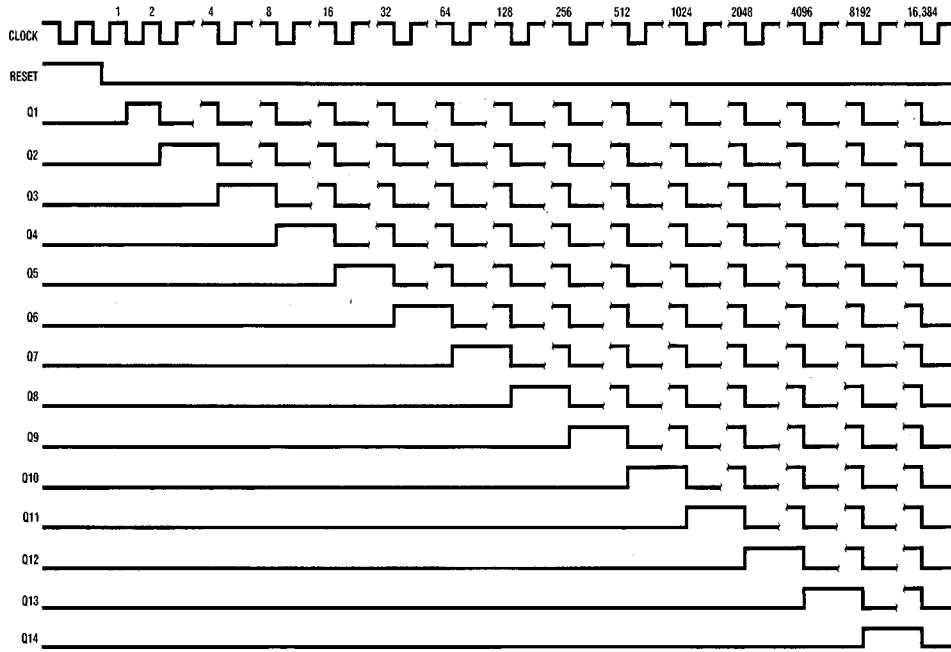
Note 5: Typical Propagation delay time to any output can be calculated using: $t_p = 17 + 12(N-1)$ ns; where N is the number of the output, Q_W , at $V_{CC} = 5V$.

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

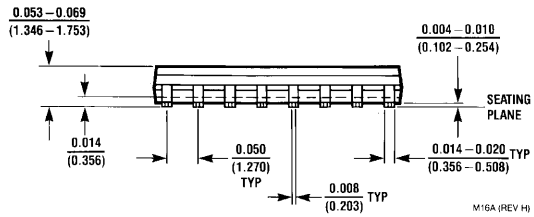
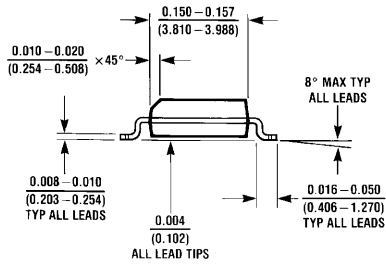
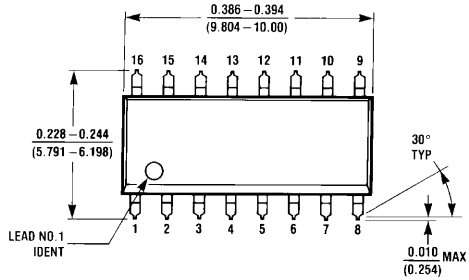
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V	10	6	5	4	MHz
			4.5V	40	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL} , t_{PLH}	Maximum Propagation Delay Clock to Q_1		2.0V	80	210	265	313	ns
			4.5V	21	42	53	63	ns
			6.0V	18	36	45	53	ns
T_{PHL} , t_{PLH}	Maximum Propagation Delay Between Stages from Q_n to Q_{n+1}		2.0V	80	125	156	188	ns
			4.5V	18	25	31	38	ns
			6.0V	15	21	26	31	ns
t_{PHL}	Maximum Propagation Delay Reset to any Q (4020 and 4040)		2.0V	72	240	302	358	ns
			4.5V	24	48	60	72	ns
			6.0V	20	41	51	61	ns
t_{REM}	Minimum Reset Removal Time		2.0V		100	126	149	ns
			4.5V		20	25	50	ns
			6.0V		16	21	25	ns
t_W	Minimum Pulse Width		2.0V		90	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t_{TLH} , t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
t_r , t_f	Maximum Input Rise and Fall Time				1000	1000	1000	ns
					500	500	500	ns
					400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 6)	(per package)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Timing Diagram

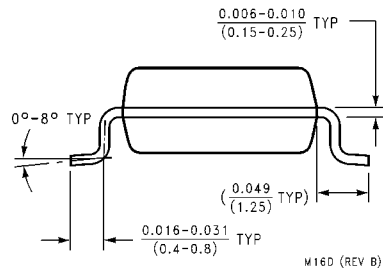
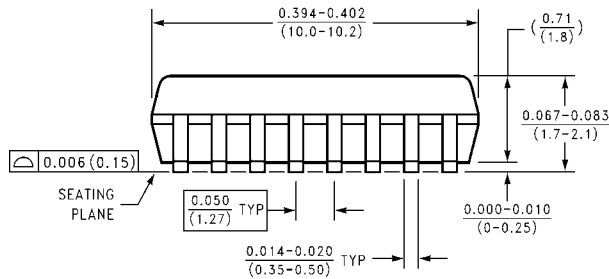
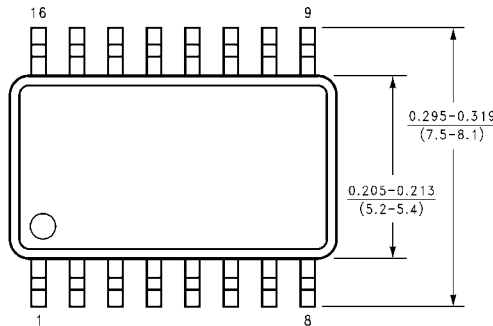


Physical Dimensions inches (millimeters) unless otherwise noted



M16A (REV H)

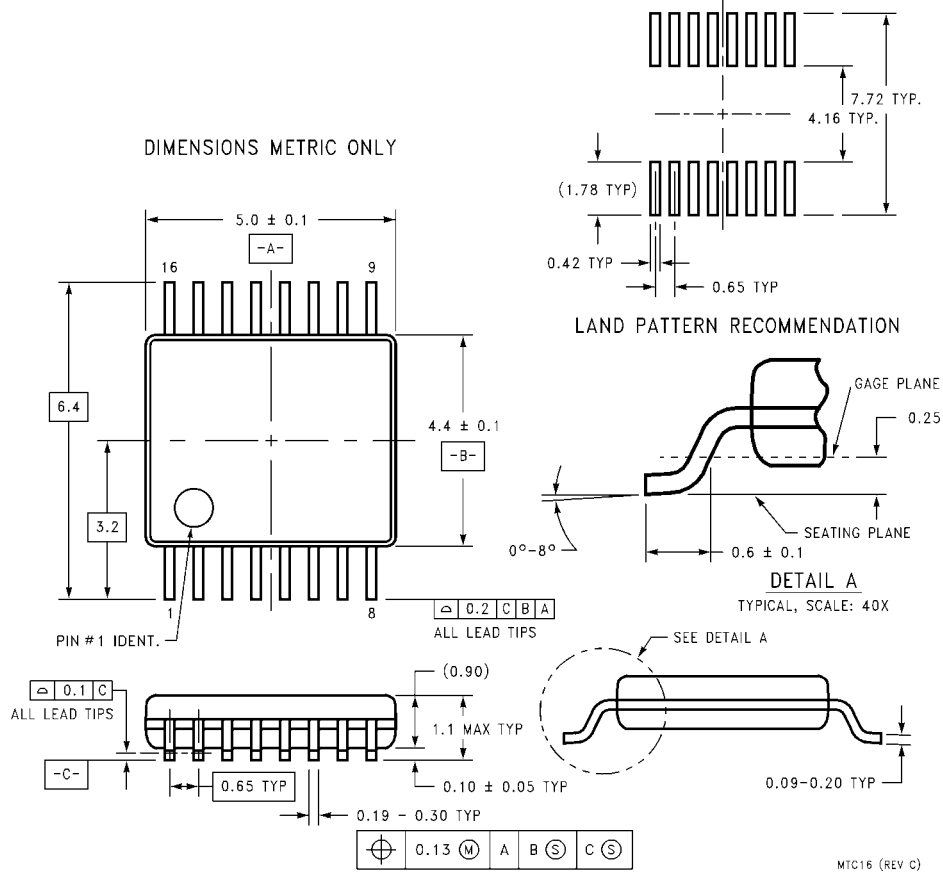
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A



M16D (REV B)

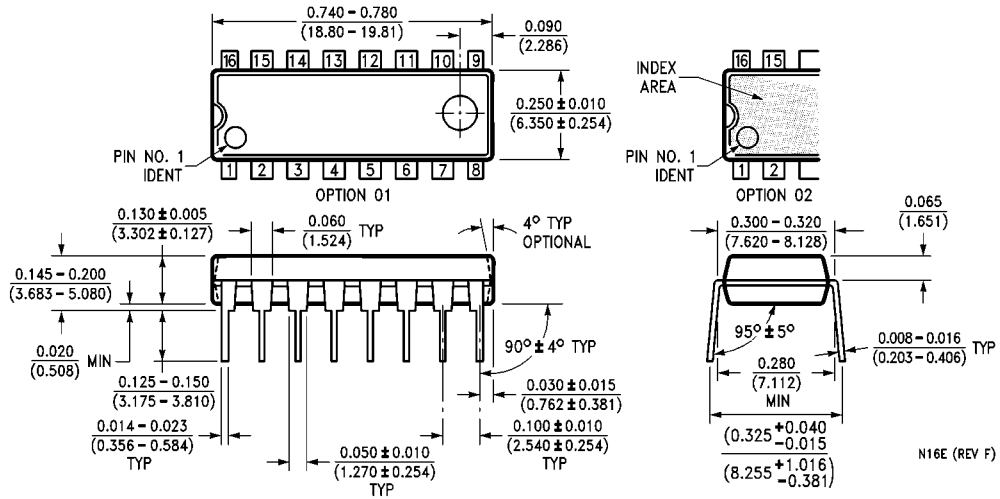
16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

N16E (REV F)

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