

Power Products Division

Advance Information

HIGH AND LOW SIDE DRIVER

The MPIC2113 is a high voltage, high speed, power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

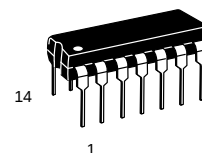
- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout for Both Channels
- Separate Logic Supply
- Operating Supply Range from 5 to 20 V
- Logic and Power Ground Operating Offset Range from -5 to +5 V
- CMOS Schmitt-triggered Inputs with Pull-down
- Cycle by Cycle Edge-triggered Shutdown Logic
- Matched Propagation Delay for Both Channels
- Outputs In Phase with Inputs

PRODUCT SUMMARY

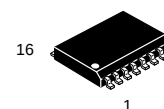
V_{OFFSET}	600 V MAX
$I_{\text{O+/-}}$	2 A/2 A
V_{OUT}	10 – 20 V
$t_{\text{on/off}}$ (typical)	120 & 94 ns
Delay Matching	10 ns

MPIC2113

HIGH AND LOW SIDE DRIVER



P SUFFIX
PLASTIC PACKAGE
CASE 646-06



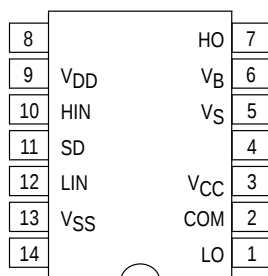
DW SUFFIX
PLASTIC PACKAGE
CASE 751G-02
SOIC – WIDE

ORDERING INFORMATION

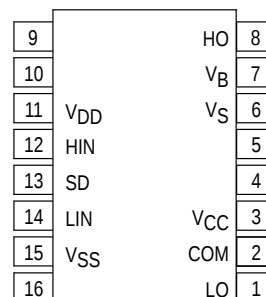
Device	Package
MPIC2113DW	SOIC WIDE
MPIC2113P	PDIP

PIN CONNECTIONS

(TOP VIEW)



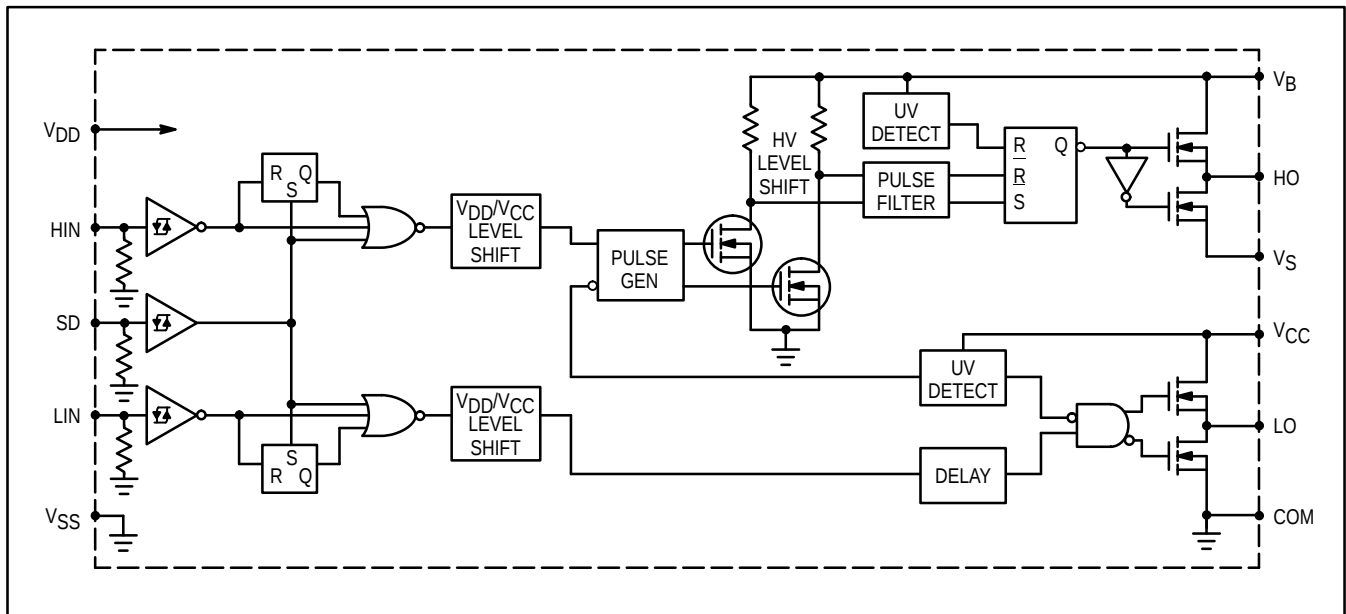
14 LEADS PDIP MPIC2113P



16 LEADS SOIC (WIDE BODY)
MPIC2113DW

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Rating	Symbol	Min	Max	Unit
High Side Floating Absolute Voltage	V_B	-0.3	625	V_{DC}
High Side Floating Supply Offset Voltage	V_S	V_B-25	$V_B+0.3$	
High Side Floating Output Voltage	V_{HO}	$V_S-0.3$	$V_B+0.3$	
Low Side Fixed Supply Voltage	V_{CC}	-0.3	25	
Low Side Output Voltage	V_{LO}	-0.3	$V_{CC}+0.3$	
Logic Supply Voltage	V_{DD}	-0.3	$V_{SS}+25$	
Logic Supply Offset Voltage	V_{SS}	$V_{CC}-25$	$V_{CC}+0.3$	
Logic Input Voltage (HIN, LIN & SD)	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	
Allowable Offset Supply Voltage Transient	dV_S/dt	-	50	V/ns
*Package Power Dissipation @ $T_A \leq +25^\circ\text{C}$	P_D	-	1.6	Watt
	-	-	1.25	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	-	75	$^\circ\text{C/W}$
		-	100	
Operating and Storage Temperature	T_j, T_{stg}	-55	150	$^\circ\text{C}$
Lead Temperature for Soldering Purposes, 10 seconds	T_L	-	260	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15 V differential.

High Side Floating Supply Absolute Voltage	V_B	V_S+10	V_S+20	V
High Side Floating Supply Offset Voltage	V_S	Note 1	600	
High Side Floating Output Voltage	V_{HO}	V_S	V_B	
Low Side Fixed Supply Voltage	V_{CC}	10	20	
Low Side Output Voltage	V_{LO}	0	V_{CC}	
Logic Supply Voltage	V_{DD}	$V_{SS}+5$	$V_{SS}+20$	
Logic Supply Offset Voltage	V_{SS}	-5	5	
Logic Input Voltage (HIN, LIN & SD)	V_{IN}	V_{SS}	V_{DD}	
Ambient Temperature	T_A	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of -5 to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$.

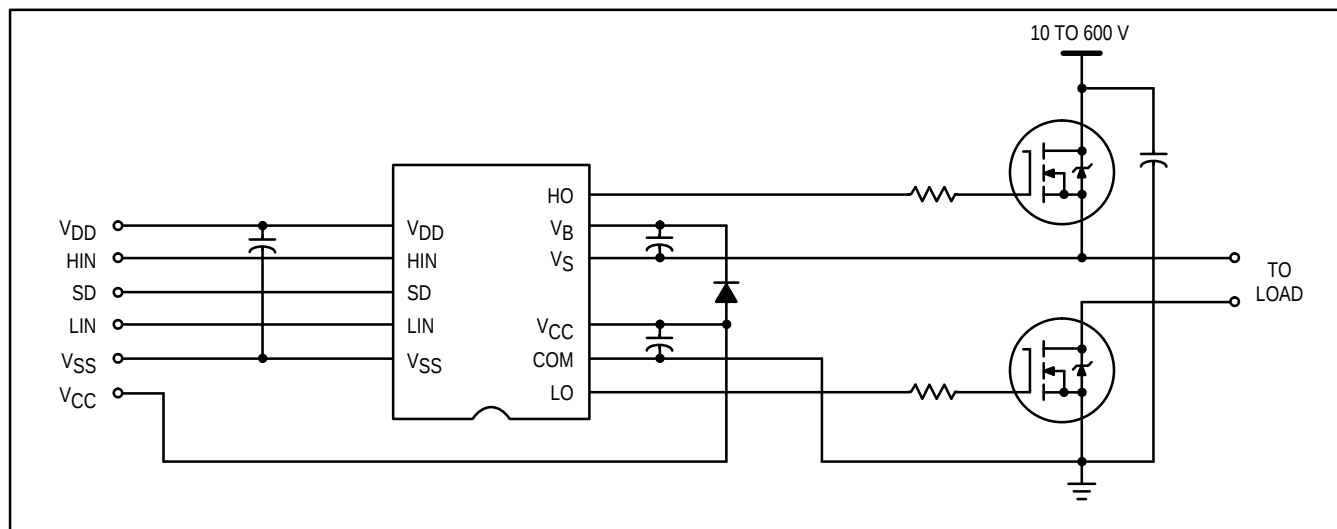
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC ELECTRICAL CHARACTERISTICS – SUPPLY CHARACTERISTICS					
V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15 V and $V_{SS} = \text{COM}$ unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM or V_{SS} and are applicable to the respective output leads: HO or LO.					
Logic "1" Input Voltage	V_{IH}	9.5	–	–	V
Logic "0" Input Voltage	V_{IL}	–	–	6.0	
High Level Output Voltage, $V_{BIAS}-V_O$ @ $V_{IN} = V_{IH}$, $I_O = 0$ A	V_{OH}	–	–	1.2	
Low Level Output Voltage, V_O @ $V_{IN} = V_{IL}$, $I_O = 0$ A	V_{OL}	–	–	0.1	
Offset Supply Leakage Current @ $V_B = V_S = 600$ V	I_{LK}	–	–	50	μA
Quiescent V_{BS} Supply Current @ $V_{IN} = 0$ V or V_{DD}	I_{QBS}	–	125	230	
Quiescent V_{CC} Supply Current @ $V_{IN} = 0$ V or V_{DD}	I_{QCC}	–	180	340	
Quiescent V_{DD} Supply Current @ $V_{IN} = 0$ V or V_{DD}	I_{QDD}	–	15	30	
Logic "1" Input Bias Current @ $V_{IN} = 15$ V	I_{IN+}	–	20	40	V
Logic "0" Input Bias Current @ $V_{IN} = 0$ V	I_{IN-}	–	–	1.0	
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	7.5	–	9.7	
V_{BS} Supply Undervoltage Negative Going Threshold	V_{BSUV-}	7.0	–	9.4	
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	7.4	–	9.6	A
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}	7.0	–	9.4	
Output High Short Circuit Pulsed Current @ $V_{OUT} = 0$ V, $V_{IN} = 15$ V, $PW \leq 10$ μs	I_{O+}	2.0	2.5	–	
Output Low Short Circuit Pulsed Current @ $V_{OUT} = 15$ V, $V_{IN} = 0$ V, $PW \leq 10$ μs	I_{O-}	2.0	2.5	–	

DYNAMIC ELECTRICAL CHARACTERISTICS

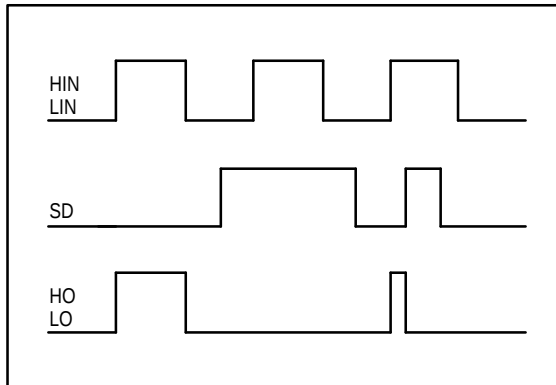
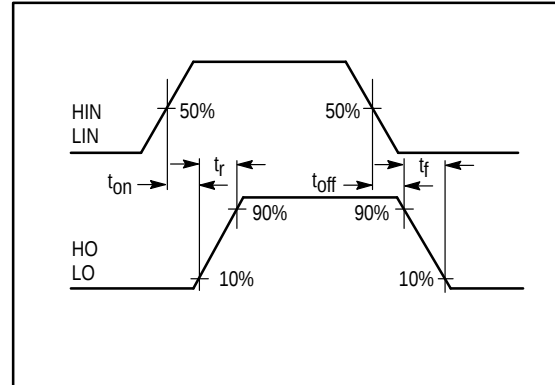
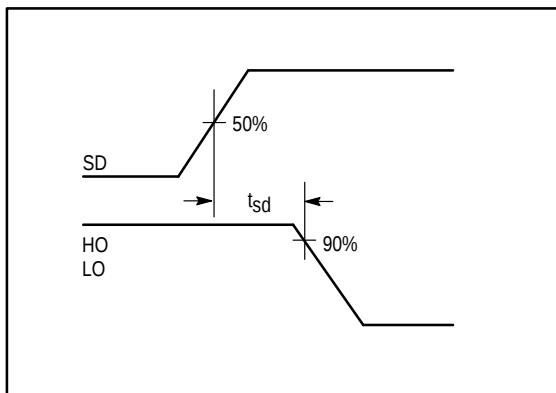
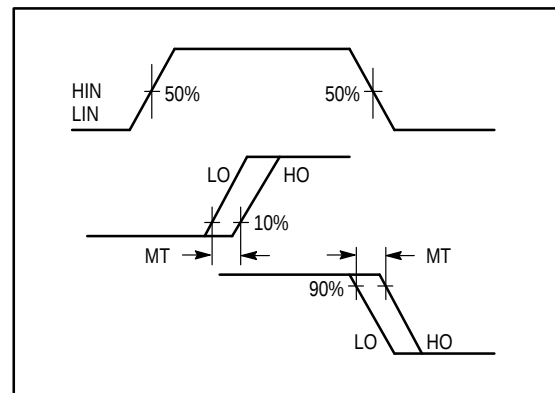
V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15 V and $V_{SS} = \text{COM}$ unless otherwise specified. $T_A = 25^\circ\text{C}$.

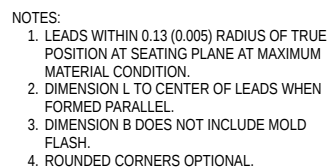
Turn-On Propagation Delay @ $V_S = 0$ V	t_{on}	–	120	150	ns
Turn-Off Propagation Delay @ $V_S = 600$ V	t_{off}	–	94	125	
Shutdown Propagation Delay @ $V_S = 600$ V	t_{sd}	–	110	140	
Turn-On Rise Time @ $C_L = 1000$ pF	t_r	–	25	35	
Turn-Off Fall Time @ $C_L = 1000$ pF	t_f	–	17	25	
Delay Matching, HS & LS Turn-On/Off	MT	–	–	10	

TYPICAL CONNECTION

LEAD DEFINITIONS

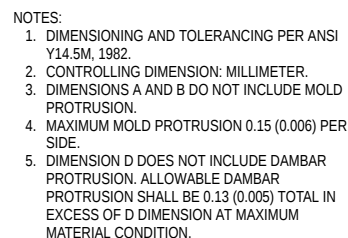
Symbol	Lead Description
V _{DD}	Logic Supply
HIN	Logic Input for High Side Gate Driver Output (HO), In Phase
SD	Logic Input for Shutdown
LIN	Logic Input for Low Side Gate Driver Output (LO), In Phase
V _{SS}	Logic Ground
V _B	High Side Floating Supply
HO	High Side Gate Drive Output
V _S	High Side Floating Supply Return
V _{CC}	Low Side Supply
LO	Low Side Gate Drive Output
COM	Low Side Return


Figure 1. Input / Output Timing Diagram

Figure 2. Switching Time Waveform Definitions

Figure 3. Shutdown Waveform Definitions

Figure 4. Delay Matching Waveform Definitions



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

CASE 646-06
ISSUE L



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

CASE 751G-02
ISSUE A

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