

MSM5117805D

2,097,152-Word × 8-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM5117805D is a 2,097,152-word × 8-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM5117805D achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM5117805D is available in a 28-pin plastic SOJ, 28-pin plastic TSOP.

FEATURES

- 2,097,152-word × 8-bit configuration
- Single 5V power supply, ±10% tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 2048 cycles/32 ms
- Fast page mode, read modify write capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
- Multi-bit test mode capability
- Package options:

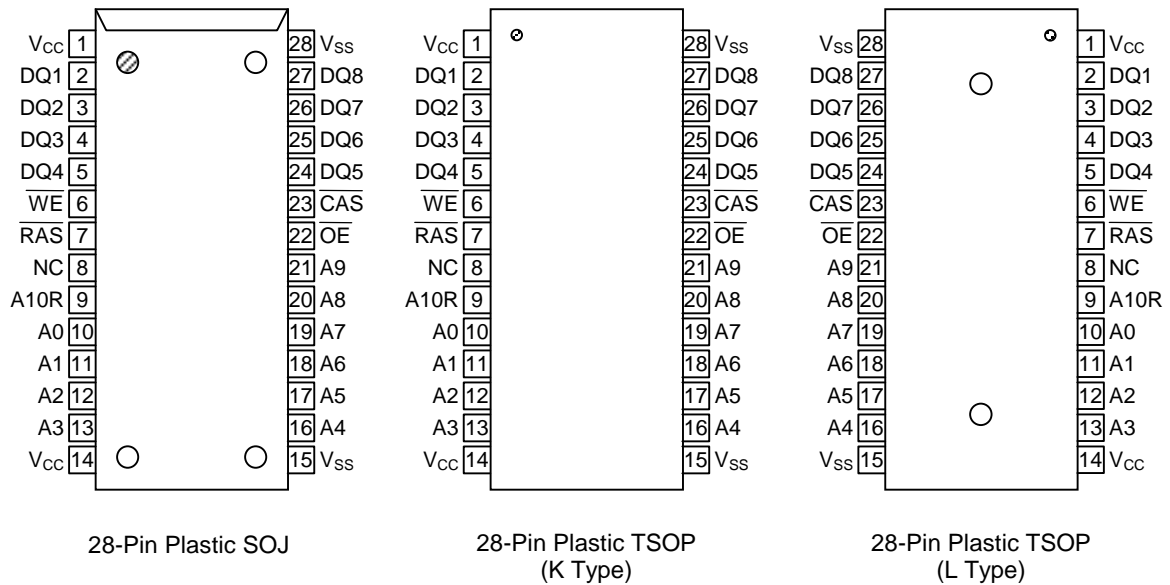
28-pin 400mil plastic SOJ	(SOJ28-P-400-1.27)	(Product : MSM5117805D-xxJS)
28-pin 400mil plastic TSOP	(TSOPII28-P-400-1.27-K)	(Product : MSM5117805D-xxTS-K)
	(TSOPII28-P-400-1.27-L)	(Product : MSM5117805D-xxTS-L)

xx : indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM5117805D-50	50ns	25ns	13ns	13ns	84ns	550mW	5.5mW
MSM5117805D-60	60ns	30ns	15ns	15ns	104ns	495mW	
MSM5117805D-70	70ns	35ns	20ns	20ns	124ns	440mW	

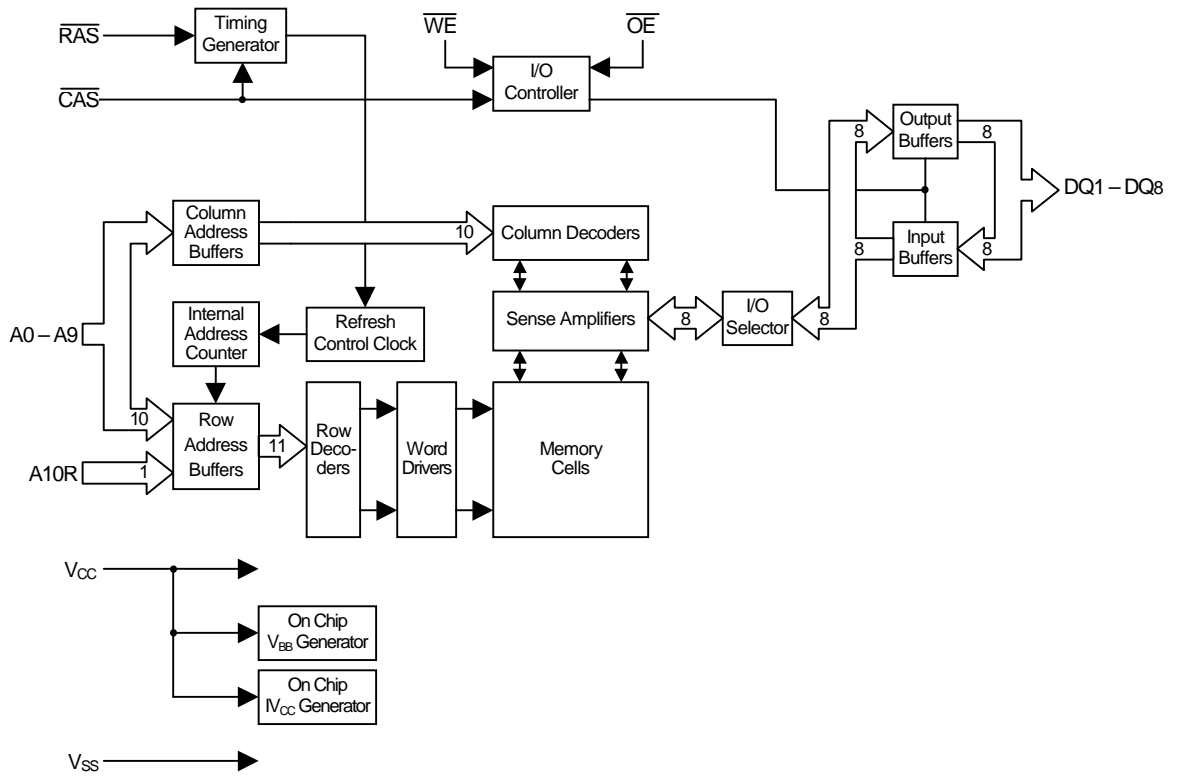
PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0 – A9, A10R	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
DQ1 – DQ8	Data Input/Data Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
V _{CC}	Power Supply (5V)
V _{SS}	Ground (0V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Voltage V_{CC} supply Relative to V_{SS}	V_{CC}	0.5 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D^*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	-55 to 150	°C

*: $T_a = 25^\circ\text{C}$

Recommended Operating Conditions

($T_a = 0^\circ\text{C}$ to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC} + 0.5^{*1}$	V
Input Low Voltage	V_{IL}	-0.5^{*2}	—	0.8	V

Notes: *1. The input voltage is $V_{CC} + 2.0\text{V}$ when the pulse width is less than 20ns (the pulse width is with respect to the point at which V_{CC} is applied).

*2. The input voltage is $V_{SS} - 2.0\text{V}$ when the pulse width is less than 20ns (the pulse width respect to the point at which V_{SS} is applied).

Capacitance

($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 25^\circ\text{C}$, $f=1\text{MHz}$)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 – A9, A10R)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 – DQ8)	$C_{I/O}$	—	7	pF

DC Characteristics

 $(V_{CC} = 5V \pm 10\%, T_a = 0^\circ C \text{ to } 70^\circ C)$

Parameter	Symbol	Condition	MSM5117805 D-50		MSM5117805 D-60		MSM5117805 D-70		Unit	Note
			Min.	Max	Min.	Max	Min.	Max		
Output High Voltage	V_{OH}	$I_{OH} = -5.0mA$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 4.2mA$	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	$0V \leq V_I \leq 6.5V$; All other pins not under test = 0V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	DQ disable $0V \leq V_O \leq V_{CC}$	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	\overline{RAS} , \overline{CAS} cycling, $t_{RC} = \text{Min.}$	—	100	—	90	—	80	mA	1,2
Power Supply Current (Standby)	I_{CC2}	\overline{RAS} , $\overline{CAS} = V_{IH}$	—	2	—	2	—	2	mA	1
		\overline{RAS} , $\overline{CAS} \geq V_{CC} - 0.2V$	—	1	—	1	—	1		
Average Power Supply Current (\overline{RAS} -only Refresh)	I_{CC3}	\overline{RAS} cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = \text{Min.}$	—	100	—	90	—	80	mA	1,2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current (\overline{CAS} before \overline{RAS} Refresh)	I_{CC6}	$\overline{RAS} = \text{cycling}$, \overline{CAS} before \overline{RAS}	—	100	—	90	—	80	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS} = V_{IL}$, \overline{CAS} cycling, $t_{PC} = \text{Min.}$	—	100	—	90	—	80	mA	1,3

- Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
 2. The address can be changed once or less while $\overline{RAS} = V_{IL}$.
 3. The address can be changed once or less while $\overline{CAS} = V_{IH}$.

AC Characteristic (1/2)

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C) Note1,2,3,11,12

Parameter	Symbol	MSM5117805 D-50		MSM5117805 D-60		MSM5117805 D-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	84	—	104	—	124	—	ns	
Read Modify Write Cycle Time	t _{RWC}	110	—	135	—	160	—	ns	
Fast Page Mode Cycle Time	t _{HPC}	20	—	25	—	30	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{HPRWC}	58	—	68	—	78	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	50	—	60	—	70	ns	4,5,6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	13	—	15	—	20	ns	4,5
Access Time from Column Address	t _{AA}	—	25	—	30	—	35	ns	4,6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	30	—	35	—	40	ns	4
Access Time from $\overline{\text{OE}}$	t _{OEA}	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
Data Output Hold After $\overline{\text{CAS}}$ Low	t _{DOH}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{CEZ}	0	13	0	15	0	20	ns	7,8
$\overline{\text{RAS}}$ to Data Output Buffer Turn-off Delay Time	t _{REZ}	0	13	0	15	0	20	ns	7,8
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	13	0	15	0	20	ns	7
$\overline{\text{WE}}$ to Data Output Buffer Turn-off Delay Time	t _{WEZ}	0	13	0	15	0	20	ns	7
Transition Time	t _T	1	50	1	50	1	50	ns	3
Refresh Period	t _{REF}	—	32	—	32	—	32	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	30	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	50	100,000	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	7	—	10	—	13	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	7	—	10	—	13	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	7	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	7	10,000	10	10,000	13	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	35	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	30	—	35	—	40	—	ns	
$\overline{\text{OE}}$ Hold Time from $\overline{\text{CAS}}$ (DQ Disable)	t _{CHO}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	11	37	14	45	14	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	9	25	12	30	12	35	ns	6

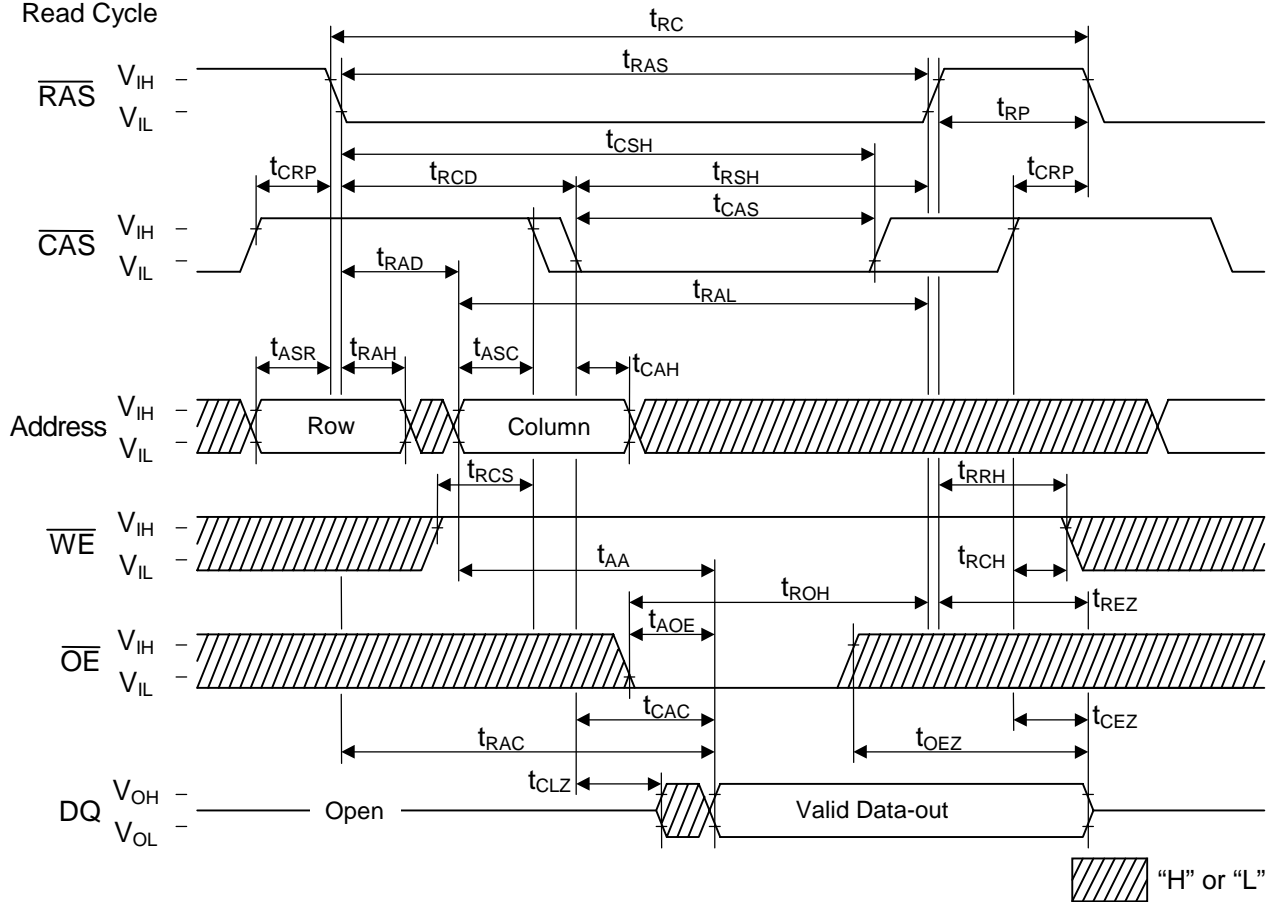
AC Characteristic (2/2) $(V_{CC} = 5V \pm 10\%, T_a = 0^\circ C \text{ to } 70^\circ C)$ Note1,2,3,11,12

Parameter	Symbol	MSM5117805 D-50		MSM5117805 D-60		MSM5117805 D-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	7	—	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	7	—	10	—	13	—	ns	
Column Address to \overline{RAS} Lead Time	t_{RAL}	25	—	30	—	35	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	9
Read Command Hold Time referenced to \overline{RAS}	t_{RRH}	0	—	0	—	0	—	ns	9
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	7	—	10	—	13	—	ns	
Write Command Pulse Width	t_{WP}	7	—	10	—	10	—	ns	
\overline{WE} Pulse Width (DQ Disable)	t_{WPE}	7	—	10	—	10	—	ns	
\overline{OE} Command Hold Time	t_{OEH}	7	—	10	—	13	—	ns	
\overline{OE} Precharge Time	t_{OEP}	7	—	10	—	10	—	ns	
\overline{OE} Command Hold Time	t_{OCH}	7	—	10	—	10	—	ns	
Write Command to \overline{RAS} Lead Time	t_{RWL}	7	—	10	—	13	—	ns	
Write Command to \overline{CAS} Lead Time	t_{CWL}	7	—	10	—	13	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	7	—	10	—	13	—	ns	11
\overline{OE} to Data-in Delay Time	t_{OED}	13	—	15	—	20	—	ns	
\overline{CAS} to \overline{WE} Delay Time	t_{CWD}	30	—	34	—	44	—	ns	10
Column Address to \overline{WE} Delay Time	t_{AWD}	42	—	49	—	59	—	ns	10
\overline{RAS} to \overline{WE} Delay Time	t_{RWD}	67	—	79	—	94	—	ns	10
\overline{CAS} Precharge \overline{WE} Delay Time	t_{CPWD}	47	—	54	—	64	—	ns	10
\overline{CAS} Active Delay Time from \overline{RAS} Precharge	t_{RPC}	5	—	5	—	5	—	ns	
\overline{RAS} to \overline{CAS} Set-up Time (CAS before \overline{RAS})	t_{CSR}	5	—	5	—	5	—	ns	
\overline{RAS} to \overline{CAS} Hold Time (CAS before \overline{RAS})	t_{CHR}	10	—	10	—	10	—	ns	
\overline{WE} to \overline{RAS} Precharge Time (CAS before \overline{RAS})	t_{WRP}	10	—	10	—	10	—	ns	
\overline{WE} Hold Time from \overline{RAS} (CAS before \overline{RAS})	t_{WRH}	10	—	10	—	10	—	ns	
\overline{RAS} to \overline{WE} Set-up Time (Test Mode)	t_{WTS}	10	—	10	—	10	—	ns	
\overline{RAS} to \overline{WE} Hold Time (Test Mode)	t_{WTH}	10	—	10	—	10	—	ns	

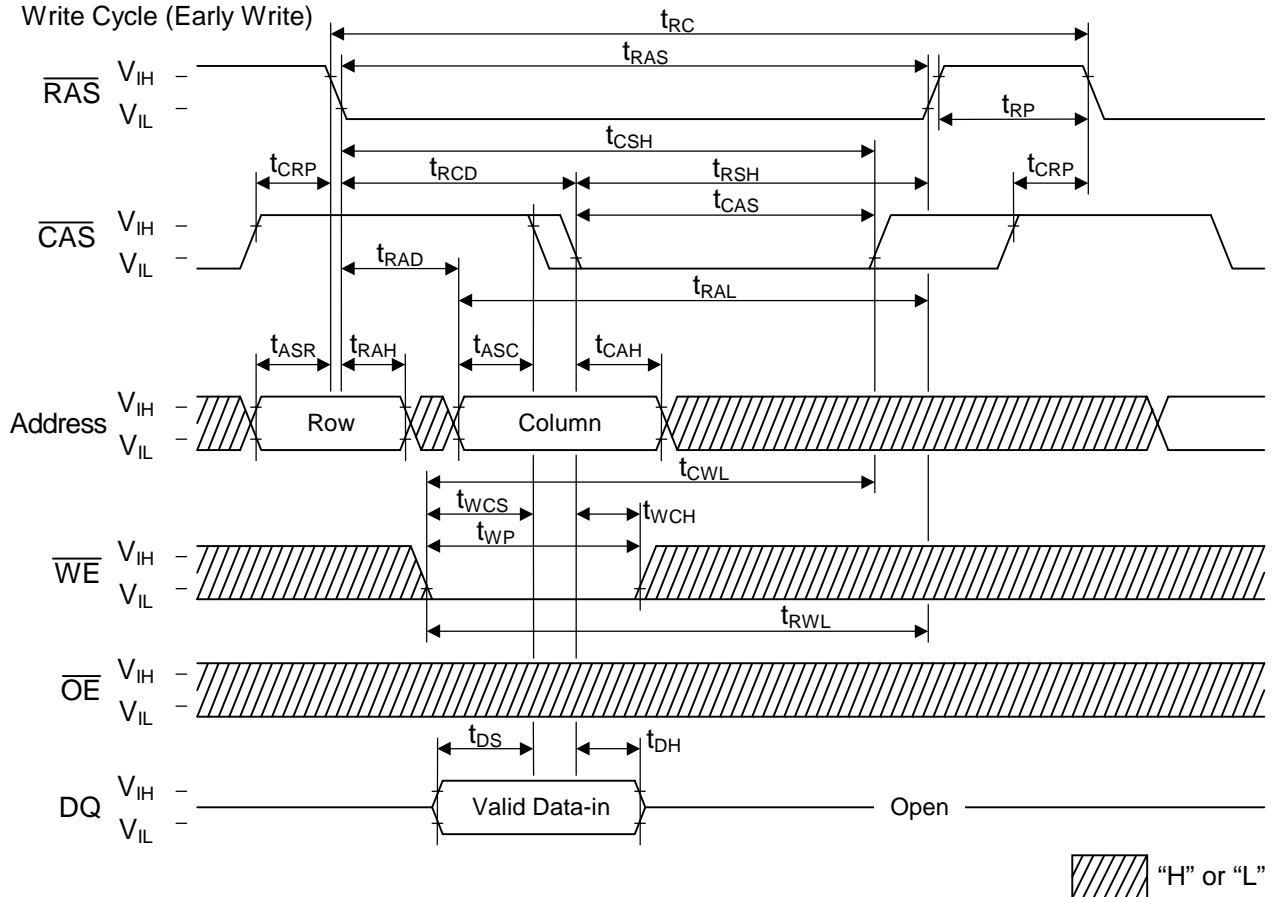
- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 2\text{ns}$.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 2 TTL load and 100pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{CEZ} (Max), t_{REZ} (Max), t_{WEZ} (Max), t_{OEZ} (Max) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.
 8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition.
 9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 10. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in an early write cycle, and to the $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle, or a read modify write cycle.
 12. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 2-bit parallel test function. CA9 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{\text{RAS}}$ -only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 13. In a test mode read cycle, the value of access time parameters is delayed for 5ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.

Timing Chart

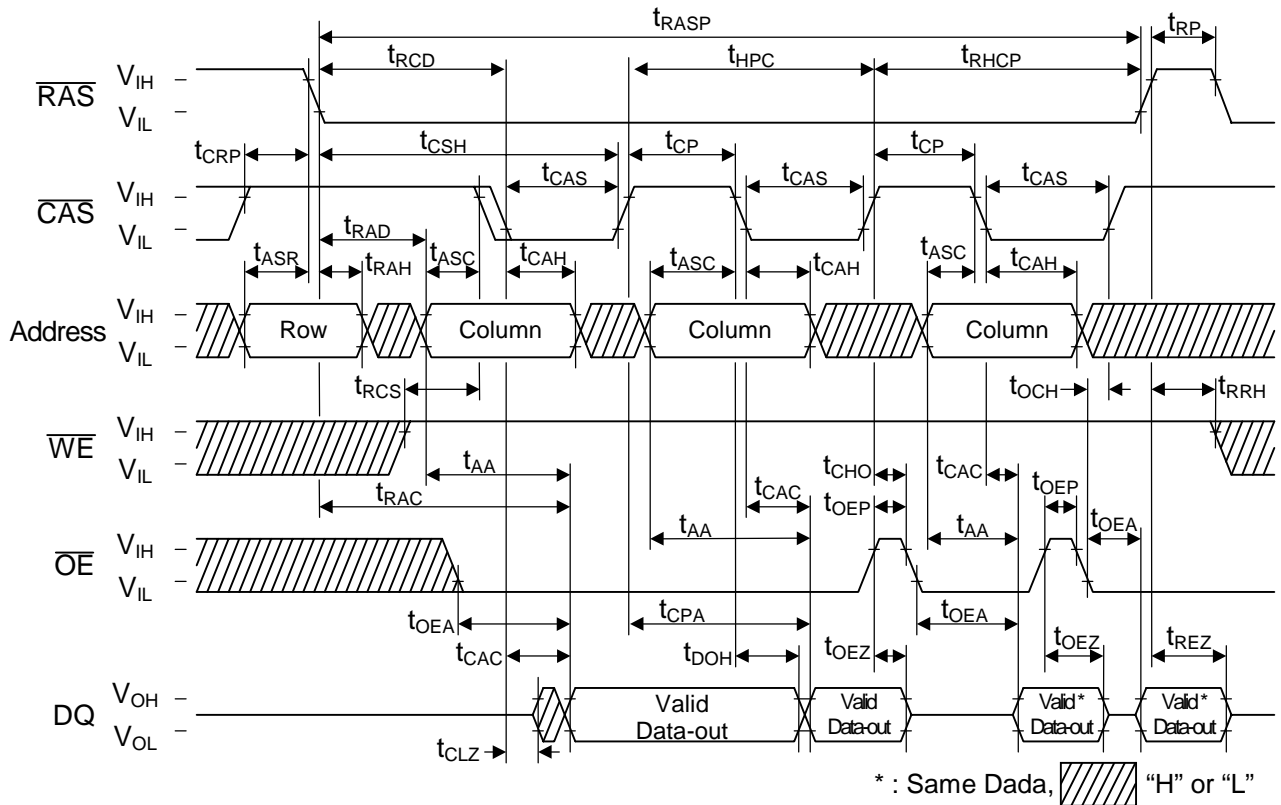
• Read Cycle



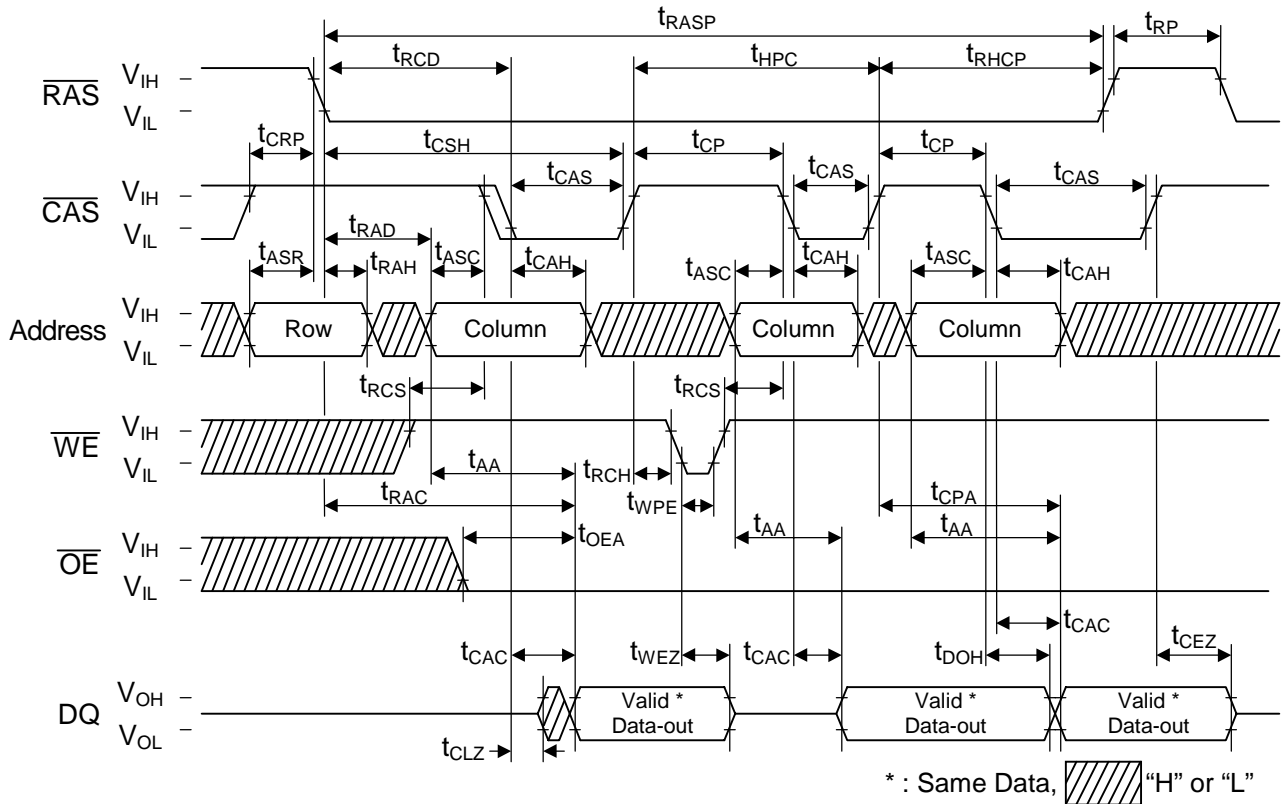
• Write Cycle (Early Write)



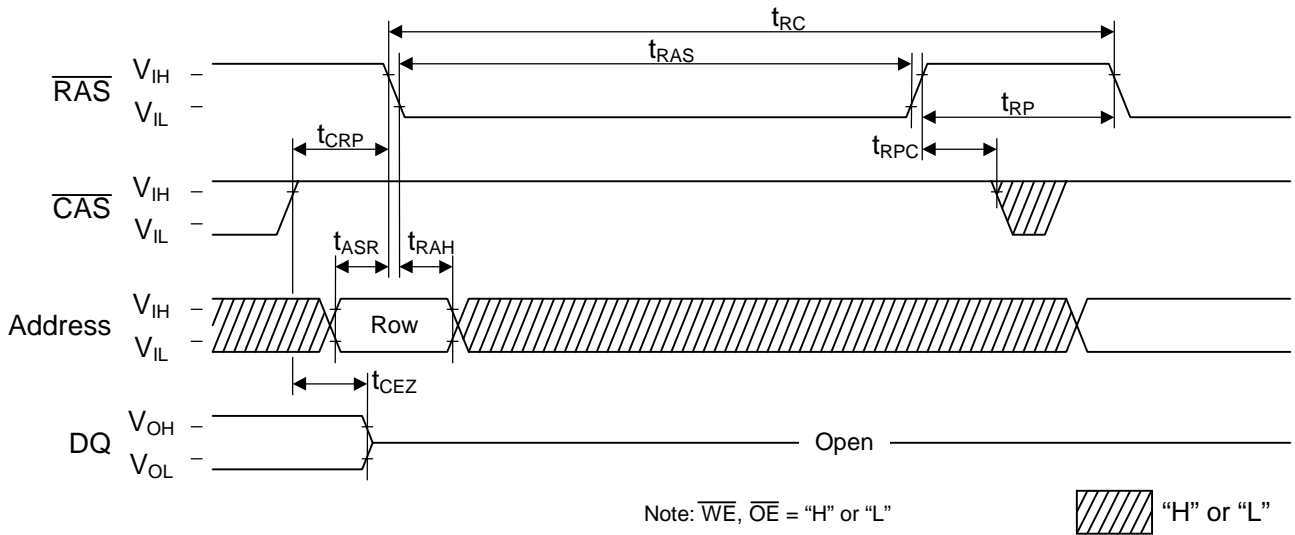
• Fast Page Mode Read Cycle (Part-1)



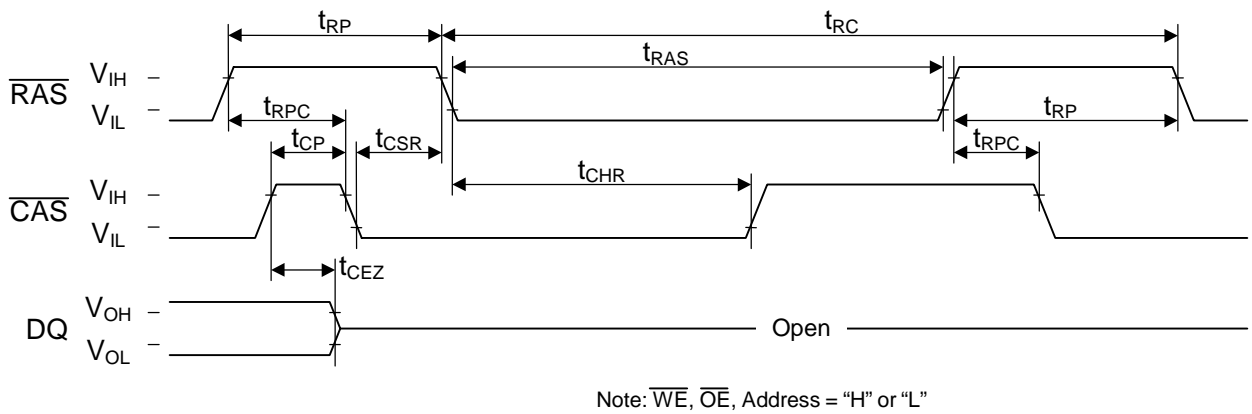
• Fast Page Mode Read Cycle (Part-2)



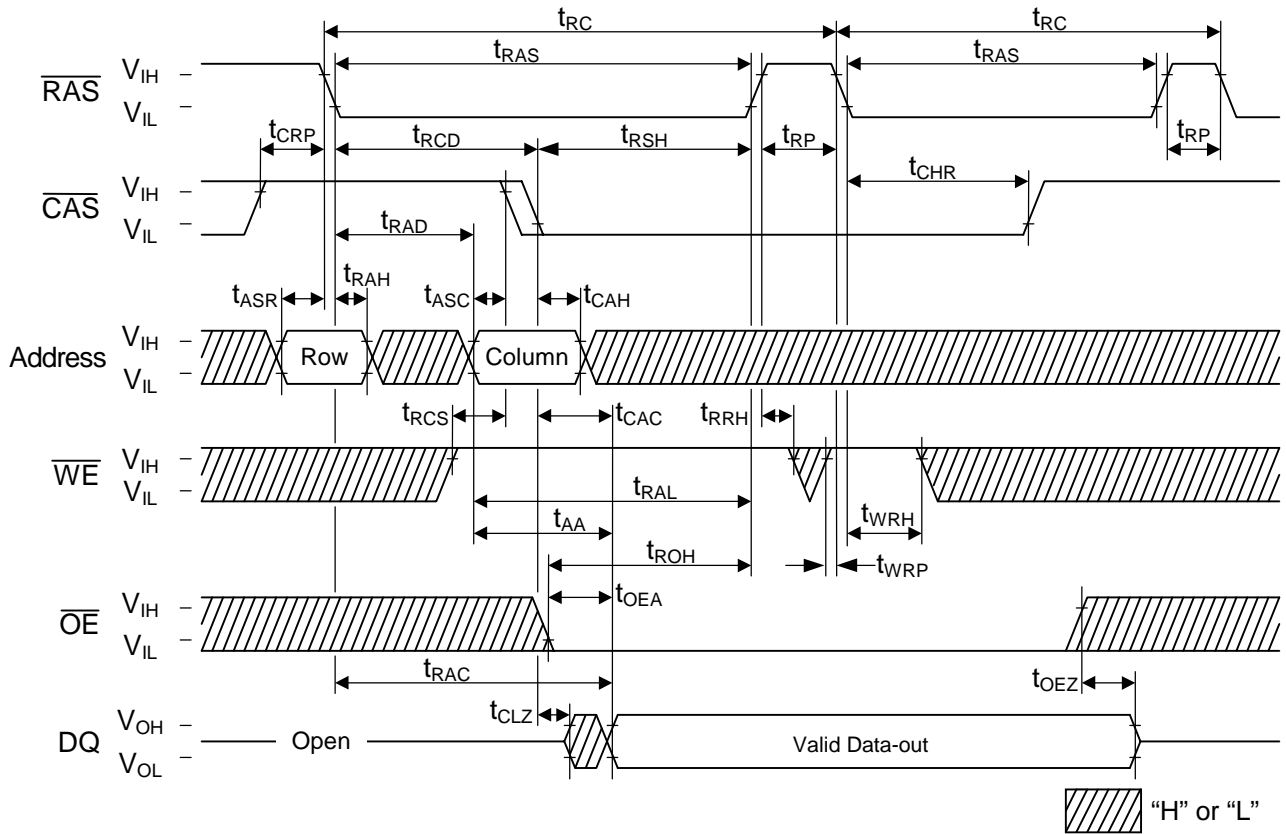
• $\overline{\text{RAS}}$ -Only Refresh Cycle



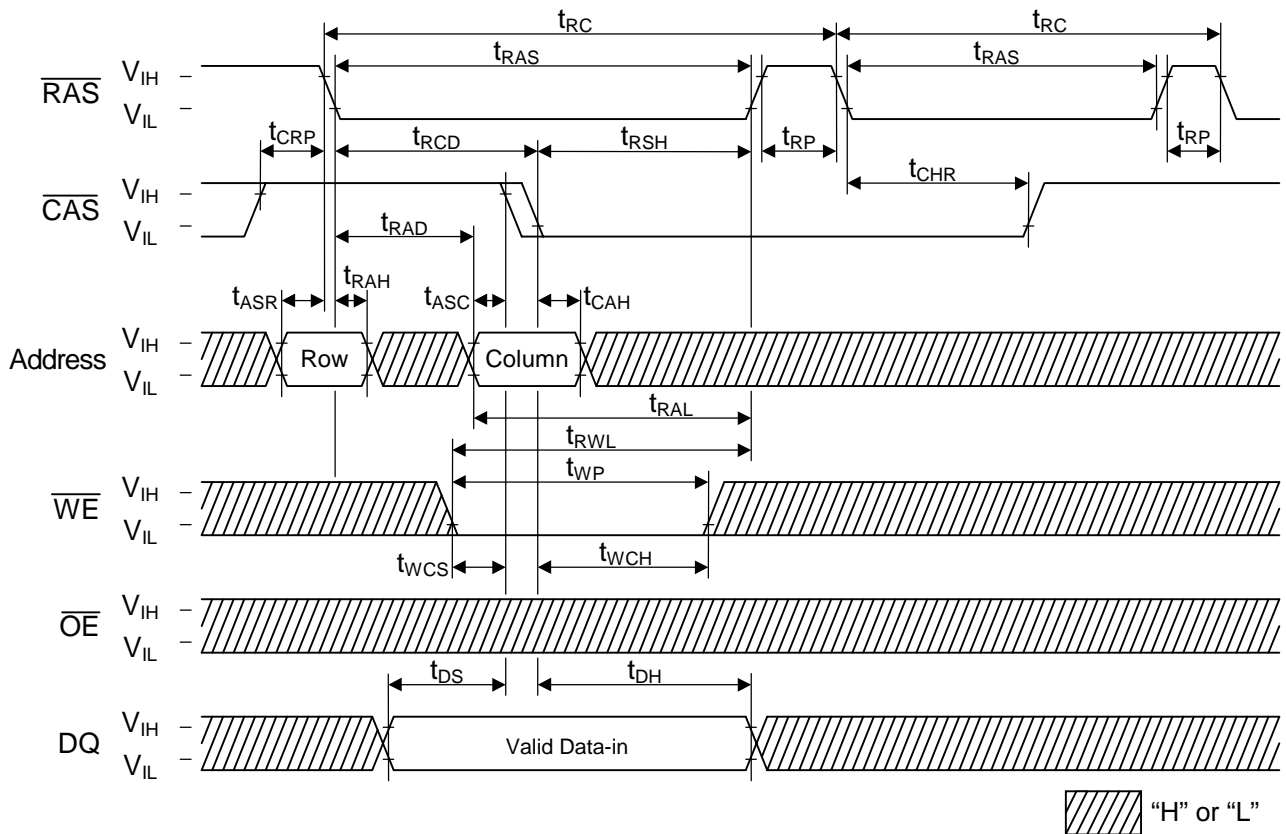
• $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle



• Hidden Refresh Read Cycle



• Hidden Refresh Write Cycle



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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit and assembly designs.
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