pASIC® 2 FPGA FAMILY

Combining Speed, Density, Low Cost and Flexibility
The Ultimate Verilog / VHDL Silicon Solution

Rev. D

FAMILY HIGHLIGHTS

Ultimate Verilog/VHDL Silicon Solution
-Abundant, high-speed interconnect eliminates manual routing
-Flexible logic cell provides high efficiency *and* performance
-Design tools produce fast, efficient Verilog/VHDL synthesis

Speed, Density, Low Cost and Flexibility in One Family
-16-bit counter speeds exceeding 200 MHz
-5,000 to 16,000 usable PLD gates, Up to 225 I/Os
-3-layer metal ViaLink® antifuse for small die sizes
-100% routable and pin-out maintainable

High Performance, Flexible Logic Cell
-High performance through larger logic cells (up to 16 inputs)
-Complex functions (up to 16 product terms) in a single level of delay
-High synthesis utilization from logic cell fragments

Advanced I/O Capabilities
-Individually-clocked input and I/O registers
-Full IEEE Standard JTAG boundary scan capability
-Individually-controlled output enables on all I/O pins
-High-speed, low-skew global clock and control networks

PCI Compliance
-Full speed 33 MHz master and slave implementations
-Fully compliant at 5.0 volts (-1/-2 speed grades)

Other Important Family Features
-5.0 volt and 3.3 volt supply operation
-I/O pin-compatibility between different devices in the same packages
-Upward compatible with pASIC 1 designs
-High design security provided by security fuses

TABLE 1 pASIC 2 Device Family

	QL2003	QL2005	QL2007	QL2009
ASIC Gates	3,000	5,000	7,000	9,000
Usable PLD Gates	5,000	8,000	11,000	16,000
Logic Cells	192	320	480	672
Max. Flip-Flops	408	636	912	1236
Maximum I/Os	118	156	174	225
Packages	84 PLCC 100 TQFP 144 TQFP	84 PLCC 144 TQFP 208 PQFP	84 PLCC 144 TQFP 208 PQFP	144 TQFP 208 PQFP 256 PBGA

QUICKLOGIC

FAMILY SUMMARY

As shown in Table 1 on the previous page, QuickLogic's pASIC 2 family includes seven FPGAs ranging from 5,000 to over 16,000 usable PLD gates and 84 to 256 package pins. This family employs a unique combination of architecture, technology, and software tools to provide high speed, high usable density, low price, and flexibility in the same devices. The flexibility and speed make pASIC 2 devices an efficient and high-performance silicon solution for designs described using HDLs such as Verilog and VHDL, as well as schematics.

Devices in the pASIC 2 family are based on an array of highly flexible logic cells which have been optimized to efficiently implement a wide range of logic functions at high speed. Each cell can implement one large function, five independent smaller functions, or any combination in-between. This flexibility gives synthesized designs efficient logic utilization plus high performance within the same device.

Logic cells are configured and interconnected by rows and columns of routing metal and ViaLink metal-to-metal programmable-via antifuses. Due to their small size, ViaLink antifuses may be placed at every desired routing track junction. In the pASIC 2 family, the benefits of ViaLink technology are further enhanced by a three-layer metal process which allows all routing and programmable elements to be placed above, rather than adjacent to the logic cells. This approach allows abundant interconnect resources with small die sizes, providing users with 100% routability and pin-out maintainability with low device costs.

The extremely low resistance of a programmed ViaLink antifuse, combined with the flexible logic cell architecture, makes pASIC 2 devices among the fastest FPGAs available. Datapath speeds exceed 225 MHz and counters run at over 200 MHz. Internal logic cell delays are under 2 ns and total input to output combinatorial logic delays are under 6 ns. This performance permits QuickLogic pASIC 2 FPGAs to be used with today's fastest CISC and RISC microprocessors, while consuming a fraction of the power and board area of PAL, GAL, and discrete logic solutions.

A wide range of additional family features complement the pASIC 2 family. All members include speed grades which are PCI compliant at 5.0 volts and are capable of implementing bus master and target applications at 33 MHz. I/O pins provide individually-controlled output enables, dedicated input/feedback registers, and full implementation of IEEE standard 1149.1a JTAG for boundary scan and test. In addition, pASIC 2 devices provide the benefits of non-volatility, high design security, no configuration load times, and self-contained single chip solutions.

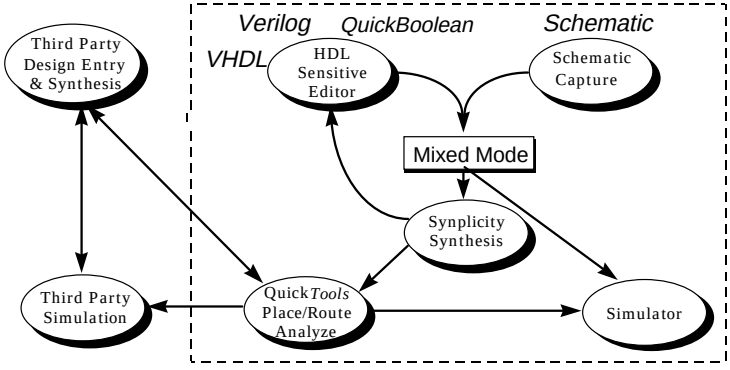
All devices share a common architecture and development software to allow easy transfer of designs from one product to another. Different devices in the same package are pin-compatible with one another, permitting easy design migration within the family. In addition, pASIC 2 devices are architectural supersets of pASIC 1 devices, providing a means for users to upgrade existing designs by integrating additional logic or increasing performance.

DEVELOPMENT TOOLS

Software support for the pASIC 2 family is available through three basic packages. The turnkey PC-based Quick*Works*® package, shown in Figure 1, provides the most complete FPGA software solution from design entry, to logic synthesis, to place and route, to simulation. Quick*Works* includes VHDL, Verilog, schematic, boolean, and mixed-mode entry with fast and efficient logic synthesis provided by the integrated Synplicity Synplify Lite™ tool, specially tuned to take advantage of the pASIC 2 architecture. Quick*Works* also provides functional and timing simulation for guaranteed timing and source-level debugging.

The PC/Sun/HP-based Quick*Tools*™ and PC-based Quick*Chip*™ packages are a subset of Quick*Works* and provide a solution for designers who use Cadence, Mentor, Synopsys, Viewlogic, Veribest, or other third-party tools for design entry, synthesis, or simulation. Quick*Tools* and Quick*Chip* read EDIF netlists and provide optimization, place and route, timing analysis, and back-annotation support for all QuickLogic devices. Quick*Tools* and Quick*Chip* also write out OVI, VITAL, VSS, EDIF, LMC, SDF, and Viewsim files to support a wide range of third-party modeling and simulation tools.

In addition, the PC-version of the Quick*Tools* package includes a schematic capture tool, providing a low-cost design entry and compilation solution.



Quick*Works* Tool Suite

FIGURE 1 Quick*Works* Tool Suite

ORGANIZATION

The pASIC 2 family contains devices covering a wide spectrum of I/O and density requirements. The seven members range from 192 logic cells to 672 logic cells arranged in regular arrays as shown in Figure 2. The single lines between logic cells in the figure below represent channels containing up to thirty wires, which are actually placed above the logic cells in the physical devices.

THREE LAYER METAL CMOS PROCESS

QuickLogic pASIC 2 devices are fabricated on a conventional high-volume CMOS process. The base technology is a 0.65 micron, n-well CMOS technology with a single polysilicon layer and three layers of metal interconnect. The only deviation from the standard process flow occurs when a single mask is used for the amorphous silicon to form the ViaLink elements between the metal deposition steps.

FAST, FLEXIBLE ARCHITECTURE

The pASIC 2 device architecture consists of an array of user-configurable logic building blocks, called logic cells, set beneath a grid of metal wiring channels similar to those of a gate array. The pASIC 2 logic cell is a general-purpose building block that can implement most TTL and gate array macro library functions. It is a superset of the pASIC 1 cell, allowing easy design upgrades. The cell has been optimized to maintain the inherent speed advantage of the ViaLink technology while ensuring maximum logic flexibility.

For a detailed description of the pASIC 2 logic cell, as well as the I/O cell and routing structure, consult the pASIC 3 FPGA Family data sheet in this data book. pASIC 2 devices have exactly the same architecture as the pASIC 3 QL3012 and QL3025.

FIGURE 2
192 to 672 Logic Cells