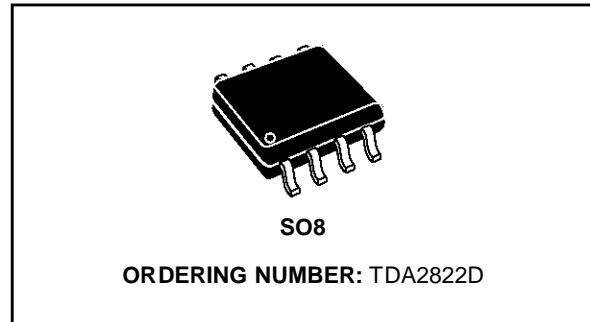


**DUAL LOW-VOLTAGE POWER AMPLIFIER**

- SUPPLY VOLTAGE DOWN TO 1.8V
- LOWCROSSOVER DISTORTION
- LOW QUIESCENT CURRENT
- BRIDGE OR STEREO CONFIGURATION

**DESCRIPTION**

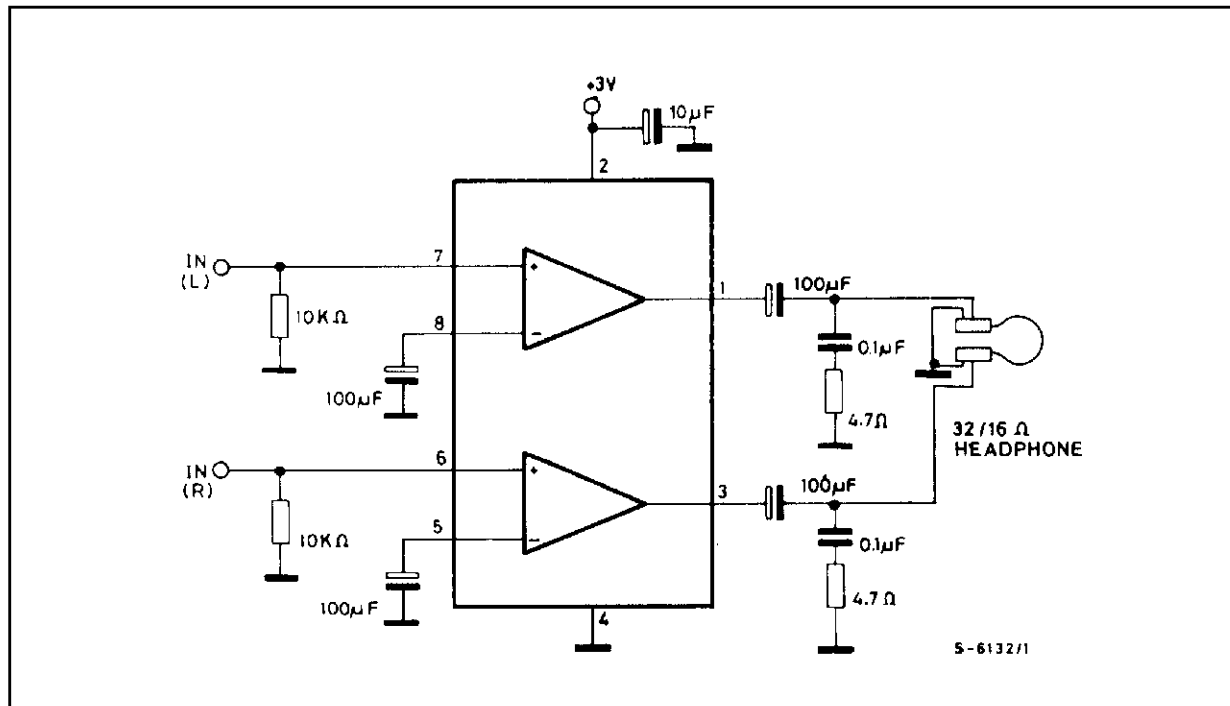
The TDA2822D is a monolithic integrated circuit in 8 lead (SO-8) package. It is intended for use as dual audio power amplifier in portable cassette players, radios and CD players



**ABSOLUTE MAXIMUM RATINGS**

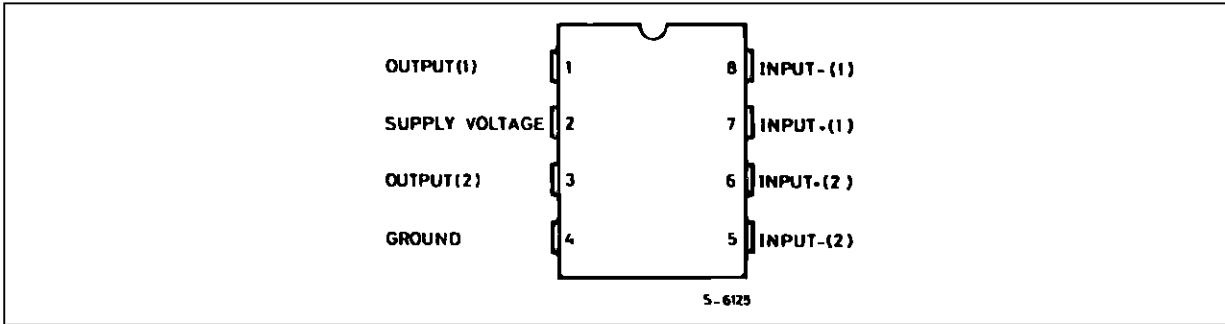
Symbol	Parameter	Value	Unit
V <sub>s</sub>	Supply Voltage	15	V
I <sub>o</sub>	Peak Output	1	A
P <sub>tot</sub>	Total Power Dissipation T <sub>amb</sub> = 50°C	0.5	W
T <sub>stg</sub> , T <sub>j</sub>	Storage and Junction Temperature	-40 to 150	°C

**APPLICATION CIRCUIT**



# TDA2822D

## PIN CONNECTION (Top view)



## THERMAL DATA

Symbol	Description	Value	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max 200	°C/W

Figure 1: Stereo Application and Test Circuit

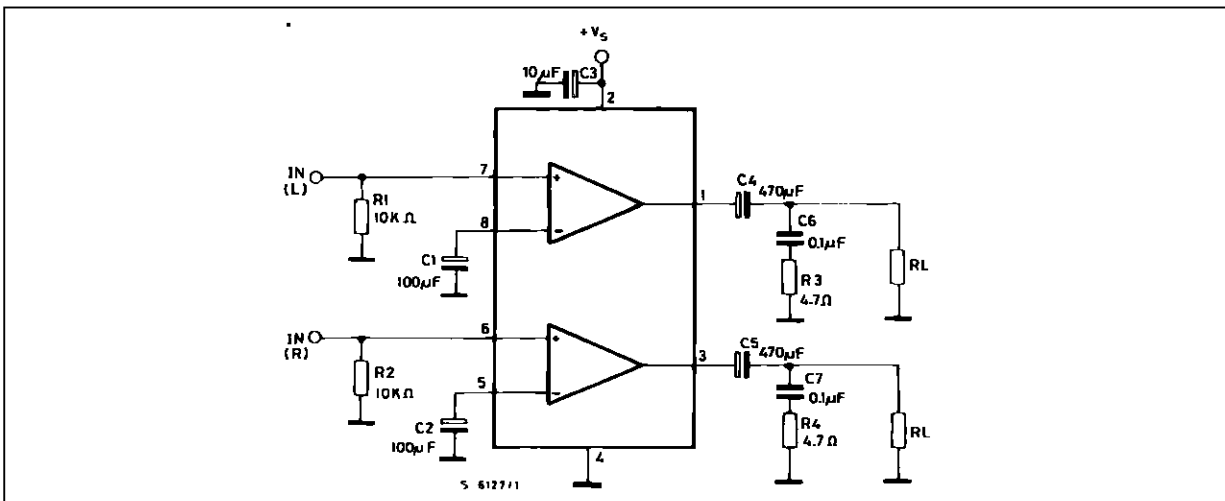
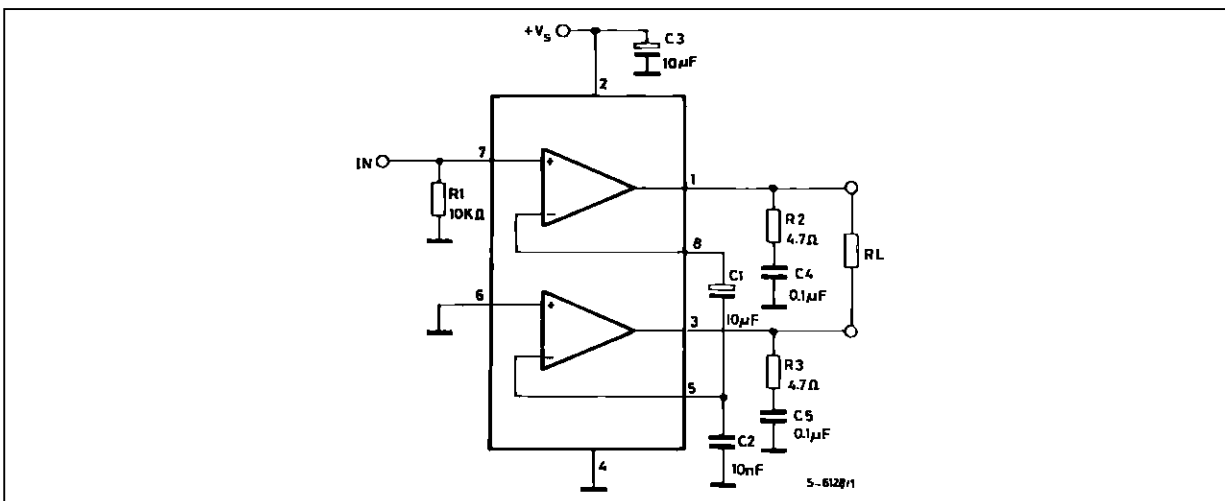


Figure 2: Bridge Application and Test Circuit



**ELECTRICAL CHARACTERISTICS** ( $V_S = 6V$ ;  $T_{amb} = 25^\circ C$ , unless otherwise specified.

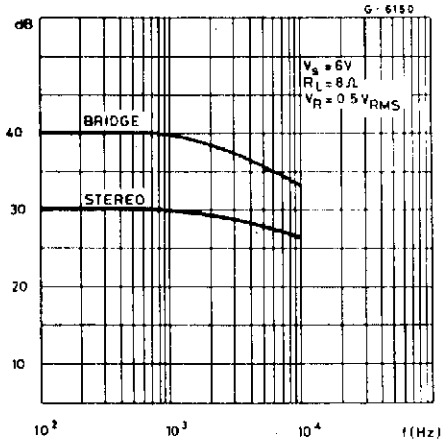
STEREO (Test circuit of fig. 1).

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
$V_S$	Supply Voltage			1.8		15	V
$I_d$	Total Quiescent Drain Current					15	mA
$V_O$	Quiescent Output Voltage				2.7		V
		$V_S = 3V$			1.2		V
$I_b$	Input Bias Current				100		nA
$P_O$	Output Power (each channel) ( $f = 1KHz$ , $d = 10\%$ )	$R_L = 32\Omega$	$V_S = 9V$		300		mW
			$V_S = 6V$		120		
			$V_S = 4.5V$		60		
			$V_S = 3V$		20		
			$V_S = 2V$		5		
		$R_L = 16\Omega$	$V_S = 6V$	170	220		mW
		$R_L = 8\Omega$	$V_S = 6V$	300	380		mW
		$R_L = 4\Omega$	$V_S = 4.5V$ $V_S = 3V$		320 110		mW mW
d	Distortion	$R_L = 32\Omega$	$P_O = 40mW$		0.2		%
		$R_L = 16\Omega$	$P_O = 75mW$		0.2		%
		$R_L = 8\Omega$	$P_O = 150mW$		0.2		%
$G_V$	Closed Loop Voltage Gain	$f = 1KHz$		36	39	41	dB
$\Delta G_V$	Channel Balance					$\pm 1$	dB
$R_i$	Input Resistance	$f = 1KHz$		100			K $\Omega$
$e_N$	Total Input Noise	$R_s = 10k\Omega$ B = Curve A			2		$\mu V$
		$R_s = 10k\Omega$ B = 22KHz to 22KHz			2.5		$\mu V$
SVR	Supply Voltage Rejection	$f = 100Hz$	$C_1 = C_2 = 100\mu F$	24	30		dB
$C_s$	Channel Separation	$f = 1KHz$			50		dB

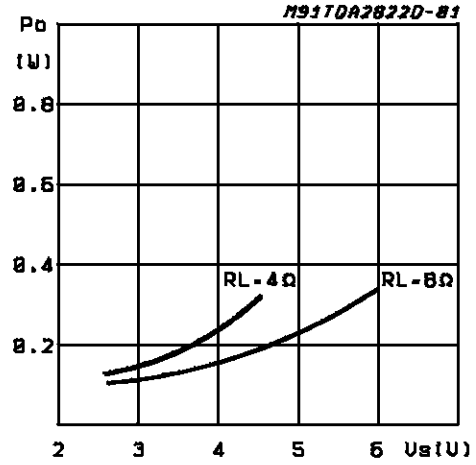
## BRIDGE (Test circuit of fig.2)

$V_S$	Supply Voltage			1.8		15	V
$I_d$	Total Quiescent Drain Current	$R_L = \infty$				15	mA
$V_{os}$	Output Offset Voltage (between the outputs)	$R_L = 8\Omega$				$\pm 80$	mV
$I_b$	Input Bias Current				100		nA
$P_O$	Output Power ( $f = 1KHz$ , $d = 10\%$ )	$R_L = 32\Omega$	$V_S = 9V$	320	1000		mW
			$V_S = 6V$		400		
			$V_S = 4.5V$		200		
			$V_S = 3V$	50	65		
			$V_S = 2V$		8		
		$R_L = 16\Omega$	$V_S = 6V$ $V_S = 3V$		800 120		mW mW
		$R_L = 8\Omega$	$V_S = 4.5V$ $V_S = 3V$		700 220		mW mW
		$R_L = 4\Omega$	$V_S = 3V$ $V_S = 2V$		350 80		mW mW
d	Distortion	$R_L = 8\Omega$ $P_O = 0.5W$ $f = 1KHz$			0.2		%
$G_V$	Closed Loop Voltage Gain	$f = 1KHz$			39		dB
$R_i$	Input Resistance	$f = 1KHz$		100			K $\Omega$
$e_N$	Total Input Noise	$R_s = 10k\Omega$ B = Curve A			2.5		$\mu V$
		$R_s = 10k\Omega$ B = 22KHz to 22KHz			3		$\mu V$
SVR	Supply Voltage Rejection	$f = 100Hz$			40		dB
B	Power Bandwidth (-3dB)	$R_L = 8\Omega$ $P_O = 1W$			120		KHz

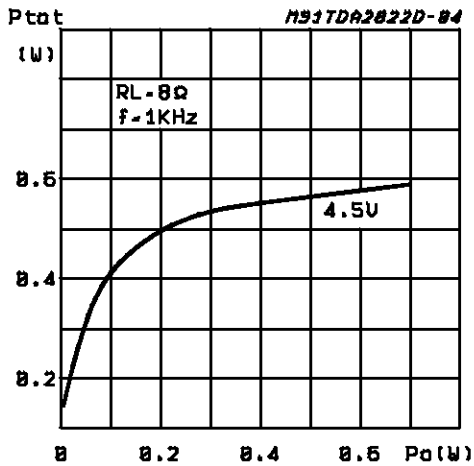
**Figure 3:** Supply Voltage Rejection vs. Frequency



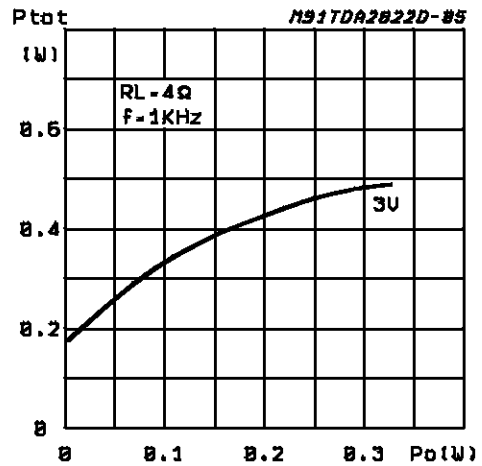
**Figure 4:** Output Power vs. Supply Voltage (THD = 10%, f = 1KHz Stereo)



**Figure 5:** Total Power Dissipation vs. Output Power (Bridge)

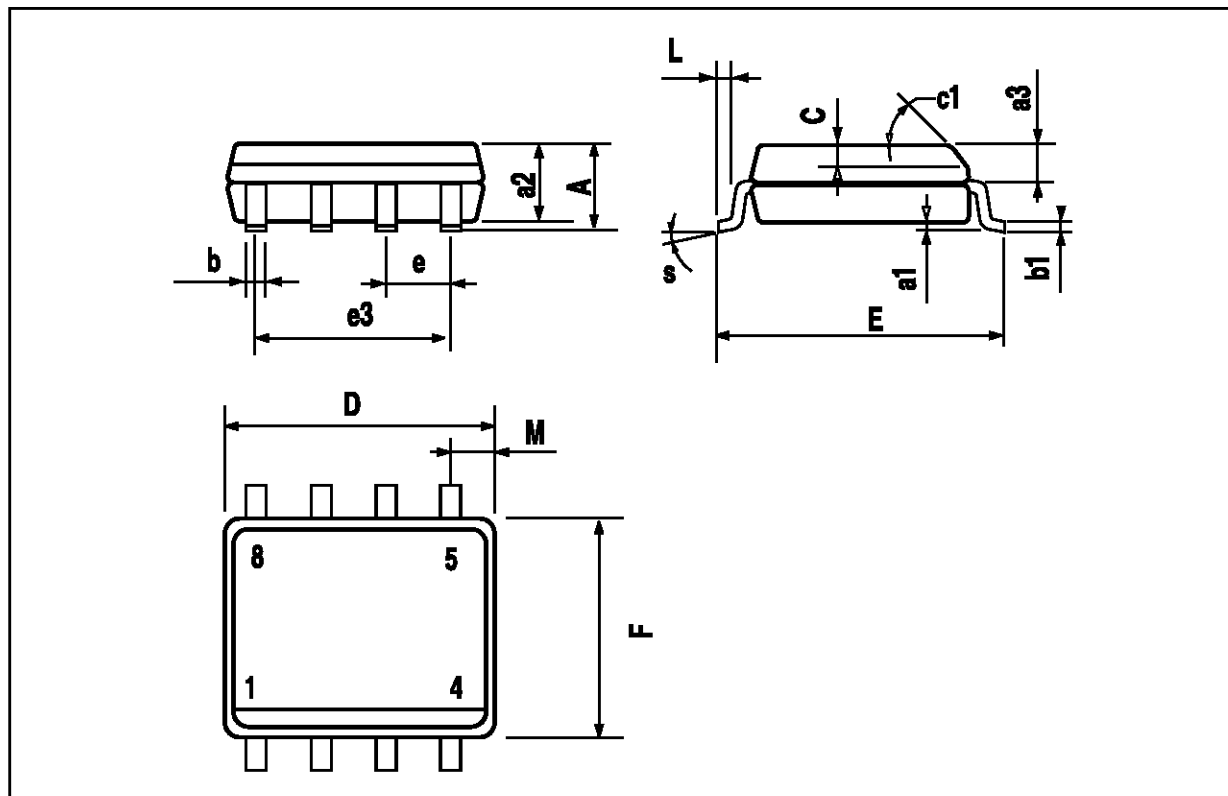


**Figure 6:** Total Power Dissipation vs. Output Power (Bridge)



## SO8 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					



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