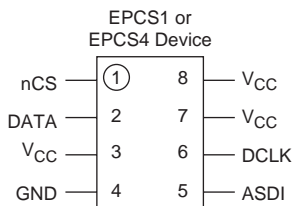


## Features

- 1- and 4-Mbit flash memory devices that serially configure Cyclone™ FPGAs
- Easy-to-use four-pin interface
- Low cost, low pin count and non-volatile memory
- Low current during configuration and near-zero standby mode current
- 3.3-V operation
- Available in 8-pin small outline integrated circuit (SOIC) package
- Enables the Nios® processor to access unused flash memory through active serial (AS) memory interface
- Re-programmable memory with more than 100,000 erase/program cycles
- Programming support with ByteBlaster™ II download cable
- Additional programming support with the Altera® Programming Unit (APU) and programming hardware from BP Microsystems, System General, and other vendors
- Software design support with the Altera Quartus® II development system for Windows-based PCs as well as Sun SPARC station and HP 9000 Series 700/800
- Delivered with the memory array erased (all the bits set to 1)

Figure 1 shows the Altera serial configuration device 8-pin SOIC package and its pin-out diagram.

**Figure 1. Altera Serial Configuration Device Package Pin-Out Diagram**



Whenever the term “serial configuration device(s)” is used in this document, it refers to Altera EPCS1 and EPCS4 devices.

## Functional Description

With SRAM-based devices such as Cyclone FPGAs, configuration data must be reloaded each time the system initializes, or when a new configuration is needed. Serial configuration devices are flash memory devices with a serial interface that can store configuration data for a Cyclone device and reload the data to the device upon power-up or reconfiguration. [Table 1](#) lists the serial configuration devices.

<b>Table 1. Serial Configuration Devices (3.3-V Operation)</b>	
<b>Device</b>	<b>Memory Size (Bits)</b>
EPCS1	1,048,576
EPCS4	4,194,304

[Table 2](#) lists the serial configuration device used with each Cyclone FPGA and the configuration file size.

<b>Table 2. Serial Configuration Device for Cyclone Devices</b>			
<b>Cyclone Device</b>	<b>Configuration File Size (Mbits) (1)</b>	<b>Serial Configuration Device</b>	
		<b>EPCS1</b>	<b>EPCS4</b>
EP1C3	0.628	✓	✓
EP1C4	0.925	✓	✓
EP1C6	1.167	✓	✓
EP1C12	2.324		✓
EP1C20	3.559		✓

**Note to [Table 2](#):**

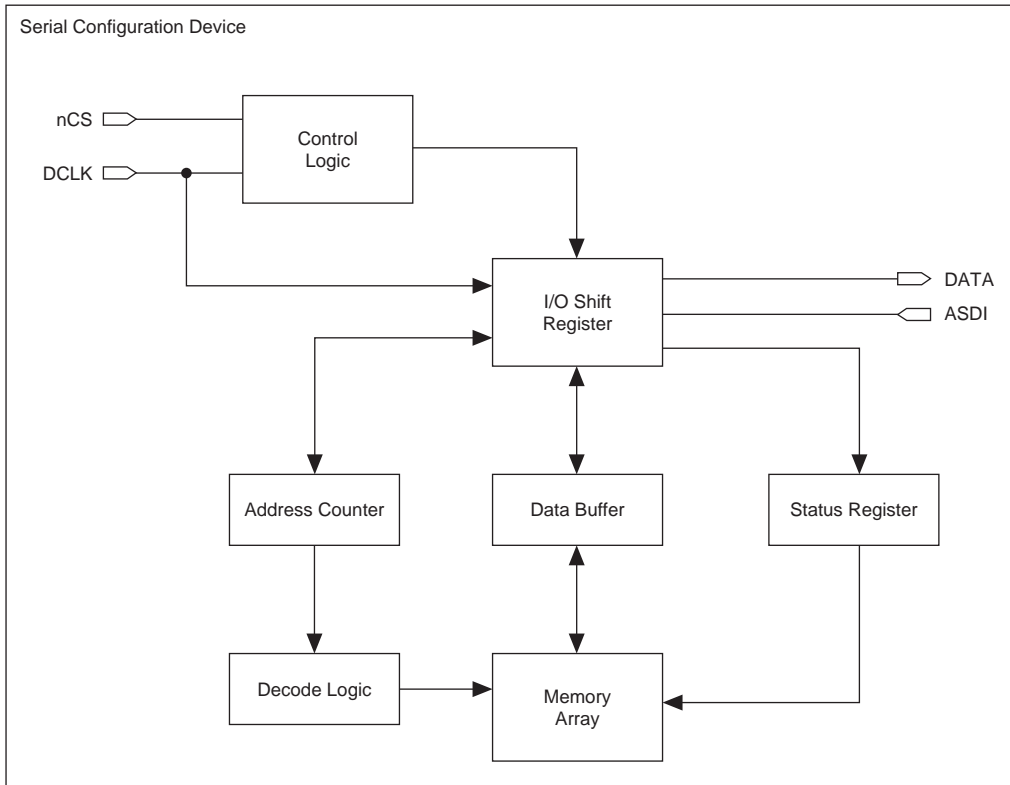
(1) These are preliminary, uncompressed file sizes.

With the new data-decompression feature in the Cyclone FPGA family, designers can use smaller serial configuration devices to configure larger Cyclone FPGAs. Serial configuration devices cannot be cascaded.



See [AN 250: Configuring Cyclone FPGAs](#) for more information regarding the Cyclone FPGA decompression feature in AS mode.

The serial configuration devices are designed to configure Cyclone FPGAs and cannot configure other existing device families. [Figure 2](#) shows the serial configuration device block diagram.

**Figure 2. Serial Configuration Device Block Diagram**

## Accessing Memory in Serial Configuration Devices

A designer can access the unused memory locations of the serial configuration device through the Nios processor and SOPC Builder to store/retrieve data or configuration files. SOPC Builder is an Altera tool for creating bus-based (especially microprocessor-based) systems in Altera devices. SOPC Builder assembles library components like processors and memories into custom microprocessor systems.

SOPC Builder includes an interface core specifically for the serial configuration device. Using this core, a designer can create a system with a Nios embedded processor that allows software access to any memory location within the serial configuration device.



For more information on accessing memory within the serial configuration device, contact Altera Applications.

## Pin Description

As shown in [Figure 1](#), the serial configuration device is an 8-pin device. The control pins on the serial configuration device are: serial data output (DATA), active serial data input (ASDI), serial clock (DCLK), and chip select (nCS). [Table 3](#) shows the serial configuration device's pin descriptions.

*Table 3. Serial Configuration Device Pin Description*

Pin Name	Pin Number	Pin Type	Description
DATA	2	Output	DATA output signal transfers the data serially out of the serial configuration device into the Cyclone FPGA during read/configuration operation. During a read/configuration operation, the serial configuration device is enabled by pulling nCS low. The DATA signal transitions on the falling edge of DCLK.
ASDI	5	Input	Active serial data input signal is used to transfer data serially into the serial configuration device. It receives the data that should be programmed into the serial configuration device. Values register on the rising edge of DCLK.
nCS	1	Input	Active low chip select input signal toggles at the beginning and end of a valid instruction. When this signal is high, the device is deselected and the DATA signal is tri-stated. When the signal is low, it enables the device and puts the device in an active mode. After power up, the serial configuration device requires a falling edge on the nCS signal before beginning any operation.
DCLK	6	Input	DCLK is provided by the Cyclone FPGA. This signal provides the timing of the serial interface. The data presented at ASDI are latched in to the serial configuration device, at the rising edge of DCLK. Data on the DATA pin changes after the falling edge of DCLK and is latched into the Cyclone FPGA on the rising edge.
VCC	3, 7, 8	Power	Power pins connect to 3.3 V.
GND	4	Ground	Ground pin.

## Programming & Configuration File Support

The Quartus II design software provides programming support for serial configuration devices. After selecting the serial configuration device, the Quartus II software automatically generates the Programmer Object File (.pof) to program the device. The software allows users to select the appropriate serial configuration device density that most efficiently stores the configuration data for a selected Cyclone FPGA.

Serial configuration devices are programmed using the APU with the appropriate programming adapter (PLMSEPC-8) via the Quartus II software or the ByteBlaster II download cable via the Quartus II software. In addition, many third-party programmers, such as BP Microsystems and System General, offer programming hardware that supports serial configuration devices.

During in-system programming of a serial configuration device via the ByteBlaster II download cable, the cable pulls  $nCONFIG$  low to reset the Cyclone device and overrides the 10-k $\Omega$  pull-down resistors on the Cyclone device's  $nCE$  pin (see Figure 5). The download cable then uses the four interface pins (DATA,  $nCS$ , ASDI, and DCLK) to program the serial configuration device memory. Once the programming is complete, the download cable releases the serial configuration device's four interface pins and the Cyclone device's  $nCE$  pin, and pulses  $nCONFIG$  to start configuration.

Figure 3 shows the timing waveform for write operation to the serial configuration device.

**Figure 3. Write Operation Timing**

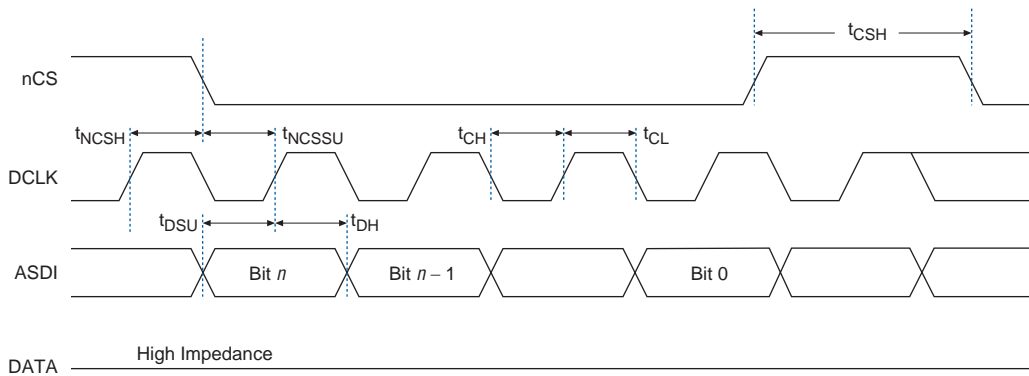


Table 4 defines the serial configuration device timing parameters for write operation.

Symbol	Parameter	Min	Max	Unit
$f_{WCLK}$	Write clock frequency (from Cyclone FPGA or ByteBlaster II cable)		20	MHz
$t_{CH}$	DCLK high time	25		ns
$t_{CL}$	DCLK low time	25		ns
$t_{NCSSU}$	Chip select ( $nCS$ ) setup time	10		ns
$t_{NCSSH}$	Chip select ( $nCS$ ) hold time	10		ns
$t_{DSU}$	Data (ASDI) in setup time before rising edge on DCLK	5		ns
$t_{DH}$	Data (ASDI) hold time after rising edge on DCLK	5		ns
$t_{CSH}$	Chip select high time	100		ns

Figure 4 shows the timing waveform for the serial configuration device's read operation.

**Figure 4. Read Operation Timing**

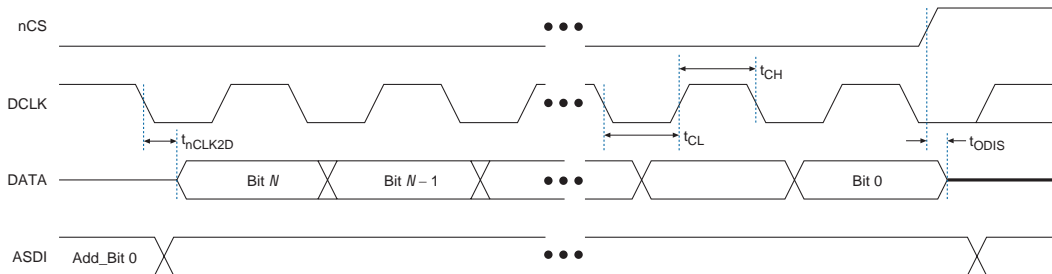


Table 5 defines the serial configuration device timing parameters for read operation.

Symbol	Parameter	Min	Max	Unit
$f_{RCLK}$	Read clock frequency (from Cyclone FPGA)		20	MHz
$t_{CH}$	DCLK high time	25		ns
$t_{CL}$	DCLK low time	25		ns
$t_{ODIS}$	Output disable time after read		15	ns
$t_{nCLK2D}$	Clock falling edge to data		15	ns



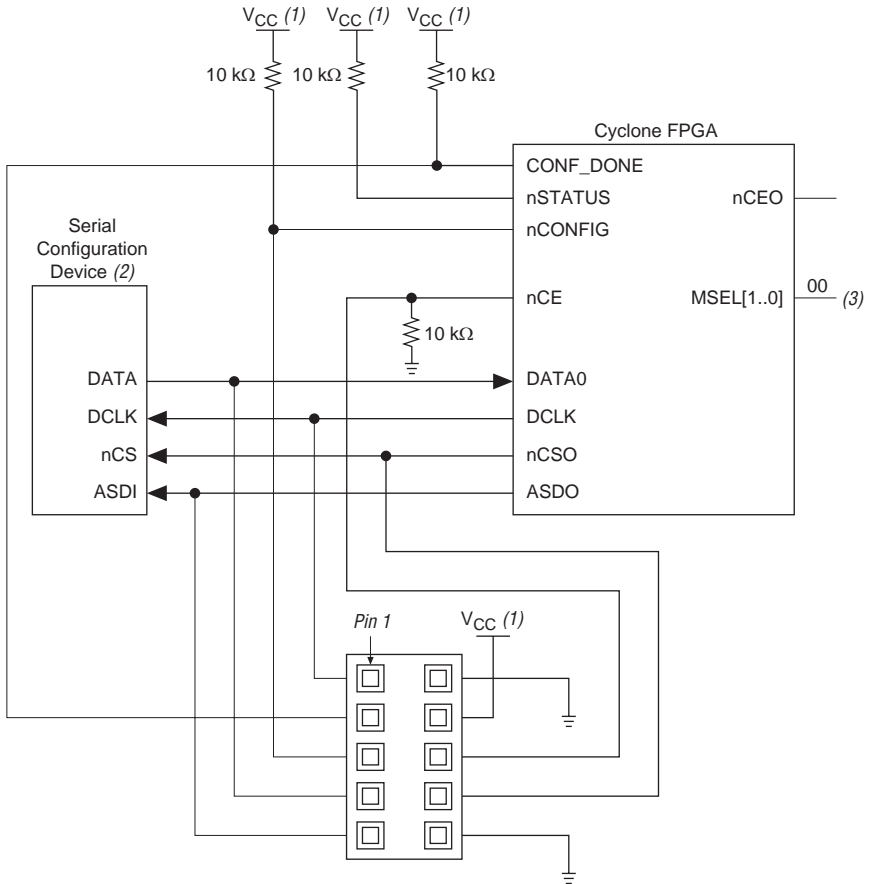
For more information on programming and configuration support, see the following documents:

- [Altera Programming Hardware Data Sheet](#)
- [Programming Hardware Manufacturers](#)
- [ByteBlaster II Parallel Port Download Cable Data Sheet](#)

## Cyclone FPGA Configuration

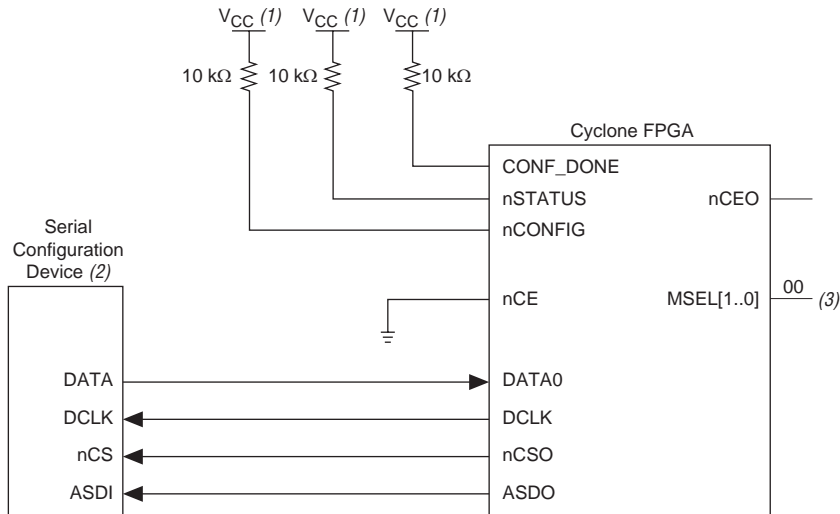
Cyclone FPGAs can be configured with a serial configuration device through AS configuration mode. There are four signals on the serial configuration device that interface directly with the Cyclone device's control signals. The serial configuration device signals DATA, DCLK, ASDI, and nCS interface with DATA0, DCLK, ASDO, and nCSO control signals on a Cyclone FPGA, respectively. Figure 5 shows a serial configuration device programmed via a download cable configuring a Cyclone FPGA in AS mode. Figure 6 shows a serial configuration device programmed using the APU or a third-party programmer configuring a Cyclone FPGA in AS configuration mode.

**Figure 5. Cyclone Configuration in AS Mode (Serial Configuration Device Programmed Using Download Cable)**





**Figure 6. Cyclone Configuration in AS Mode (Serial Configuration Device Programmed by APU or Third-Party Programmer)**



**Notes to Figures 5 and 6:**

- (1)  $V_{CC} = 3.3$  V.
- (2) Serial configuration devices cannot be cascaded.
- (3) Set MSEL0 to 0 and MSEL1 to 0 for AS configuration mode.

The Cyclone FPGA acts as the configuration master in the configuration flow and provides the DCLK to the serial configuration device. The Cyclone device enables the serial configuration device by pulling the nCS signal low via the nCSO signal (See Figures 5 and 6). Consequently, the Cyclone FPGA sends the instructions and addresses to the serial configuration device via the ASDO signal. The serial configuration device responds to the instructions by sending the configuration data to the Cyclone FPGA's DATA0 pin on the falling edge of DCLK. The data is latched into the Cyclone device's DCLK signal's rising edge.

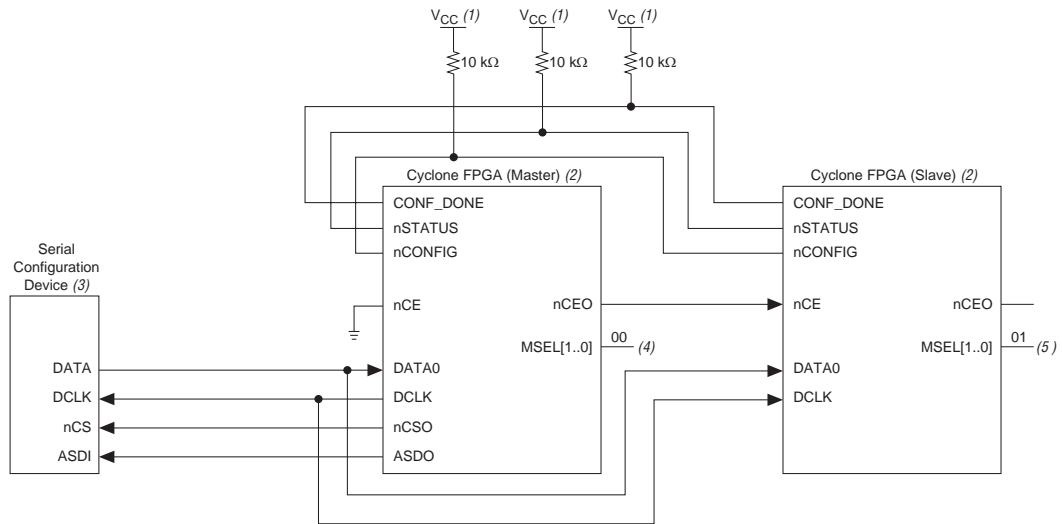
The Cyclone FPGA controls the nSTATUS and CONF\_DONE pins during configuration in AS mode. If the CONF\_DONE signal does not go high at the end of configuration or if the signal goes high too early, the Cyclone FPGA will pulse its nSTATUS pin low to start reconfiguration. Upon successful configuration, the Cyclone FPGA releases the CONF\_DONE pin, allowing the external 10-k $\Omega$  resistor to pull this signal high. Initialization begins after the CONF\_DONE goes high and completes within 136 clock cycles. After initialization, the Cyclone FPGA enters user mode.



For more information on configuring Cyclone FPGAs in AS mode or other configuration modes, see [AN 250: Configuring Cyclone FPGAs](#).

Serial configuration devices cannot be cascaded. Therefore, when a design requires multiple Cyclone FPGAs, the Cyclone FPGAs are configured by a single serial configuration device. Check [Table 1](#) to ensure the programming file size of the cascaded Cyclone FPGAs does not exceed the capacity of a serial configuration device. Designers can choose any serial configuration device according to the system requirements. [Figure 7](#) shows the AS configuration scheme with multiple Cyclone FPGAs in the chain. In AS configuration mode, all the devices in the chain must be Cyclone devices.

**Figure 7. Multiple Devices in AS Mode**



**Notes to Figure 7:**

- (1)  $V_{CC} = 3.3\text{ V}$ .
- (2) In AS mode, the first Cyclone device in the chain is the master device. The other Cyclone devices in the chain are slave devices and must be in passive serial (PS) configuration mode.
- (3) Serial configuration devices cannot be cascaded.
- (4) Set MSEL0 to 0 and MSEL1 to 0 to select AS mode in the Cyclone device.
- (5) Set MSEL0 to 0 and MSEL1 to 1 to select PS mode in the Cyclone device.

[Figure 8](#) shows the timing waveform for Cyclone FPGA AS configuration scheme using a serial configuration device.

**Figure 8. AS Configuration Timing**

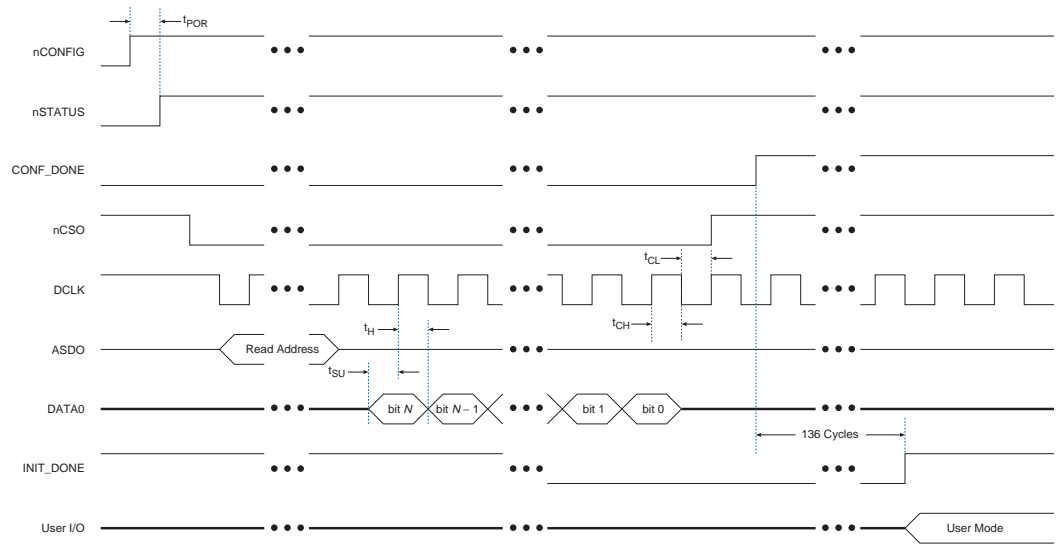


Table 6 shows the timing parameters for AS configuration mode.

<b>Table 6. Timing Parameters for AS Configuration</b>					
<b>Symbol</b>	<b>Parameter</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>
$f_{CLK}$	DCLK frequency (from Cyclone FPGA)		15	20	MHz
$t_{CH}$	DCLK high time	25			ns
$t_{CL}$	DCLK low time	25			ns
$t_H$	Data hold time after rising edge on DCLK	0			ns
$t_{SU}$	Data set up time before rising edge on DCLK	5			ns
$t_{POR}$	POR delay			100	ms

## Power & Operation

This section describes the power modes, power-on reset (POR) delay, error detection, and initial programming state of serial configuration devices.

### Power Mode

Serial configuration devices support active power and standby power modes. When  $nCS$  is low, the device is enabled and is in active power mode. The Cyclone FPGA is configured while in active power mode. When  $nCS$  is high, the device is disabled but could remain in active power mode until all internal cycles have completed (such as program or erase operations). The serial configuration device then goes into stand-by power mode. The  $I_{CC1}$  parameter specifies the  $V_{CC}$  supply current when the device is in active power mode and the  $I_{CC0}$  parameter specifies the current when the device is in stand-by power mode (see [Table 10](#)).

### Power-On Reset

During initial power-up, a POR delay occurs to help stabilize the system voltage levels. In AS configuration, the Cyclone FPGA controls the configuration and has a longer POR delay than the serial configuration device. Therefore, the POR delay is governed by the Cyclone FPGA (typically 100 ms).

### Error Detection

In AS configuration with the serial configuration device, the Cyclone FPGA monitors the configuration status through the  $nSTATUS$  and  $CONF\_DONE$  pins. If an error condition occurs ( $nSTATUS$  driven low) or if the  $CONF\_DONE$  pin does not go high, the Cyclone FPGA will initiate reconfiguration by pulsing the  $nSTATUS$  and  $nCSO$  signals, which controls the chip select pin on the serial configuration device ( $nCS$ ).

After an error, configuration automatically restarts if the *Auto-Restart Upon Frame Error* option is turned on in the Quartus II software.

## Operating Conditions

Tables 6 through 10 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for serial configuration devices.

**Table 7. Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Condition	Min	Max	Unit
$V_{CC}$	Supply voltage	With respect to ground	-0.6	4.0	V
$V_I$	DC input voltage	With respect to ground	-0.6	4.0	V
$I_{MAX}$	DC $V_{CC}$ or GND current			15	mA
$I_{OUT}$	DC output current per pin		-25	25	mA
$P_D$	Power dissipation			54	mW
$T_{STG}$	Storage temperature	No bias	-65	150	°C
$T_{AMB}$	Ambient temperature	Under bias	-65	135	°C
$T_J$	Junction temperature	Under bias		135	°C

**Table 8. Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply voltage	(2)	3.0	3.6	V
$V_I$	Input voltage	Respect to GND	-0.3	$0.3 + V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	V
$T_A$	Operating temperature	For commercial use	0	70	°C
		For industrial use	-40	85	°C
$t_R$	Input rise time			5	ns
$t_F$	Input fall time			5	ns

**Table 9. DC Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{IH}$	High-level input voltage		$0.7 \times V_{CC}$	$V_{CC} + 0.4$	V
$V_{IL}$	Low-level input voltage		-0.5	$0.3 \times V_{CC}$	V
$V_{OH}$	High-level output voltage	$I_{OH} = -100 \mu A$ (3)	$V_{CC} - 0.2$		V
$V_{OL}$	Low-level output voltage	$I_{OL} = 1.6 mA$ (3)		0.4	V
$I_I$	Input leakage current	$V_I = V_{CC}$ or GND	-10	10	$\mu A$
$I_{OZ}$	Tri-state output off-state current	$V_O = V_{CC}$ or GND	-10	10	$\mu A$

**Table 10.  $I_{CC}$  Supply Current**

Symbol	Parameter	Conditions	Min	Max	Unit
$I_{CC0}$	$V_{CC}$ supply current (standby)			50	$\mu\text{A}$
$I_{CC1}$	$V_{CC}$ supply current (during active power mode)		5	14	mA

**Table 11. Capacitance** *Note (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input pin capacitance	$V_{IN} = 0\text{ V}$		6	pF
$C_{OUT}$	Output pin capacitance	$V_{OUT} = 0\text{ V}$		8	pF

**Notes to Tables 7 – 11:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Maximum  $V_{CC}$  rise time is 100 ms.
- (3) The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current; the  $I_{OL}$  parameter refers to low-level TTL or CMOS output current.
- (4) Capacitance is sample-tested only at  $T_A = 25\text{ }^\circ\text{C}$  and at a 20-MHz frequency.

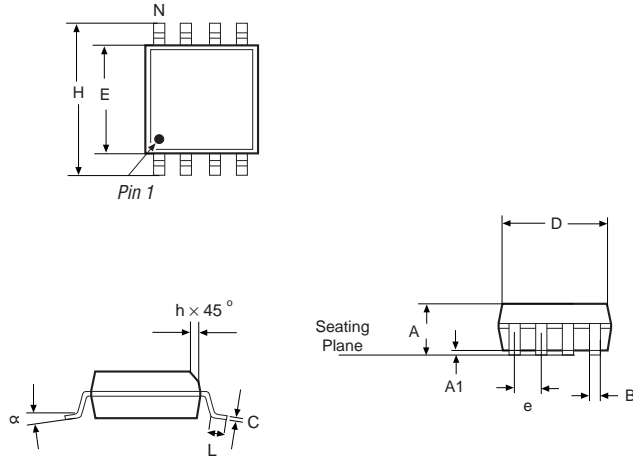
## Package

All serial configuration devices are available in 8-pin plastic SOIC package. [Figure 9](#) shows the mechanical drawing and specifications for this package.



For more information on Altera device packaging, see the *Altera Device Package Information Data Sheet*.

**Figure 9. 8-Pin SOIC Serial Configuration Device Package** Notes (1), (2)



Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	—	1.35	1.75
A1	—	0.10	0.25
B	—	0.33	0.51
C	—	0.19	0.25
D	—	4.80	5.00
E	—	3.80	4.00
e	1.27 BSC		
H	—	5.80	6.20
h	—	0.25	0.50
L	—	0.40	0.90
N	8		
$\alpha$	—	0 °C	8 °C

**Notes to Figure 9:**

- (1) All dimensions and tolerances conform to ANSI Y14.5M - 1982.
- (2) JEDEC reference MS-013 option AE.

## Ordering Code

Table 12 shows the ordering codes for serial configuration devices.

Device	Ordering Code
EPCS1	EPCS1S18
EPCS4	EPCS4S18



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