

1, 2, 4, 6 and 8-Channel Low Capacitance ESD Protection Arrays

Features

- 1, 2, 4, 6 and 8 channels of ESD protection
- Provides ± 8 kV ESD protection on each channel per the IEC 61000-4-2 ESD requirements
- Low loading capacitance of 1.0pF typical
- Minimal capacitance change with temperature and voltage
- Channel I/O to GND capacitance difference of 0.02pF typical
- Channel I/O to I/O capacitance 0.8pF typical
- Zener diode protects supply rail and eliminates the need for external by-pass capacitors
- Each I/O pin can withstand over 1000 ESD strikes
- Available in SOT, SOIC and MSOP packages

Applications

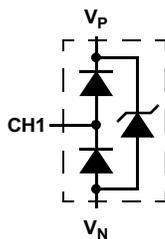
- USB2.0 ports at 480Mbps
- IEEE1394 Firewire® ports at 400Mbps / 800Mbps
- HDMI ports
- DVI ports
- Serial ATA ports
- General purpose high-speed data line ESD protection

Product Description

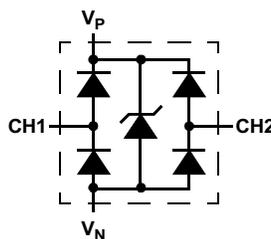
The CM1213 family of diode arrays has been designed to provide ESD protection for electronic components or sub-systems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail. A Zener diode is embedded between V_P and V_N , offering two advantages. First, it protects the V_{CC} rail against ESD strikes, and second, it eliminates the need for a bypass capacitor that would otherwise be needed for absorbing positive ESD strikes to ground. The CM1213 will protect against ESD pulses up to ± 8 kV per the IEC 61000-4-2 standard.

This device is particularly well-suited for protecting systems using high-speed ports such as USB2.0, IEEE1394 (Firewire®, iLink™), Serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

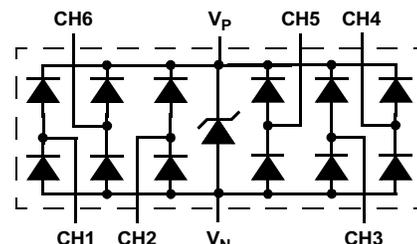
Electrical Schematics



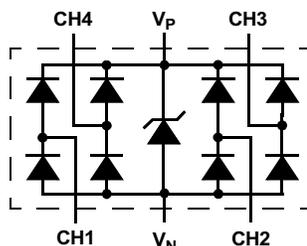
CM1213-01ST



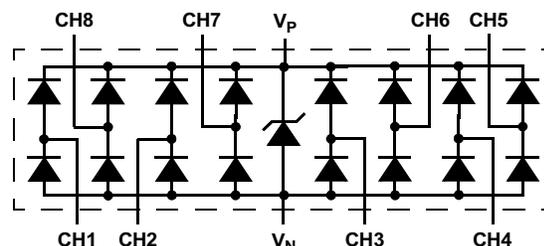
CM1213-02ST
CM1213-02SS



CM1213-06MS
CM1213-06SN

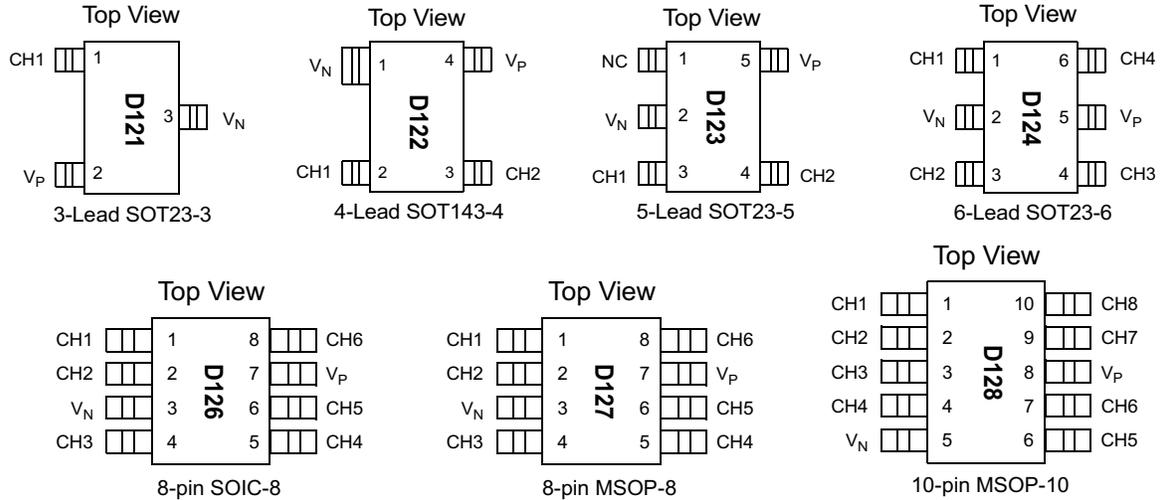


CM1213-04ST



CM1213-08MS

PACKAGE / PINOUT DIAGRAMS



Note: These drawings are not to scale.

1-CHANNEL SOT23-3 PACKAGE PIN DESCRIPTIONS

PIN	NAME	TYPE	DESCRIPTION
1	CH1	I/O	ESD Channel
2	V _P	PWR	Positive voltage supply rail
3	V _N	GND	Negative voltage supply rail

2-CHANNEL SOT23-5 PACKAGE PIN DESCRIPTIONS

PIN	NAME	TYPE	DESCRIPTION
1	NC		No connect
2	V _N	GND	Negative voltage supply rail
3	CH1	I/O	ESD Channel
4	CH2	I/O	ESD Channel
5	V _P	PWR	Positive voltage supply rail

4-CHANNEL SOT23-6 PACKAGE PIN DESCRIPTIONS

PIN	NAME	TYPE	DESCRIPTION
1	CH1	I/O	ESD Channel
2	V _N	GND	Negative voltage supply rail
3	CH2	I/O	ESD Channel
4	CH3	I/O	ESD Channel
5	V _P	PWR	Positive voltage supply rail
6	CH4	I/O	ESD Channel

2-CHANNEL SOT143-4 PACKAGE PIN DESCRIPTIONS

PIN	NAME	TYPE	DESCRIPTION
1	V _N	GND	Negative voltage supply rail
2	CH1	I/O	ESD Channel
3	CH2	I/O	ESD Channel
4	V _P	PWR	Positive voltage supply rail

6-CHANNEL MSOP-8/SOIC-8 PACKAGE PIN DESCRIPTIONS

PIN	NAME	TYPE	DESCRIPTION
1	CH1	I/O	ESD Channel
2	CH2	I/O	ESD Channel
3	V _N	GND	Negative voltage supply rail
4	CH3	I/O	ESD Channel
5	CH4	I/O	ESD Channel
6	CH5	I/O	ESD Channel
7	V _P	PWR	Positive voltage supply rail
8	CH6	I/O	ESD Channel

8-CHANNEL MSOP-10 PACKAGE PIN DESCRIPTIONS

PIN	NAME	TYPE	DESCRIPTION
1	CH1	I/O	ESD Channel
2	CH2	I/O	ESD Channel
3	CH3	I/O	ESD Channel
4	CH4	I/O	ESD Channel
5	V _N	GND	Negative voltage supply rail
6	CH5	I/O	ESD Channel
7	CH6	I/O	ESD Channel
8	V _P	PWR	Positive voltage supply rail
9	CH7	I/O	ESD Channel
10	CH8	I/O	ESD Channel

Ordering Information

PART NUMBERING INFORMATION				
# of Channels	Pins	Package	Ordering Part Number ¹	Part Marking
1	3	SOT23-3	CM1213-01ST	D121
2	4	SOT143-4	CM1213-02SS	D122
2	5	SOT23-5	CM1213-02ST	D123
4	6	SOT23-6	CM1213-04ST	D124
6	8	SOIC-8	CM1213-06SN	D126
6	8	MSOP-8	CM1213-06MS	D127
8	10	MSOP-10	CM1213-08MS	D128

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
Operating Supply Voltage ($V_P - V_N$)	6.0	V
Diode Forward DC Current (Note 1)	8	mA
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	($V_N - 0.5$) to ($V_P + 0.5$)	V

Note 1: Only one diode conducting at a time.

STANDARD OPERATING CONDITIONS		
PARAMETER	RATING	UNITS
Operating Temperature Range	-40 to +85	°C
Package Power Rating		
SOT23-3 Package (CM1213-01ST)	225	mW
SOT143-4 Package (CM1213-02SS)	225	mW
SOT23-5 Package (CM1213-02ST)	225	mW
SOT23-6 Package (CM1213-04ST)	225	mW
MSOP8 Package (CM1213-06MS)	400	mW
SOIC8 Package (CM1213-06SN)	600	mW
MSOP10 Package (CM1213-08MS)	400	mW

ELECTRICAL OPERATING CHARACTERISTICS¹

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_P	Operating Supply Voltage (V_P-V_N)	V_P-V_N		3.3	5.5	V
I_P	Operating Supply Current	$(V_P-V_N)=3.3V$			8.0	μA
V_F	Diode Forward Voltage Top Diode Bottom Diode	$I_F = 8mA$	0.60 0.60	0.80 0.80	0.95 0.95	V V
I_{LEAK}	Channel Leakage Current	$T_A=25^\circ C$		± 0.1	± 1.0	μA
C_{IN}	Channel Input Capacitance	At 1 MHz, $V_P=3.3V$, $V_N=0V$, $V_{IN}=1.65V$; Note 2 applies		1.0	1.5	pF
ΔC_{IN}	Channel I/O to GND capacitance difference			0.80		pF
V_{ESD}	ESD Protection Peak Discharge Voltage at any channel input, in system a) Contact discharge per IEC 61000-4-2 standard	Notes 2,3 and 5; $T_A=25^\circ C$	± 8			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	At 8kV ESD HBM; $T_A=25^\circ C$; Notes 2 & 4		+9.0 -9.0		V V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	$I_{IN} = 1A$; $T_A=25^\circ C$; Note 6		1.2 0.6		Ω Ω

Note 1: All parameters specified at $T_A = -40^\circ C$ to $+85^\circ C$ unless otherwise noted.

Note 2: These parameters guaranteed by design and characterization.

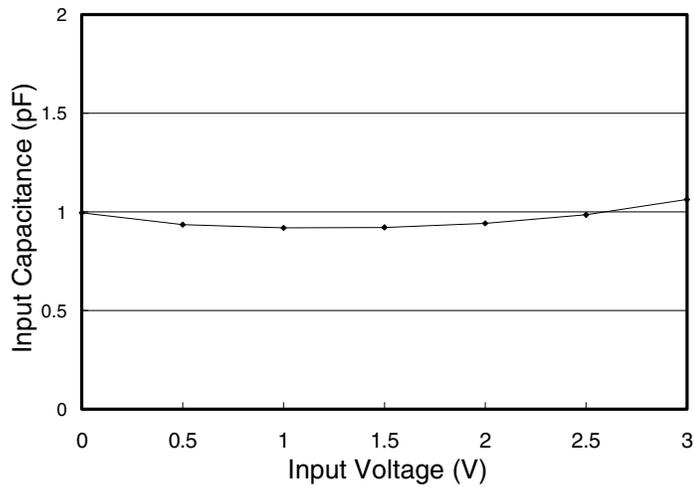
Note 3: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge} = 100pF$, $R_{Discharge} = 1.5K\Omega$, $V_P = 3.3V$, V_N grounded.

Note 4: Standard IEC 61000-4-2 with $C_{Discharge} = 150pF$, $R_{Discharge} = 330\Omega$, $V_P = 3.3V$, V_N grounded.

Note 5: These measurements performed with no external capacitor on V_P .

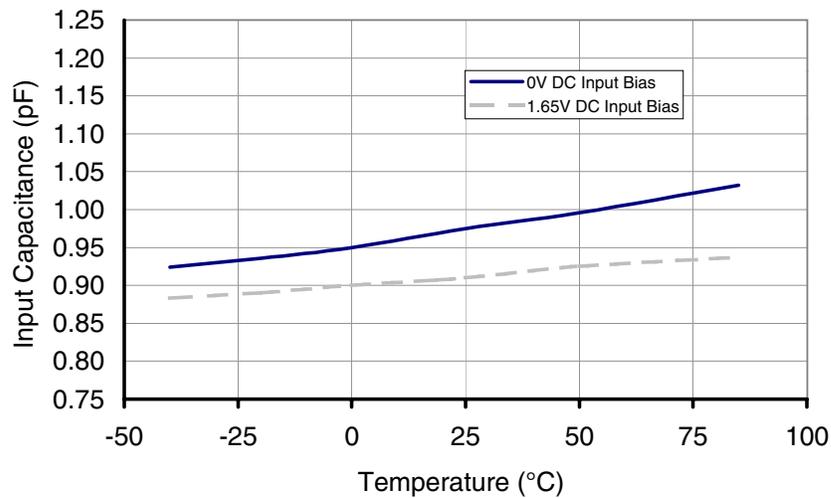
Performance Information

Input Channel Capacitance Performance Curves



Typical Variation of C_{IN} vs. V_{IN}

($f=1\text{MHz}$, $V_P = 3.3\text{V}$, $V_N = 0\text{V}$, $0.1\ \mu\text{F}$ chip capacitor between V_P and V_N , 25°C)



Typical Variation of C_{IN} vs. Temp

($f=1\text{MHz}$, $V_{IN}=30\text{mV}$, $V_P = 3.3\text{V}$, $V_N = 0\text{V}$, $0.1\ \mu\text{F}$ chip capacitor between V_P and V_N)

Performance Information (Cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

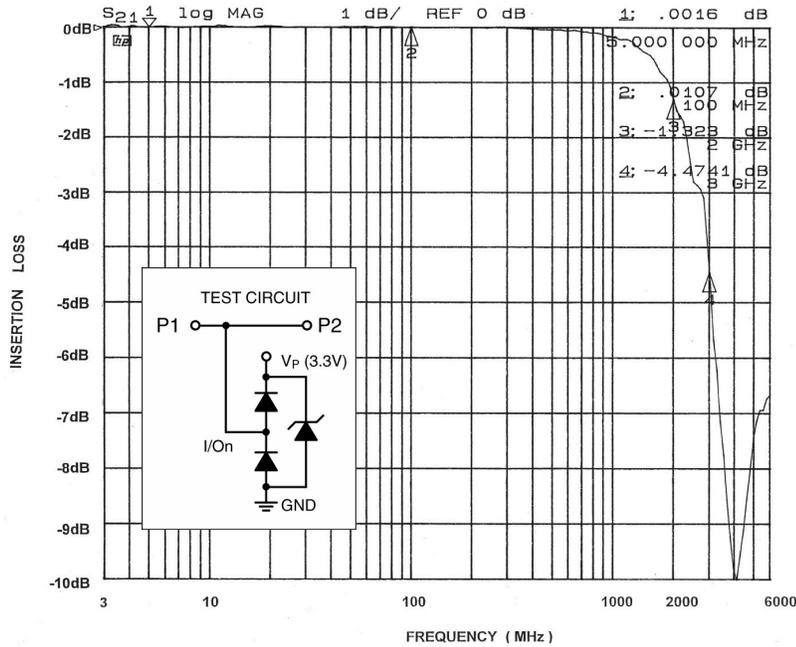


Figure 1. Insertion Loss (S21) VS. Frequency (0V DC Bias, $V_P=3.3V$)

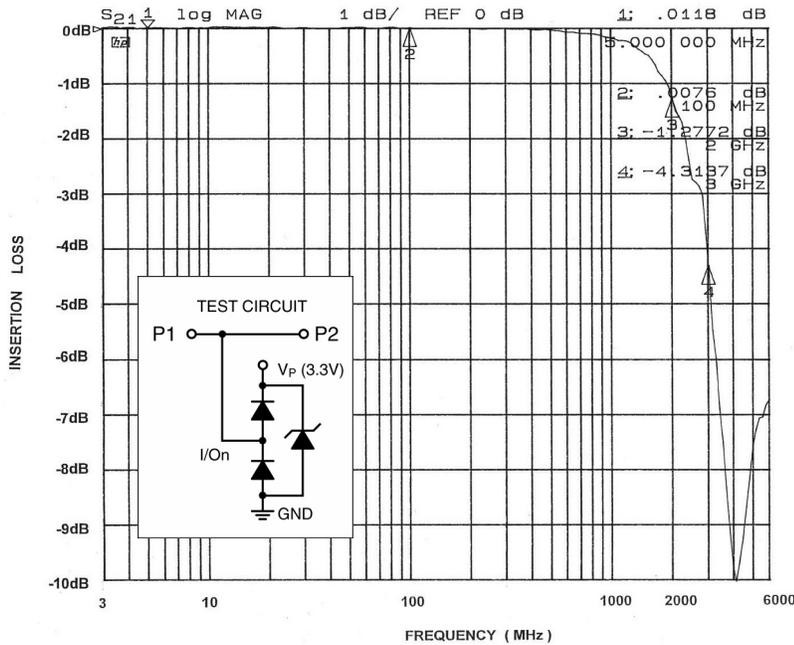


Figure 2. Insertion Loss (S21) VS. Frequency (2.5V DC Bias, $V_P=3.3V$)

Application Information

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to [Figure 3](#), which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L_1 and L_2 . The clamp voltage V_{CL} on the line being protected is:

$$V_{CL} = L_1 \times d(I_{ESD})/dt + V_{FD1} + L_2 \times d(I_{ESD})/dt + V_{CC}$$

where I_{ESD} is the ESD current pulse, V_{FD1} is the forward voltage of D_1 and V_{CC} is the positive supply voltage.

An ESD current pulse can increase from zero to its peak value in a very short time. As an example, an $\pm 8\text{kV}$ contact discharge per the IEC61000-4-2 standard results in a current pulse that increases from zero to 25 Amps in 1ns. Here $d(I_{ESD})/dt$ can be approximated to $\Delta I_{ESD}/\Delta t$, or $25/(1 \times 10^{-9})$ or 25×10^9 . So just 10nH of series inductance (L_1 and L_2 combined) will contribute to a 250V increment in V_{CL} ! A short length pf PCB trace can easily contribute 10nH of inductance.

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will contribute to drastically increased negative voltage on the line being protected.

Another consideration is the output impedance of the power supply when dealing with fast transient currents.

Most power supplies exhibit a high output impedance to fast transient current spikes. In the V_{CL} equation above, the V_{CC} term, in reality, is given by $(V_{DC} + I_{ESD} \times R_{OUT})$, where V_{DC} and R_{OUT} are the nominal supply DC output voltage and effective output impedance of the power supply respectively. As an example, a R_{OUT} of 1 ohm would result in a 10V increment in V_{CL} for a peak I_{ESD} of 10A.

The embedded Zener diode typically eliminates the need for an external bypass capacitor. This is because during a positive ESD strike, the ESD current flows through D_1 , through the Zener diode and then to ground. However, to achieve maximum performance and minimum clamping voltage of the ESD network, it is recommended that a $0.22\mu\text{F}$ capacitor be applied directly and in very close proximity to the V_P and V_N pins of the device as shown in Figure 3. This is especially useful when V_{CC} is less than 4V.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. There should be minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See also California Micro Devices Application Notes AP209, "Design Considerations for ESD Protection" or visit www.calmicro.com.

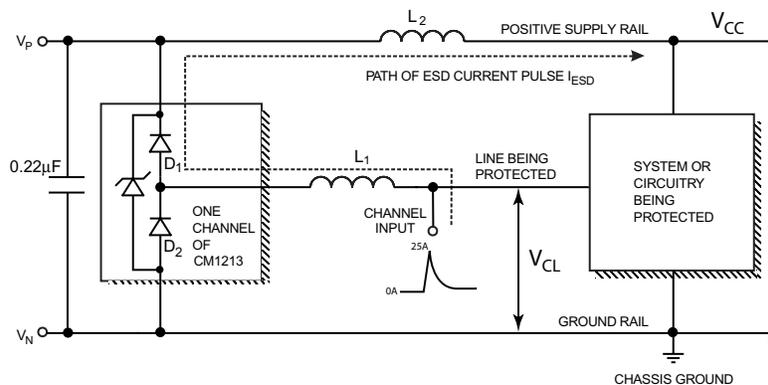


Figure 3. Application of Positive ESD Pulse between Input Channel and Ground

Mechanical Details

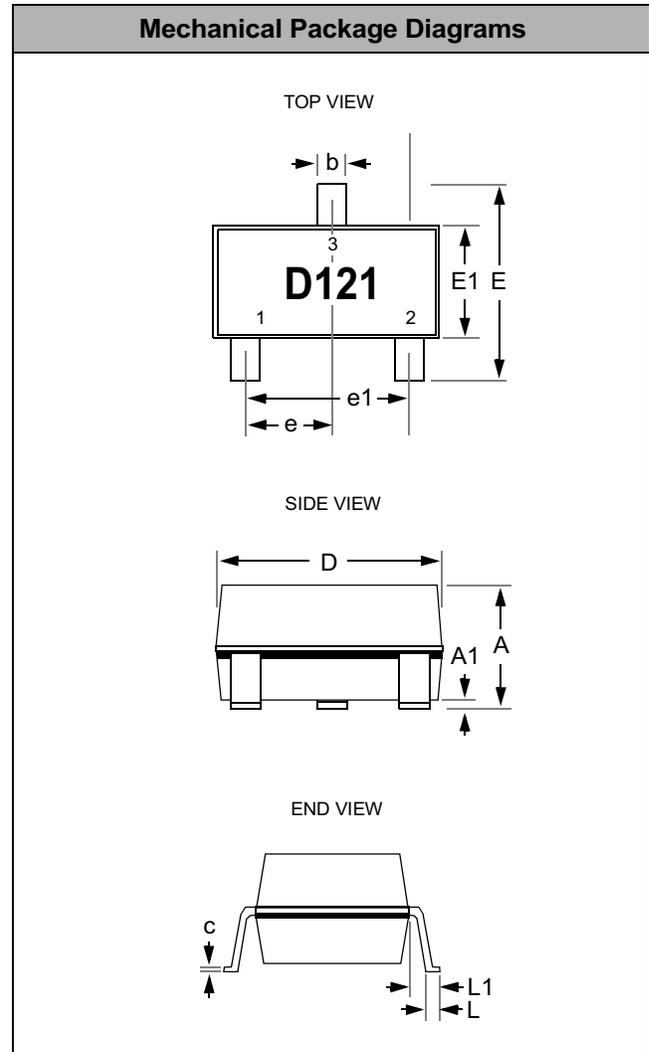
The CM1213 is available in SOT23-3, SOT143-4, SOT23-5, SOT23-6, MSOP-8, SOIC-8 and MSOP-10 packages. The various package drawings are presented below.

SOT23-3 Mechanical Specifications

Dimensions for CM1213-01ST devices packaged in 3-pin SOT23 packages are presented below.

For complete information on the SOT23-3 package, see the California Micro Devices SOT23 Package Information document.

PACKAGE DIMENSIONS				
Package	SOT23-3 (JEDEC name is TO-236)			
Pins	3			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	0.89	1.12	0.0350	0.0441
A1	0.01	0.10	0.0004	0.0039
b	0.30	0.50	0.0118	0.0197
c	0.08	0.20	0.0031	0.0079
D	2.80	3.04	0.1102	0.1197
E	2.10	2.64	0.0827	0.1039
E1	1.20	1.40	0.0472	0.0551
e	0.95 BSC		0.0374 BSC	
e1	1.90 BSC		0.0748 BSC	
L	0.40	0.60	0.0157	0.0236
L1	0.54 REF		0.0213 REF	
# per tape and reel	3000 pieces			
Controlling dimension: millimeters				



Package Dimensions for SOT23-3.

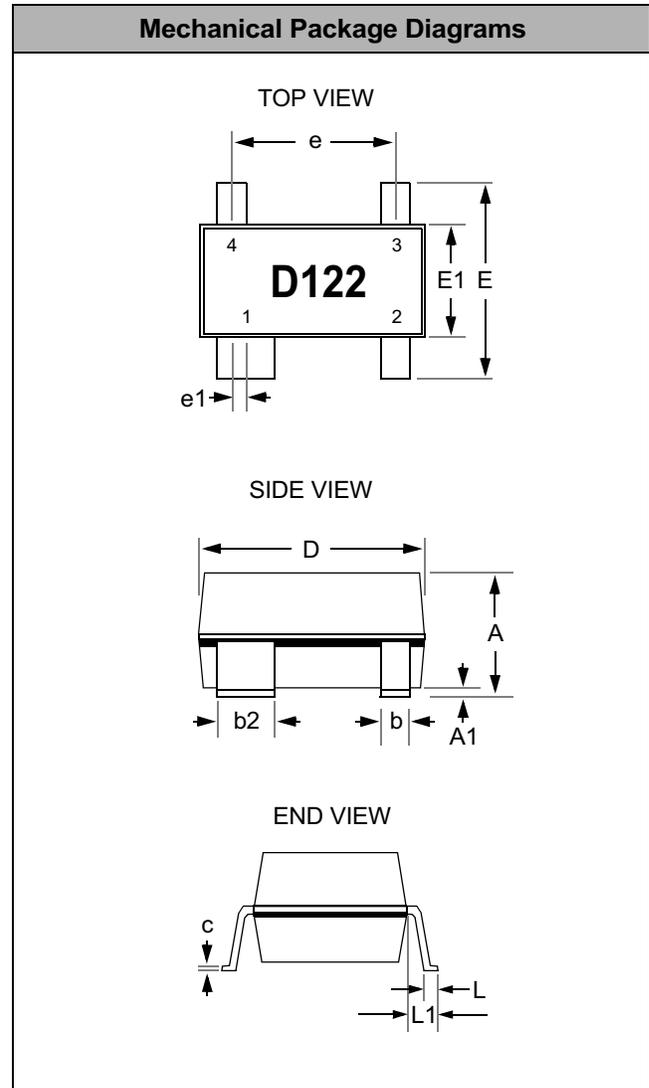
Mechanical Details (cont'd)

SOT143 Mechanical Specifications

Dimensions for CM1213-02SS devices packaged in 4-pin SOT143 packages are presented below.

For complete information on the SOT143 package, see the California Micro Devices SOT143 Package Information document.

PACKAGE DIMENSIONS				
Package	SOT143			
Pins	4			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.22	0.031	0.048
A1	0.05	0.15	0.002	0.006
b	0.30	0.50	0.012	0.019
b2	0.76	0.89	0.030	0.035
c	0.08	0.20	0.003	0.008
D	2.80	3.04	0.110	0.119
E	2.10	2.64	0.082	0.103
E1	1.20	1.40	0.047	0.055
e	1.92 BSC		0.075 BSC	
e1	0.20 BSC		0.008 BSC	
L	0.4	0.6	0.016	0.024
L1	0.54 REF		0.021 REF	
# per tape and reel	3000 pieces			
Controlling dimension: millimeters				



Package Dimensions for SOT143.

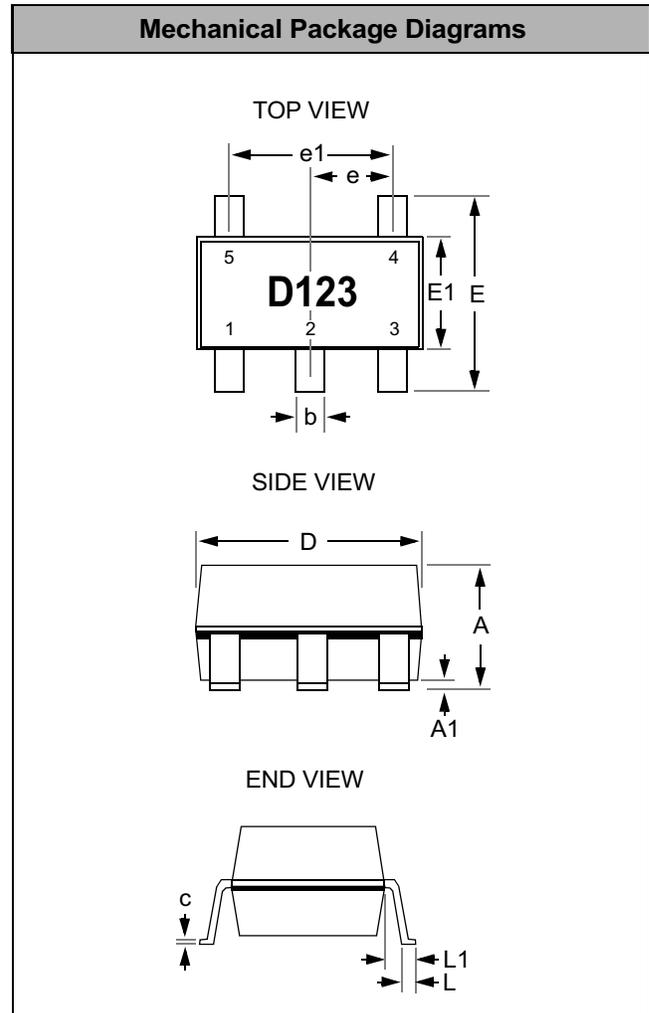
Mechanical Details (cont'd)

SOT23-5 Mechanical Specifications

Dimensions for CM1213-02ST devices packaged in 5-pin SOT23 packages are presented below.

For complete information on the SOT23-5 package, see the California Micro Devices SOT23 Package Information document.

PACKAGE DIMENSIONS				
Package	SOT23-5 (JEDEC name is MO-178)			
Pins	5			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	--	1.45	--	0.0571
A1	0.00	0.15	0.0000	0.0059
b	0.30	0.50	0.0118	0.0197
c	0.08	0.22	0.0031	0.0087
D	2.75	3.05	0.1083	0.1201
E	2.60	3.00	0.1024	0.1181
E1	1.45	1.75	0.0571	0.0689
e	0.95 BSC		0.0374 BSC	
e1	1.90 BSC		0.0748 BSC	
L	0.30	0.60	0.0118	0.0236
L1	0.60 REF		0.0236 REF	
# per tape and reel	3000 pieces			
Controlling dimension: millimeters				



Package Dimensions for SOT23-5.

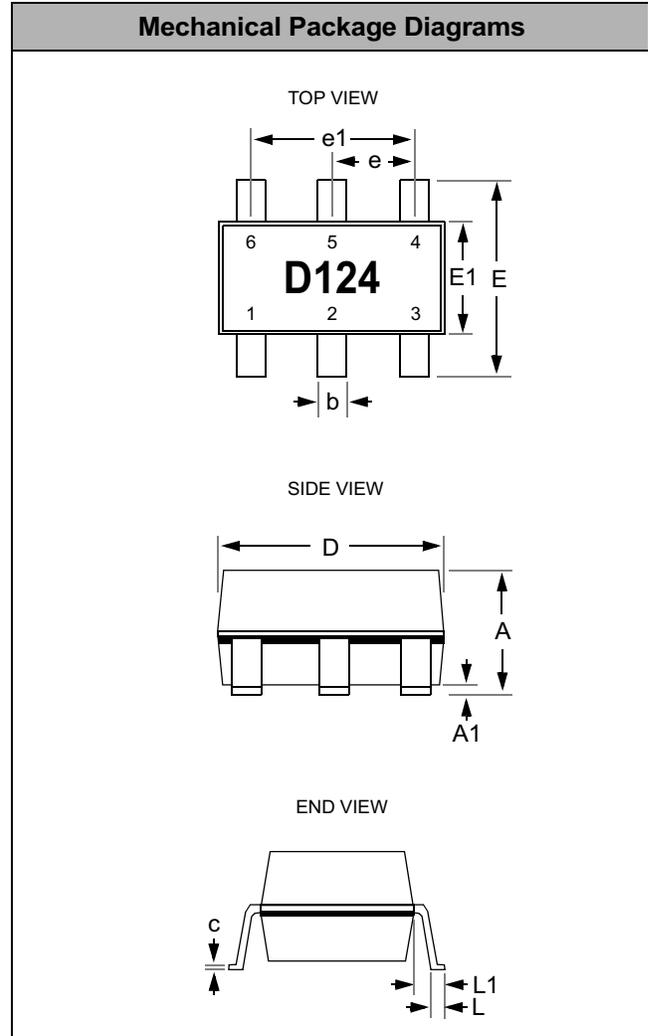
Mechanical Details (cont'd)

SOT23-6 Mechanical Specifications

CM1213-04ST devices are packaged in 6-pin SOT23 packages. Dimensions are presented below.

For complete information on the SOT23-6 package, see the California Micro Devices SOT23 Package Information document.

PACKAGE DIMENSIONS				
Package	SOT23-6 (JEDEC name is MO-178)			
Pins	6			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	--	1.45	--	0.0571
A1	0.00	0.15	0.0000	0.0059
b	0.30	0.50	0.0118	0.0197
c	0.08	0.22	0.0031	0.0087
D	2.75	3.05	0.1083	0.1201
E	2.60	3.00	0.1024	0.1181
E1	1.45	1.75	0.0571	0.0689
e	0.95 BSC		0.0374 BSC	
e1	1.90 BSC		0.0748 BSC	
L	0.30	0.60	0.0118	0.0236
L1	0.60 REF		0.0236 REF	
# per tape and reel	3000 pieces			
Controlling dimension: millimeters				



Package Dimensions for SOT23-6.



Mechanical Details

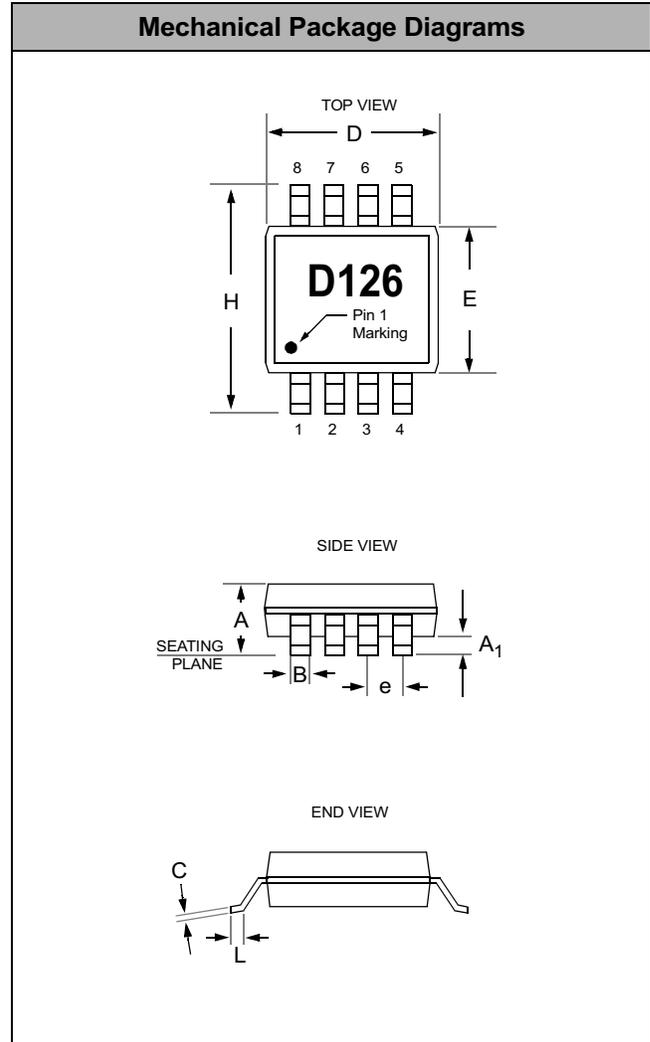
SOIC-8 Mechanical Specifications

Dimensions for CM1213-06SN devices packaged in 8-pin SOIC packages are presented below.

For complete information on the SOIC-8 package, see the California Micro Devices SOIC Package Information document.

PACKAGE DIMENSIONS				
Package	SOIC			
Pins	8			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.25	0.004	0.010
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.19	0.150	0.165
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.



Package Dimensions for SOIC-8

Mechanical Details

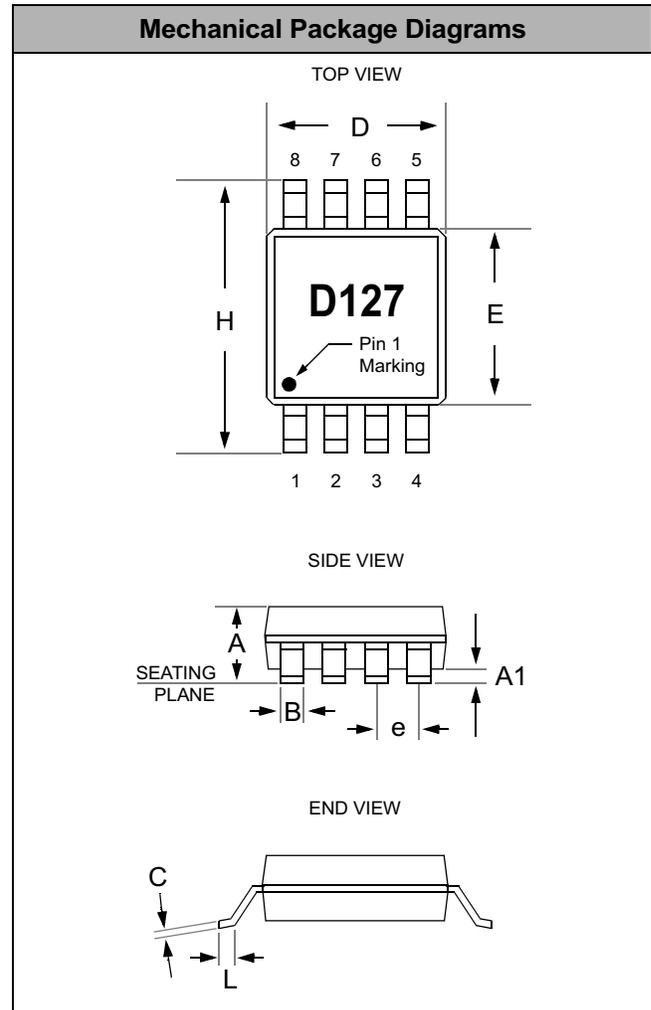
MSOP-8 Mechanical Specifications:

CM1213-06MS devices are packaged in 8-pin MSOP packages. Dimensions are presented below.

For complete information on the MSOP-8 package, see the California Micro Devices MSOP Package Information document.

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	8			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	0.87	1.17	0.034	0.046
A1	0.05	0.25	0.002	0.010
B	0.30 (typ)		0.012 (typ)	
C	0.18		0.007	
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.65 BSC		0.025 BSC	
H	4.78	4.98	0.188	0.196
L	0.52	0.54	0.017	0.025
# per tube	80 pieces*			
# per tape and reel	4000 pieces			
Controlling dimension: inches				

* This is an approximate amount which may vary.



Package Dimensions for MSOP-8

Mechanical Details (cont'd)

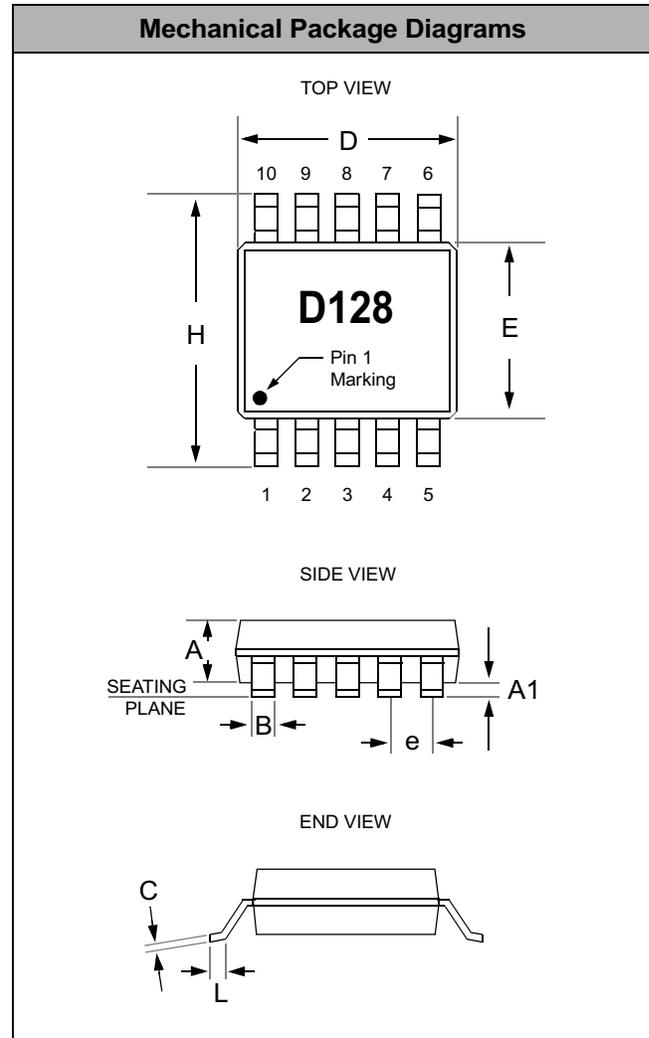
MSOP-10 Mechanical Specifications

CM1213-08MS devices are packaged in 10-pin MSOP packages. Dimensions are presented below.

For complete information on the MSOP-10 package, see the California Micro Devices MSOP Package Information document.

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	10			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	0.75	0.95	0.028	0.038
A1	0.05	0.15	0.002	0.006
B	0.18	0.40	0.006	0.016
C	0.18		0.007	
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.50 BSC		0.0196 BSC	
H	4.76	5.00	0.187	0.197
L	0.40	0.70	0.0137	0.029
# per tube	80 pieces*			
# per tape and reel	4000			
Controlling dimension: inches				

* This is an approximate number which may vary.



Package Dimensions for MSOP-10