1.1 Scope.

This specification covers the detail requirements for a monolithic dielectrically isolated CMOS switch, consisting of two independent single pole double throw switches.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	AD7512DIS(X)/883B
–2	AD7512DIT(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-14	14-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = 25°C unless otherwise noted)

V_{DD} to GND	+17V
V_{SS} to GND	–17V
Overvoltage at V_D (V_S)	
(1 second surge)	V_{DD} +25V or V_{SS} –25V
(Continuous)	V_{DD} +20V or V_{SS} –20V
Switch Current (I_{DS}, Continuous)	50mA
1ms Duration, 10% Duty Cycle	150mA
Digital Input Voltage Range	–0.3V to V_{DD} +0.3V
Power Dissipation	
Up to +75°C	450mW
Derate above +75°C	6mW/°C
Operating Temperature Range	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W
θ_{JA} = 120°C/W

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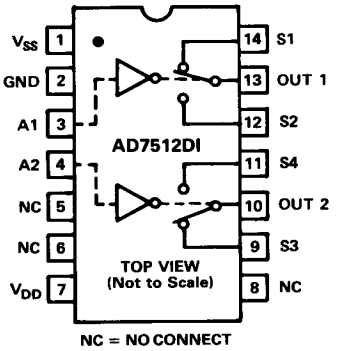
Table 1.

Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Switch "ON" Resistance	R_{ON}	−1, 2	175	100	175		$-10V \leq V_{OUT} \leq +10V$, $I_{DS} = 1mA$	Ω max
Leakage Current, Switch Open	I_S	−1, 2	200		200	3	$V_{OUT} = -10V$, $V_S = +10V$ and $V_{OUT} = +10V$, $V_S = -10V$	± nA max
Difference Between Output[2] and Input Current	I_{OUT}–I_S	−1, 2	600		600	9	$V_{OUT} = -10V$, $V_S = +10V$ and $V_{OUT} = +10V$, $V_S = -10V$	± nA max
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8			V max
Digital Input High Voltage	V_{IH}	−1 −2	3.0 2.4	3.0 2.4	3.0 2.4			V min V min
Input Leakage Current[3]	I_{IN}	−1, 2	10	10			$V_{IN} = 0V$ or V_{DD}	± nA max
Enable to Switch "ON"[3]	t_{ON}	−1, 2	1.0				$V_{IN} = 0$ to +3V and +3V to 0V	μs max
Enable to Switch "OFF"[3]	t_{OFF}	−1, 2	1.0					μs max
Supply Current from V_{DD}	I_{DD}	−1, 2	800 500	800 500	800 500		All Digital Inputs = V_{IH} All Digital Inputs = V_{IL}	μA max μA max
Supply Current from V_{SS}	I_{SS}	−1, 2	800 500	800 500	800 500		All Digital Inputs = V_{IH} All Digital Inputs = V_{IL}	μA max μA max

NOTES
[1]$V_{DD} = +15V$; $V_{SS} = -15V$ unless otherwise stated.
[2]This is the leakage current flowing in the OUT terminal with 20V across the S terminals.
[3]These design limits are at +25°C only.

3.2.1 Functional Block Diagram and Terminal Assignments.



AD7512DI: Address "HIGH" makes S1 to OUT 1 and S3 to OUT 2.

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (82).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).