



# 512Kx8 Monolithic SRAM CMOS

## FEATURES

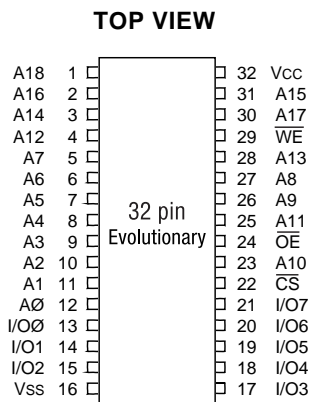
- 512Kx8 bit CMOS Static
- Random Access Memory
  - Access Times of 70, 85, 100ns
  - Data Retention Function (LP version)
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- 32 lead JEDEC Approved Evolutionary Pinout
  - Ceramic Sidebrazed 600 mil DIP (Package 9)
  - Ceramic SOJ (Package 140)
- Single +5V (±10%) Supply Operation

The EDI88512C is a 4 megabit Monolithic CMOS Static RAM.

The 32 pin DIP pinout adheres to the JEDEC evolutionary standard for the four megabit device. Both the DIP and CSOJ packages are pin for pin upgrades for the single chip enable 128K x 8, the EDI88128C. Pins 1 and 30 become the higher order addresses.

A Low Power version with Data Retention (EDI88512LP) is also available for battery backed applications. Military product is available compliant to Appendix A of MIL-PRF-38535.

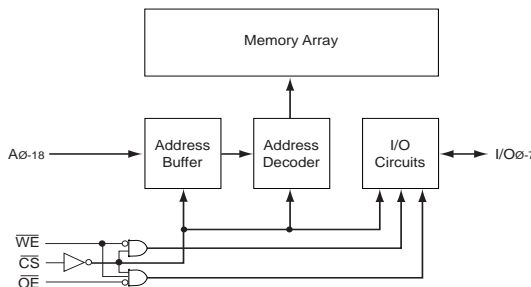
FIG. 1 PIN CONFIGURATION



## PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}$	Write Enables
$\overline{CS}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power (+5V ±10%)
Vss	Ground
NC	Not Connected

## BLOCK DIAGRAM





**ABSOLUTE MAXIMUM RATINGS**

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature TA (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1	W
Output Current	20	mA
Junction Temperature, TJ	175	°C

**NOTE:**

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**TRUTH TABLE**

$\overline{OE}$	$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
X	H	X	Standby	High Z	Icc2, Icc3
H	L	H	Output Deselect	High Z	Icc1
L	L	H	Read	Data Out	Icc1
X	L	L	Write	Data In	Icc1

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Supply Voltage	Vss	0	0	0	V
Input High Voltage	VIH	2.2	—	Vcc +0.5	V
Input Low Voltage	VIL	-0.3	—	+0.8	V

**CAPACITANCE**

(TA = +25°C)

Parameter	Symbol	Condition	Max	Unit
Address Lines	CI	VIN = Vcc or Vss, f = 1.0MHz	12	pF
Data Lines	Co	VOUT = Vcc or Vss, f = 1.0MHz	14	pF

These parameters are sampled, not 100% tested.

**DC CHARACTERISTICS**

(VCC = 5V, \*TA = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ*	Max	Units	
Input Leakage Current	II1	VIN = 0V to Vcc	—	—	±10	µA	
Output Leakage Current	ILO	VI/O = 0V to Vcc	—	—	±10	µA	
Operating Power Supply Current	Icc1	$\overline{WE}, \overline{CS} = V_{IL}, I_{I/O} = 0mA, \text{Min Cycle (70-100ns)}$	—	45	75	mA	
Standby (TTL) Power Supply Current	Icc2	$\overline{CS} \geq V_{IH}, V_{IN} \leq V_{IL}, V_{IN} \geq V_{IH}$	—	3	10	mA	
Full Standby Power Supply Current	Icc3	$\overline{CS} \geq V_{cc} - 0.2V$ $V_{IN} \geq V_{cc} - 0.2V \text{ or } V_{IN} \leq 0.2V$	C	—	—	5	mA
			LP	—	—	2	mA
Output Low Voltage	VO1	IOL = 2.1mA	—	—	0.4	V	
Output High Voltage	VOH	IOH = -1.0mA	2.4	—	—	V	

NOTE: DC test conditions: VIL = 0.3V, VIH = Vcc -0.3V

**AC TEST CONDITIONS**

Figure 1

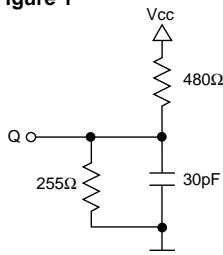
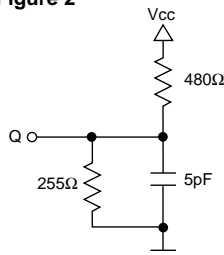


Figure 2



Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For tEHOZ, tEHOZ and tWLOZ, CL = 5pF Figure 2)



## AC CHARACTERISTICS – READ CYCLE

(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0°C to +70°C)

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	70		85		100		ns
Address Access Time	tAVQV	tAA		70		85		100	ns
Chip Enable Access Time	tELQV	tACS		70		85		100	ns
Chip Enable to Output in Low Z (1)	tELQX	tCLZ	10		10		10		ns
Chip Disable to Output in High Z (1)	tEHQZ	tCHZ		25		30		30	ns
Output Hold from Address Change	tAVQX	tOH	10		10		10		ns
Output Enable to Output Valid	tGLQV	tOE		35		45		50	ns
Output Enable to Output in Low Z (1)	tGLQX	tOLZ	5		5		5		ns
Output Disable to Output in High Z(1)	tGHQZ	tOHZ	0	25	0	30	0	30	ns

1. This parameter is guaranteed by design but not tested.

## AC CHARACTERISTICS – WRITE CYCLE

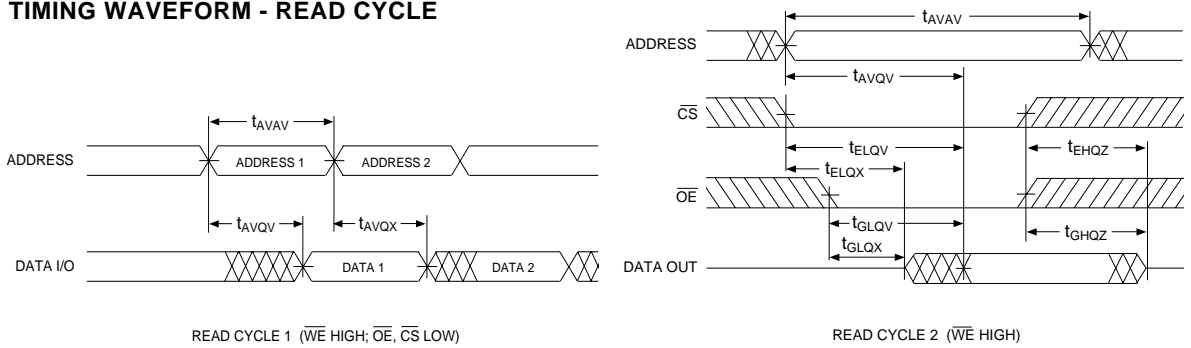
(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0°C to +70°C)

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	70		85		100		ns
Chip Enable to End of Write	tELWH	tCW	60		70		80		ns
	tELEH	tCW	60		70		80		ns
Address Setup Time	tAVWL	tAS	0		0		0		ns
	tAVEL	tAS	0		0		0		ns
Address Valid to End of Write	tAVWH	tAW	65		70		80		ns
	tAVEH	tAW	65		70		80		ns
Write Pulse Width	tWLWH	tWP	50		55		60		ns
	tWLEH	tWP	50		55		60		ns
Write Recovery Time	tWHAX	tWR	0		0		0		ns
	tEHAX	tWR	0		0		0		ns
Data Hold Time	tWHDX	tDH	0		0		0		ns
	tEHDX	tDH	0		0		0		ns
Write to Output in High Z (1)	tWLQZ	tWHZ	0	25	0	30	0	30	ns
Data to Write Time	tDVWH	tDW	40		40		40		ns
	tDVEH	tDW	30		35		40		ns
Output Active from End of Write (1)	tWHQX	tWLZ	5		5		5		ns

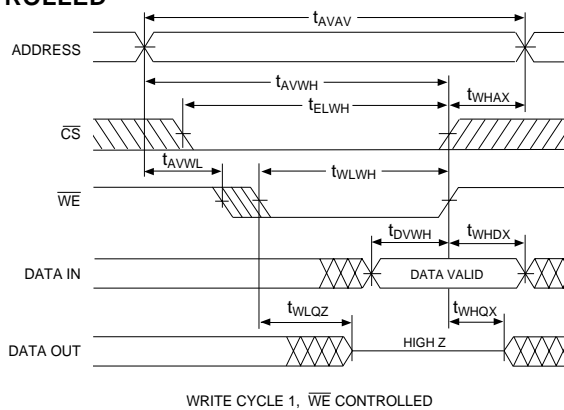
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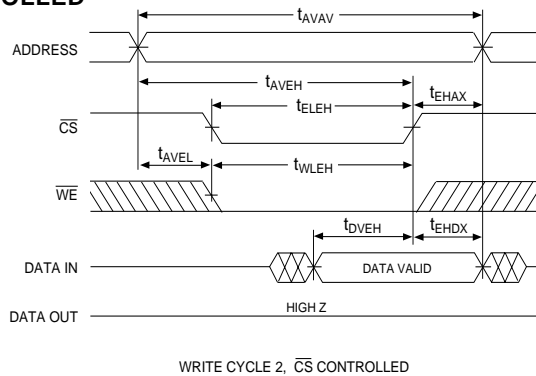
**FIG. 2**  
**TIMING WAVEFORM - READ CYCLE**



**FIG. 3**  
**WRITE CYCLE -  $\overline{WE}$  CONTROLLED**



**FIG. 4**  
**WRITE CYCLE -  $\overline{CS}$  CONTROLLED**

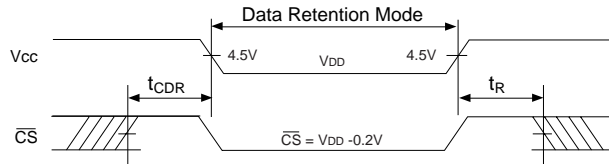




**DATA RETENTION CHARACTERISTICS (EDI88512LP ONLY)**  
(TA = -55°C to +125°C)

Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V <sub>DD</sub>	V <sub>DD</sub> = 2.0V	2	–	–	V
Data Retention Quiescent Current	I <sub>CCDR</sub>	$\overline{CS} \geq V_{DD} - 0.2V$	–	–	185	μA
Chip Disable to Data Retention Time	T <sub>CDR</sub>	V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V	0	–	–	ns
Operation Recovery Time	T <sub>R</sub>	or V <sub>IN</sub> ≤ 0.2V	T <sub>AVAV</sub>	–	–	ns

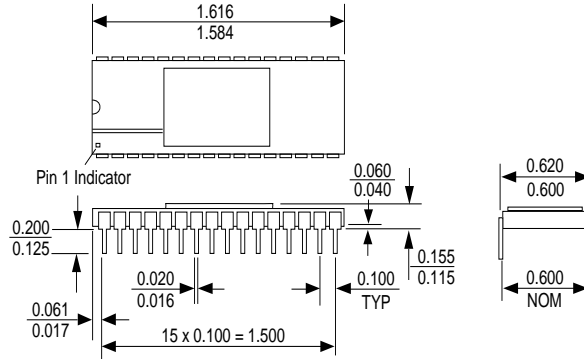
**FIG. 5**  
**DATA RETENTION -  $\overline{CS}$  CONTROLLED**



DATA RETENTION,  $\overline{CS}$  CONTROLLED

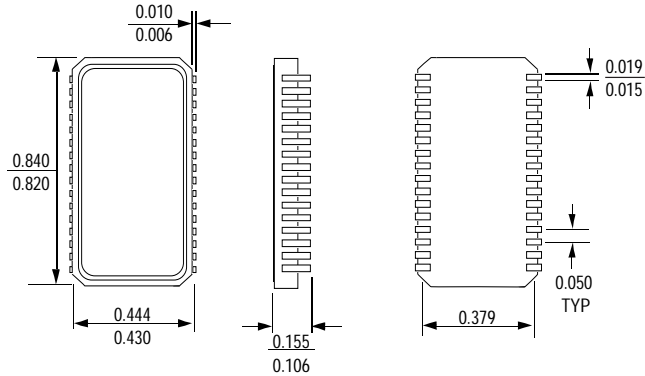


**PACKAGE 9: 32 LEAD SIDEBRAZED CERAMIC DIP**



ALL DIMENSIONS ARE IN INCHES

**PACKAGE 140: 32 LEAD CERAMIC SOJ**



ALL DIMENSIONS ARE IN INCHES



### ORDERING INFORMATION

**EDI 8 8 512 C X X X**

**WHITE ELECTRONIC DESIGNS** \_\_\_\_\_

**SRAM** \_\_\_\_\_

**ORGANIZATION, 512Kx8** \_\_\_\_\_

**TECHNOLOGY:** \_\_\_\_\_

C = CMOS Standard Power

LP = Low Power

**ACCESS TIME (ns)** \_\_\_\_\_

**PACKAGE TYPE:** \_\_\_\_\_

C = 32 lead Sidebraced DIP, 600 mil (Package 9)

N = 32 lead Ceramic SOJ (Package 140)

**DEVICE GRADE:** \_\_\_\_\_

B = MIL-STD-883 Compliant

M = Military Screened      -55°C to +125°C

I = Industrial                -40°C to +85°C

C = Commercial              0°C to +70°C