

## FDS6990A

### Dual N-Channel Logic Level PowerTrench® MOSFET

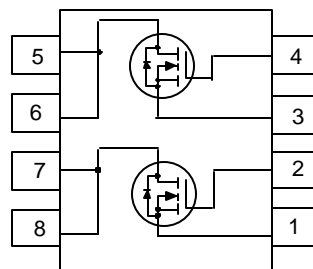
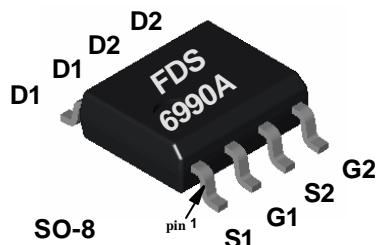
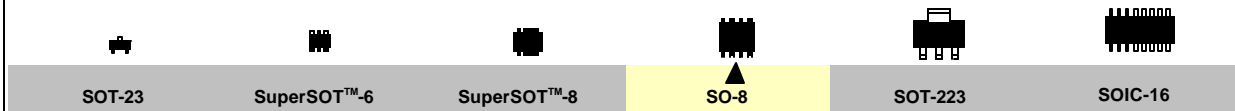
#### General Description

These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

#### Features

- 7.5 A, 30 V.  $R_{DS(ON)} = 0.018 \Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 0.023 \Omega @ V_{GS} = 4.5 \text{ V}$
- Fast switching speed.
- Low gate charge (typical 18nC).
- High performance trench technology for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.



#### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a) - Pulsed	7.5	A
		20	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	2	W
		1.6	
		0.9	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

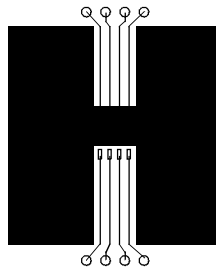
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

# Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		20		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V T <sub>J</sub> = 55°C			1 10	μA uA
I <sub>GSSF</sub>	Gate–Body Leakage, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate–Body Leakage, Reverse	V <sub>GS</sub> = - 20 V, V <sub>DS</sub> = 0 V			-100	nA
<b>ON CHARACTERISTICS</b> (Note 2)						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	1.5	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		-4		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.5 A T <sub>J</sub> = 125°C		0.015 0.022	0.018 0.031	Ω
I <sub>D(on)</sub>	On–State Drain Current	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 5 V	20			A
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 7.5 A		24		S
<b>DYNAMIC CHARACTERISTICS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		1650		pF
C <sub>oss</sub>	Output Capacitance			365		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			170		pF
R <sub>G</sub>	Gate Resistance	V <sub>GS</sub> = 15mV, f = 1.0 MHz		1.2		Ω
<b>SWITCHING CHARACTERISTICS</b> (Note 2)						
t <sub>d(on)</sub>	Turn–On Delay Time	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		11	20	ns
t <sub>r</sub>	Turn–On Rise Time			9	18	ns
t <sub>d(off)</sub>	Turn–Off Delay Time			25	40	ns
t <sub>f</sub>	Turn–Off Fall Time			11	20	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 7.5 A, V <sub>GS</sub> = 5 V		18	25	nC
Q <sub>gs</sub>	Gate–Source Charge			5.5		nC
Q <sub>gd</sub>	Gate–Drain Charge			6.7		nC
<b>DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
I <sub>S</sub>	Maximum Continuous Drain–Source Diode Forward Current				1.3	A
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.3 A (Note 2)			1.2	V

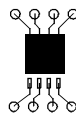
## Notes:

1. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.

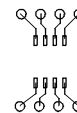


Scale 1 : 1 on letter size paper

a) 50°C/W when mounted on a 1in<sup>2</sup> pad of 2 oz copper



b) 105°C/W when mounted on a .04 in<sup>2</sup> pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

## Typical Electrical Characteristics

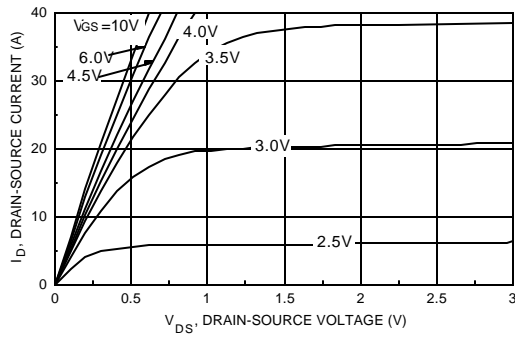


Figure 1. On-Region Characteristics.

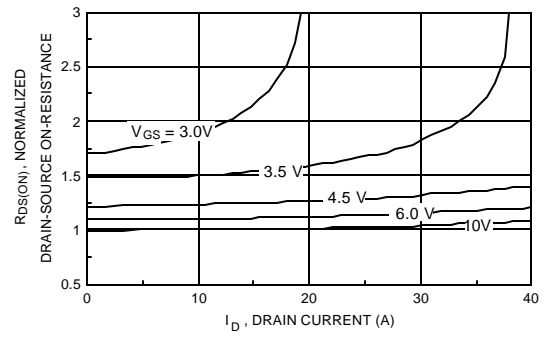


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

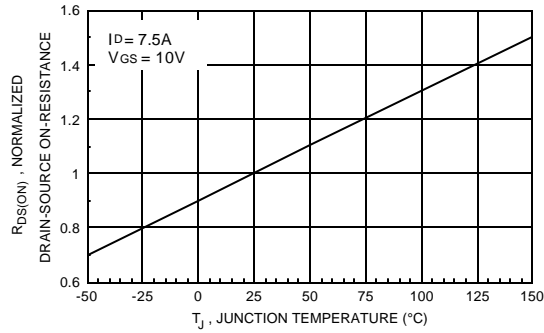


Figure 3. On-Resistance Variation with Temperature.

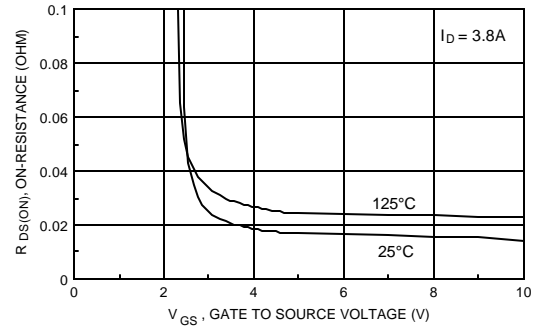


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

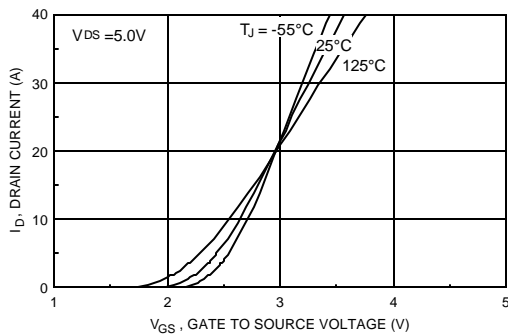


Figure 5. Transfer Characteristics.

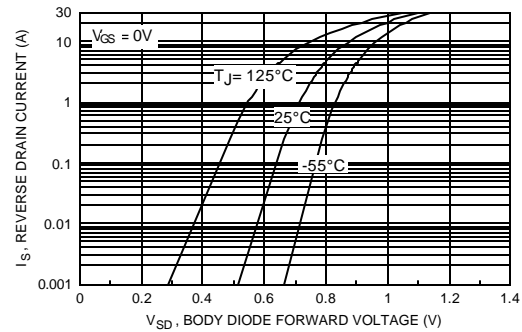


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical Characteristics

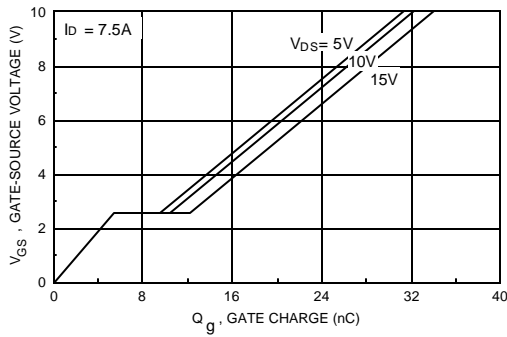


Figure 7. Gate Charge Characteristics.

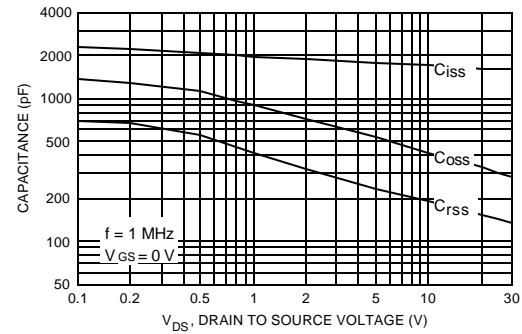


Figure 8. Capacitance Characteristics.

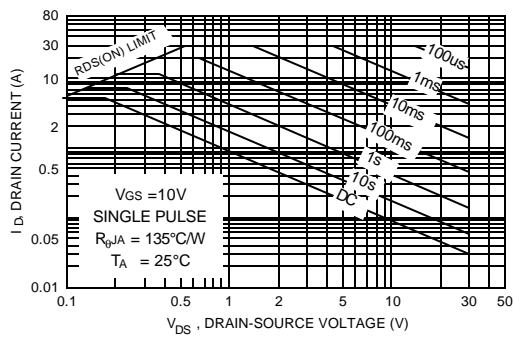


Figure 9. Maximum Safe Operating Area.

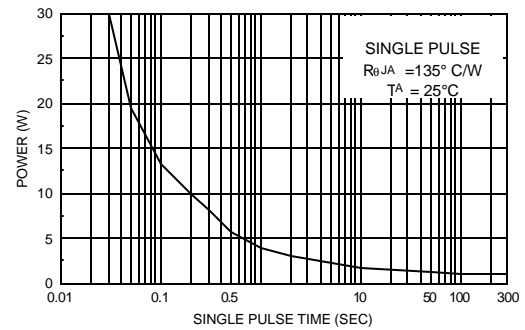


Figure 10. Single Pulse Maximum Power Dissipation.

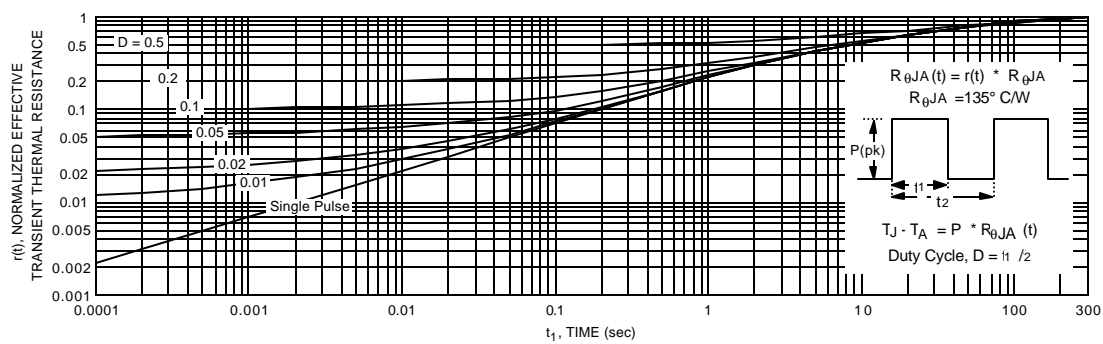


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.  
Transient thermal response will change depending on the circuit board design.

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