Integrated Device Technology, Inc.

3.3V CMOS STATIC RAM 1 MEG (64K x 16-BIT)

PRELIMINARY
IDT71V016

FEATURES:

- 64K x 16 advanced high-speed CMOS Static RAM
- Equal access and cycle times
  - — Commercial: 12/15/20/25ns
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Upper and Lower Byte Enable Pins
- Single 3.3V(±0.3V) power supply
- Available in 44-pin Plastic SOJ and 44-pin TSOP package

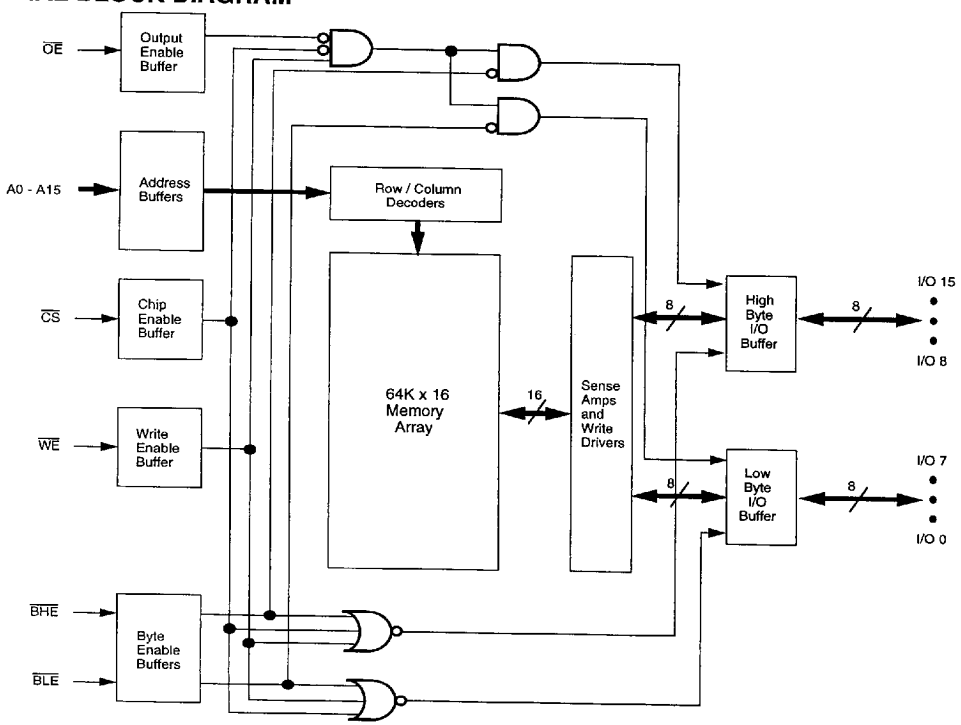
DESCRIPTION:

The IDT71V016 is a 1,048,576-bit high-speed Static RAM organized as 64K x 16. It is fabricated using IDT's high-perfomance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71V016 has an output enable pin which operates as fast as 7ns, with address access times as fast as 12ns. All bidirectional inputs and outputs of the IDT71V016 are TTL-compatible and operation is from a single 3.3V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

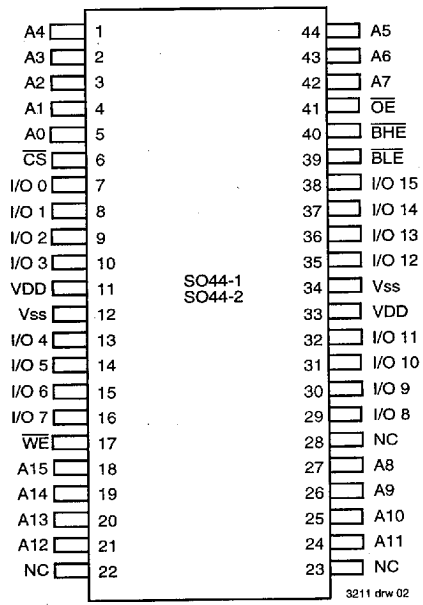
The IDT71V016 is packaged in a JEDEC standard 44-pin Plastic SOJ and 44-pin TSOP Type II.

FUNCTIONAL BLOCK DIAGRAM



3211 drw 01

PIN CONFIGURATIONS



SOJ/TSOP
TOP VIEW

PIN DESCRIPTIONS

$A_0 - A_{15}$	Address Inputs	Input
$\overline{CS}$	Chip Select	Input
$\overline{WE}$	Write Enable	Input
$\overline{OE}$	Output Enable	Input
$\overline{BHE}$	High Byte Enable	Input
$\overline{BLE}$	Low Byte Enable	Input
I/O_0 - I/O_{15}	Data Input/Output	I/O
V_{DD}	3.3V Power	Pwr
Vss	Ground	Gnd

3211 tbl 01

TRUTH TABLE(1)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0-I/O_7	I/O_8-I/O_{15}	Function
H	X	X	X	X	High-Z	High-Z	Deselected - Standby
L	L	H	L	H	$DATA_{OUT}$	High-Z	Low Byte Read
L	L	H	H	L	High-Z	$DATA_{OUT}$	High Byte Read
L	L	H	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Word Read
L	X	L	L	L	$DATA_{IN}$	$DATA_{IN}$	Word Write
L	X	L	L	H	$DATA_{IN}$	High-Z	Low Byte Write
L	X	L	H	L	High-Z	$DATA_{IN}$	High Byte Write
L	H	H	X	X	High-Z	High-Z	Outputs Disabled
L	X	X	H	H	High-Z	High-Z	Outputs Disabled

3211 tbl 02

NOTE:
1.H = V_{IH}, L = V_{IL}, X = Don't care.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc+0.5V	V
T_A	OperatingTemperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

3211 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. Input, Output,and I/O terminals; 4.6V maximum.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	V_{DD}
Commercial	0°C to +70°C	0V	3.3V ± 0.3V

3211 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	4.6	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

3211 tbl 05

NOTE:
1. V_{IL} (min.) = –1.5V for pulse width less than tRC/2, once per cycle.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

3211 tbl 06

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V ± 0.3V, Commercial Temperature Range

Symbol	Parameter	Test Condition	IDT71V016 Min.	IDT71V016 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = GND to V_{DD}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{DD} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{DD}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{DD} = Min.	2.4	—	V

3211 tbl 07

DC ELECTRICAL CHARACTERISTICS(1)

(V_{DD} = 3.3V ± 0.3V, V_{LC} = 0.2V, V_{HC} = V_{DD}–0.2V)

Symbol	Parameter	71V016S12(3) Com'l.	71V016S12(3) Mil.	71V016S15 Com'l.	71V016S15 Mil.	71V016S20 Com'l.	71V016S20 Mil.	71V016S25 Com'l.	71V016S25 Mil.	Unit
I_{CC}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{DD} = Max., f = f_{MAX}(2)	150	—	130	—	120	—	110	—	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, Outputs Open, V_{DD} = Max., f = f_{MAX}(2)	45	—	35	—	30	—	25	—	mA
I_{SB1}	Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, Outputs Open, V_{DD} = Max., f = 0(2) $V_{IN} \le V_{LC}$ or $V_{IN} \ge V_{HC}$	5	—	5	—	5	—	5	—	mA

3211 tbl 08

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/tRC (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.
3. 12ns specification is preliminary.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1.5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

3211 tbl 09

AC TEST LOADS

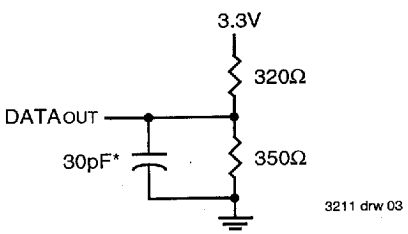
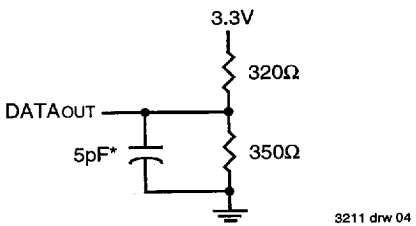


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

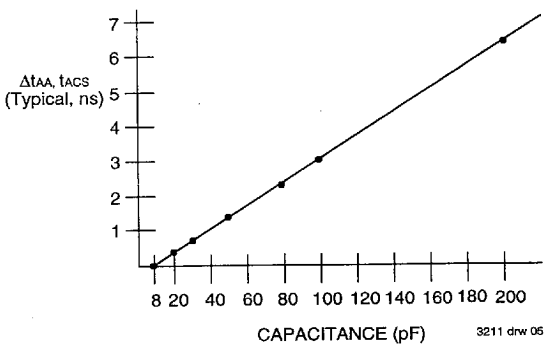


Figure 3. Output Capacitive Derating

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V ± 0.3V, Commercial Temperature Range)

Symbol	Parameter	71V016S12[2]		71V016S15		71V016S20		71V016S25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	12	—	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	20	—	25	ns
t_{CLZ}[1]	Chip Select Low to Output in Low-Z	4	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Select High to Output in High-Z	—	6	—	6	—	8	—	8	ns
t_{OE}	Output Enable Low to Output Valid	—	7	—	8	—	10	—	12	ns
t_{OLZ}[1]	Output Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Enable High to Output in High-Z	—	6	—	6	—	8	—	8	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	5	—	5	—	ns
t_{BE}	Byte Enable Low to Output Valid	—	7	—	8	—	10	—	12	ns
t_{BLZ}[1]	Byte Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{BHZ}[1]	Byte Enable High to Output in High-Z	—	6	—	6	—	8	—	8	ns
Write Cycle										
t_{WC}	Write Cycle Time	12	—	15	—	20	—	25	—	ns
t_{AW}	Address Valid to End of Write	9	—	10	—	12	—	14	—	ns
t_{CW}	Chip Select Low to End of Write	9	—	10	—	12	—	14	—	ns
t_{BW}	Byte Enable Low to End of Write	9	—	10	—	12	—	14	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Address Hold from End of Write	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	9	—	10	—	12	—	14	—	ns
t_{DW}	Data Valid to End of Write	7	—	8	—	10	—	10	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Write Enable High to Output in Low-Z	1	—	1	—	1	—	1	—	ns
t_{WHZ}[1]	Write Enable Low to Output in High-Z	—	6	—	6	—	8	—	8	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. 12ns specification is preliminary.

3211 tbl 10

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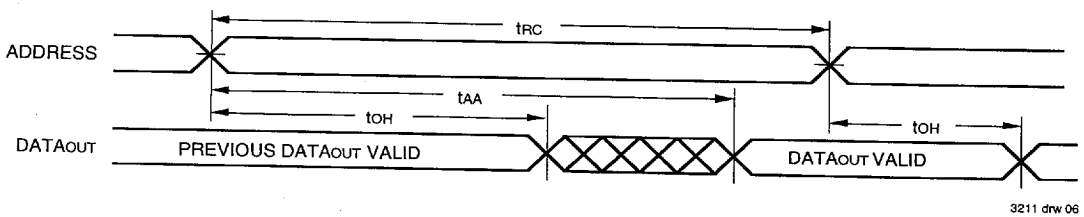
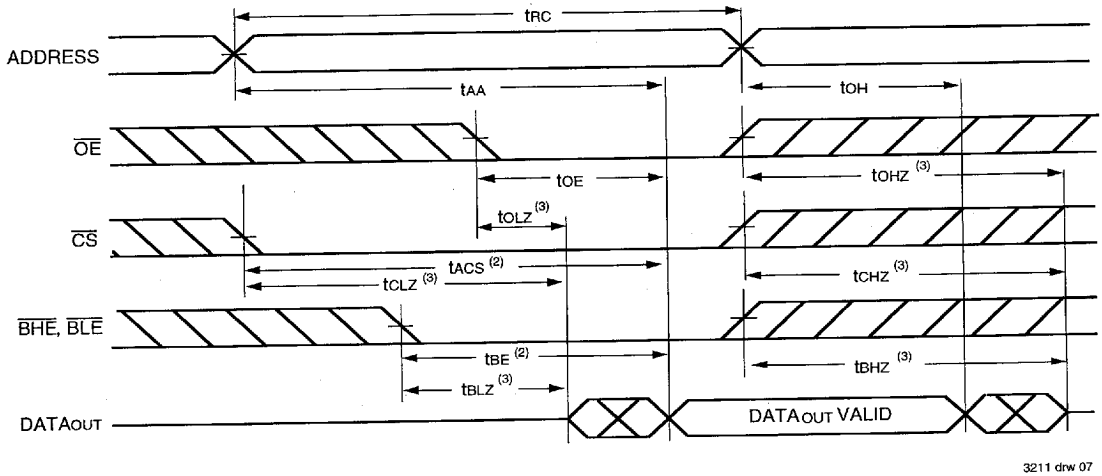
TIMING WAVEFORM OF READ CYCLE NO. 1[1,2,3]



3211 drw 06

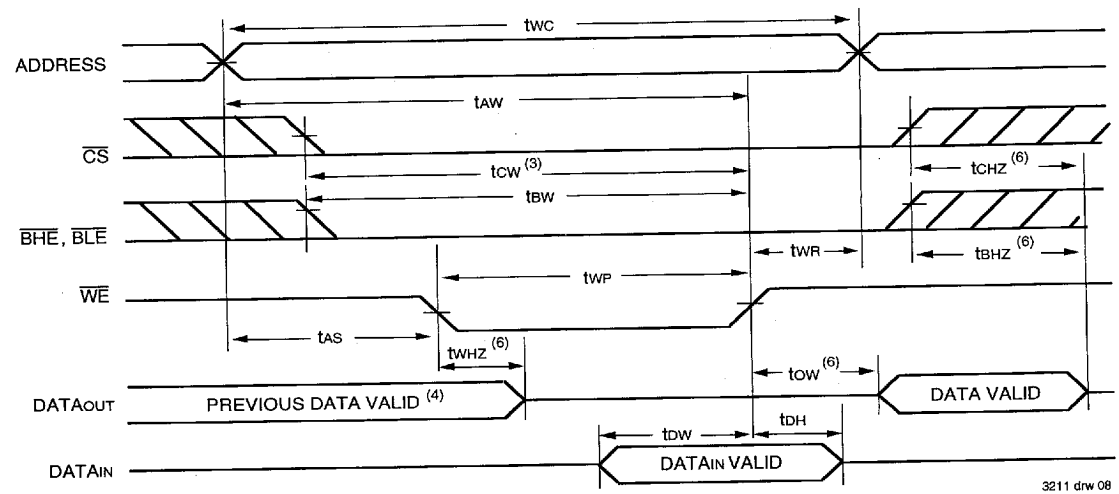
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. $\overline{OE}$, $\overline{BHE}$, and $\overline{BLE}$ are LOW.

TIMING WAVEFORM OF READ CYCLE NO. 2(1)



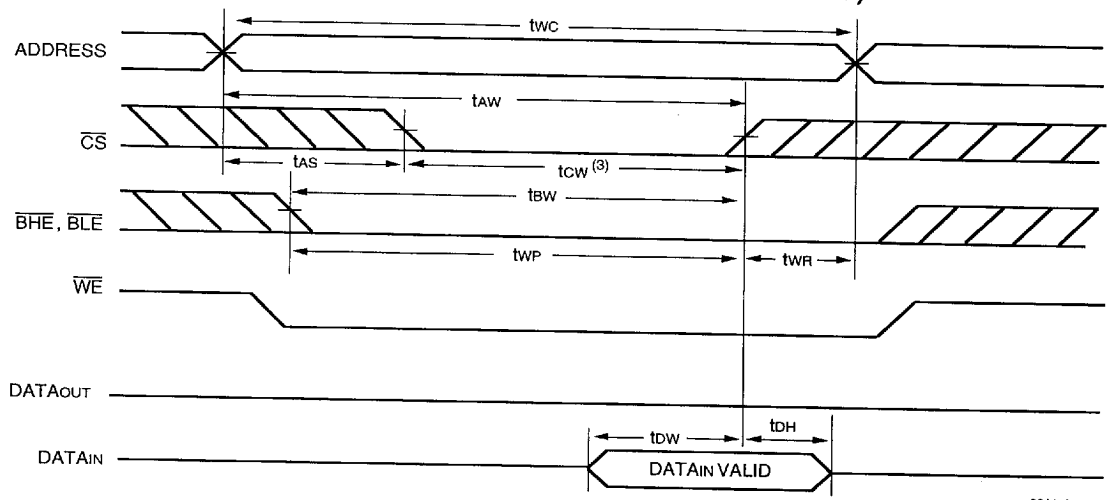
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of $\overline{CS}$, $\overline{BHE}$, or $\overline{BLE}$ transition LOW; otherwise t_{AA} is the limiting parameter.
3. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)



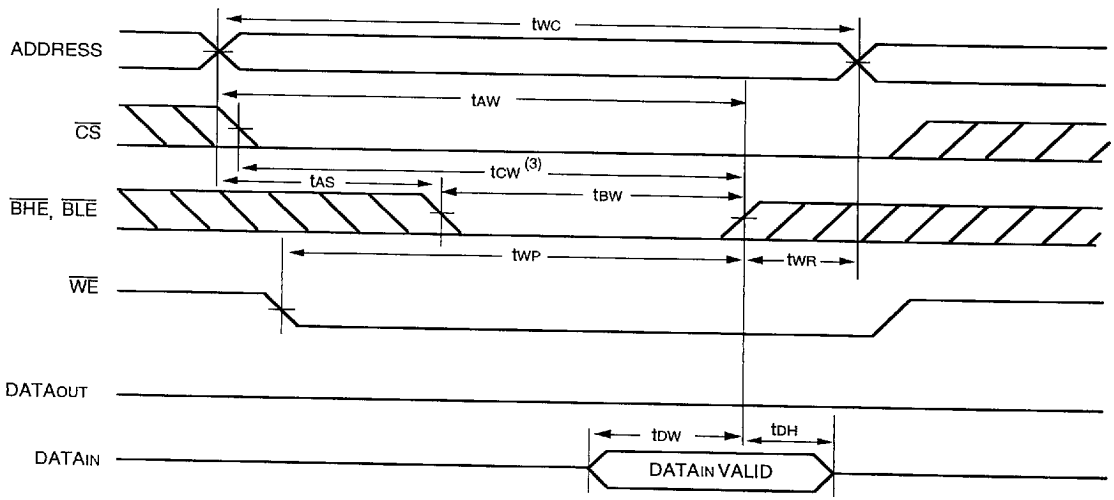
NOTES:
1. $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$, or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



3211 drw 09

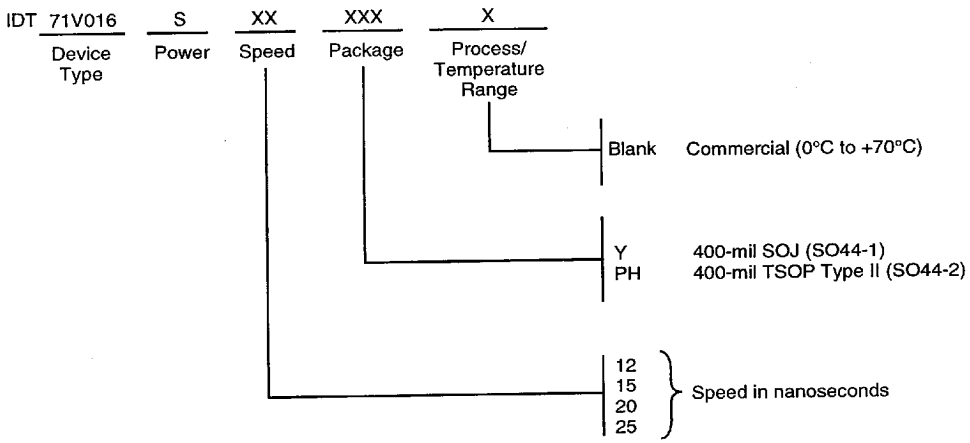
TIMING WAVEFORM OF WRITE CYCLE NO. 3 ($\overline{BHE}$, $\overline{BLE}$ CONTROLLED TIMING)(1,2,5)



3211 drw 10

NOTES:
1. $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$, or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, twp must be greater than or equal to twhz + tdw to allow the I/O drivers to turn off and data to be placed on the bus for the required tdw. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified twp.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



3211 drw 11