OKI Semiconductor

This version: Nov. 1997
Previous version: Jul. 1996

MSC1162A

40-Bit Vacuum Fluorescent Display Tube Grid/Anode Driver

GENERAL DESCRIPTION

The MSC1162A is a monolithic IC designed for directly driving the grid and anode of the vacuum fluorescent display tube. The device contains a 40-bit bidirectional shift register, a 40-bit latch circuit, and 40-output circuit on a single chip.

Display data is serially stored in the shift register at the rising edge of a clock pulse.

Setting the $\overline{CL}$ pin low allows all the driver outputs to be driven low, which makes it possible to set the display blanking.

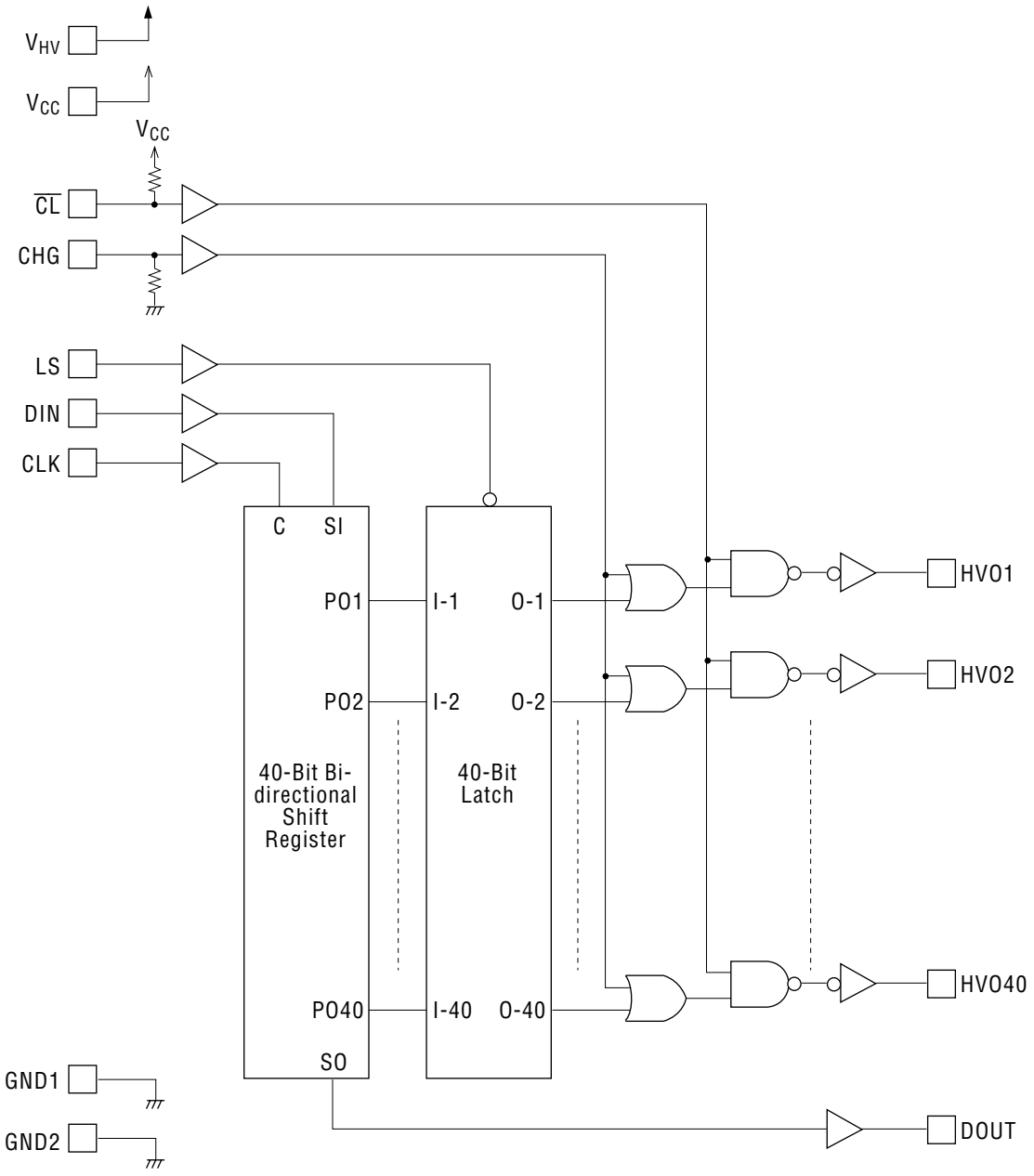
Also, setting both of the $\overline{CL}$ and CHG pins high allows all the driver outputs to be driven high, which provides the easy testing of all lights after final assembly of a VFD tube panel.

The MSC1162A is compatible with the MSC1162.

FEATURES

- Logic Supply Voltage (V_{CC}) : 5V
- Driver Supply Voltage (V_{HV}): 65V
- Driver Output Current
  I_{OHVH1} (Only one driver output : "H") : –40mA
  I_{OHVH2} (All the driver outputs : "H") : –2mA
  I_{OHVL}:1mA
- Directly connected to VFD tube without pull-down resistors
- Data Transfer Speed: 4MHz
- Package :
  60-pin plastic SSOP (SSOP60-P-700-0.65-BK) (Product name : MSC1162AGS-BK)

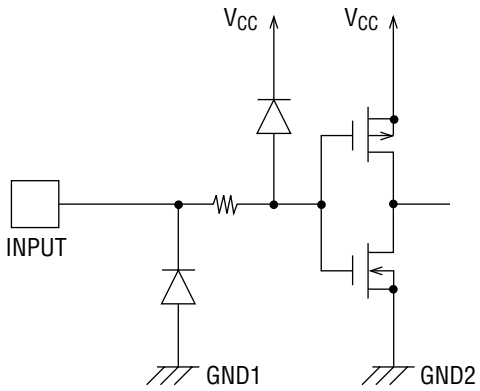
BLOCK DIAGRAM



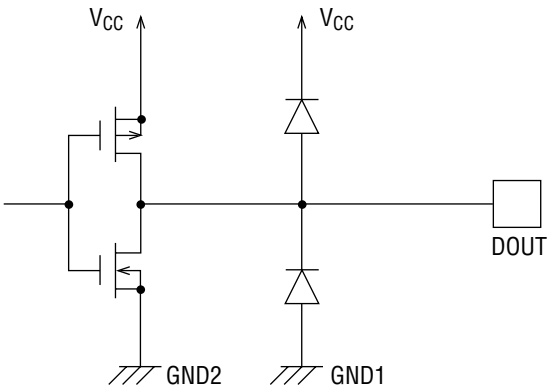
INPUT AND OUTPUT CONFIGURATION

Schematic Diagrams of Logic portion Input/Output Circuits and Driver Output Circuits

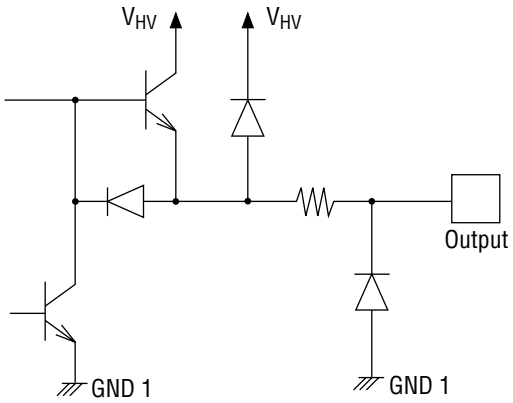
Input Pin



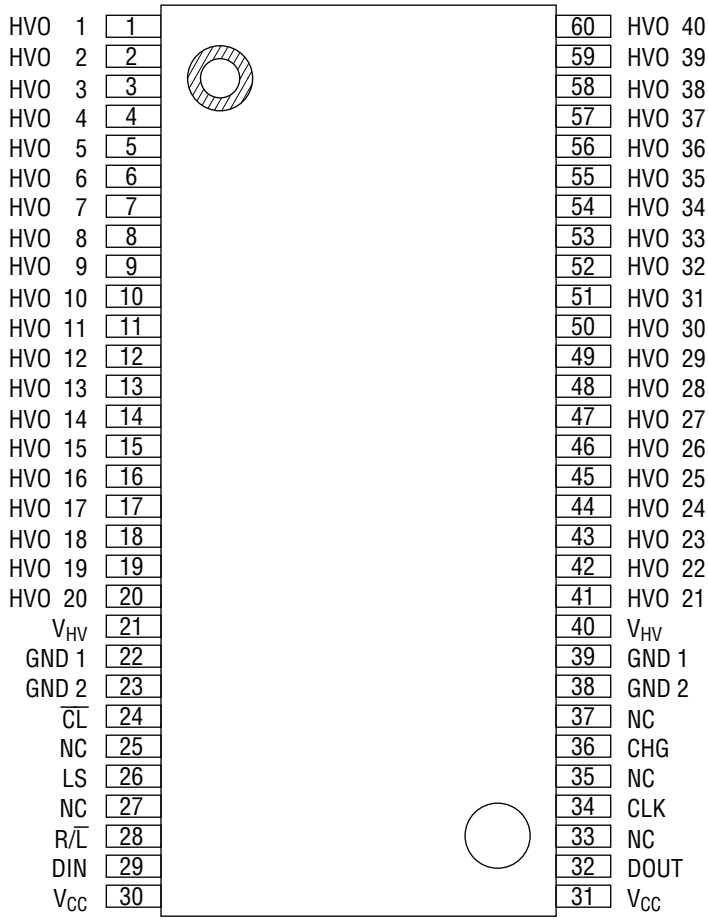
Output Pin



Driver Output Circuit



PIN CONFIGURATION (TOP VIEW)



NC : No-connection pin

60-Pin Plastic SSOP

PIN DESCRIPTION

Symbol	Type	Description
CLK	I	Shift register clock input pin. Shift register reads data through DIN while the CLK pin is low state and the data in the shift register is shifted from one stage to the next stage at the rising edge of the clock.
DIN	I	Serial data input pin of the shift register. Display data (positive logic) is input in through the DIN pin synchronization with clock.
DOUT	O	Serial data output pin of the shift register. Data is output through the DOUT pin in synchronization with the CLK signal. When R/L = High, the data of PO40 in the shift register is output through the DOUT pin. When R/L = Low, the data of PO1 pin in the shift register is output through the DOUT pin.
LS	I	Latch strobe input pin When LS is high, the parallel output data (PO1-40) of the shift register read out. When LS goes from high to low, the parallel output data (PO1-40) of the shift register is held.
$\overline{CL}$	I	Clear input pin with a built-in pull-up resistor The $\overline{CL}$ pin is normally being set high. If the $\overline{CL}$ pin is high and the CHG pin is low, the driver outputs (HV01 to HV40) are in phase with the corresponding latch outputs (O1 to O40). If the $\overline{CL}$ pin is high and the CHG pin is high, the driver outputs (HV01 to HV40) are high irrespective of the states of the latch outputs. If the $\overline{CL}$ pin is set low, the driver outputs are driven low irrespective of the states of the CHG pin and latch outputs. This allows display blanking to be set.
CHG	I	Input for testing (with a pull-down resistor) The $\overline{CL}$ pin is normally being set low. If the CHG pin is low and the $\overline{CL}$ pin is high, the driver outputs (HV01 to HV40) are in phase with the corresponding latch outputs (O1 to O40). If the CHG pin is low and the $\overline{CL}$ pin is low, the driver outputs (HV01 to HV40) are low irrespective of the states of the latch outputs. If the CHG pin is set high, the driver outputs are driven high irrespective of the states of the latch outputs. This provides the easy testing of all lights after final assembly.
VHO1-40	O	High voltage driver outputs for driving VFD tube The driver outputs are in phase with the corresponding latch outputs (O1 to O40). The direct connection to the grid or anode of a VFD tube eliminates pull-down resistors.
VHV		Power supply pin for driver circuits of VFD tube
VCC		Power supply pin for logic
GND1		GND pin for driver circuits of a VFD tube. (D-GND) Since the GND1 is not be connected to L-GND, connect this pin to the external L-GND.
GND2		GND pin for the logic circuits. (L-GND) Since the GND2 pin is not be connected to D-GND, connect this pin to the external D-GND.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Logic Supply Voltage *1	V_{CC}	Applicable to logic supply pin	–0.3 to +6.5	V
Driver Supply Voltage *1, *2	V_{HV}	Applicable to driver supply pin	–0.3 to +70	V
Input Voltage *1	V_{IN}	Applicable to all input pins	–0.3 to V_{CC} +0.3	V
Output Voltage *1	V_O	Applicable to data output pin	–0.3 to V_{CC} +0.3	V
Driver Driving Frequency	f_{DRV}	Applicable to driver output pin	0 to 15	kHz
Withstand Output Voltage *1, *2	V_{HVO}	Applicable to driver output pin	–0.3 to V_{HV} +0.3	V
Power Dissipation	P_D	Ta ≤ 25°C	860	mW
Package Thermal Resistance *3	R_{j-a}	Ta > 25°C	145	°C/W
Storage Temperature	T_{STG}	—	–55 to +150	°C

Notes: *1 Maximum Supply Voltage with respect to L-GND and D-GND
*2 Permanent damage may be caused if the voltage is supplied over the rating value.
*3 Package Thermal Resistance (between junction and ambient)
The junction temperature (Tj) expressed by the equation indicated below should not exceed 150°C.
$T_j = P \times R_{j-a} + Ta$ (P: Maximum power consumption)

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition		Min.	Max.	Unit
Logic Supply Voltage		V_{CC}	Applicable to logic supply voltage pin		4.5	5.5	V
Driver Supply Voltage		V_{HV}	Applicable to driver supply voltage pin		10	65	V
High Level Input Voltage		V_{IH}	Applicable to all input pins		3.6	—	V
Low Level Input Voltage		V_{IL}	Applicable to all input pins		—	1.1	V
High Level Driver Output Current		I_{OHVH1}	Applicable to driver output pin	Only one output is high	—	–40	mA
		I_{OHVH2}		All outputs are high	—	–2	mA
Low Level Driver Output Current		I_{OHVL}	Applicable to all driver output pins		—	1	mA
CLK Frequency		f_{CLK}	See timing diagram		—	4	MHz
CLK Pulse Width		$tw_{(CLK)}$			75	—	ns
Data Setup Time		$tsu_{(D\text{-}CLK)}$			80	—	ns
Data Hold Time		$th_{(CLK\text{-}D)}$			50	—	ns
Data Pulse Width		$tw_{(D)}$			140	—	ns
Latch Probe Pulse Width		$tw_{(LS)}$			80	—	ns
Setup Time	CLK-LS	$tsu_{(CLK\text{-}LS)}$			50	—	ns
	LS-CLK	$tsu_{(LS\text{-}CLK)}$			0	—	ns
	LS-CHG	$tsu_{(LS\text{-}CHG)}$			0	—	µs
	LS-$\overline{CL}$	$tsu_{(LS\text{-}\overline{CL})}$			0	—	µs
Pulse Width	CHG	$tw_{(CHG)}$	—		2	—	µs
	$\overline{CL}$	$tw_{(\overline{CL})}$	—		2	—	µs
Operating Temperature		T_{op}	—		–40	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC}=4.5 to 5.5V, V_{HV}=10 to 65V, Ta=–40 to +85°C)

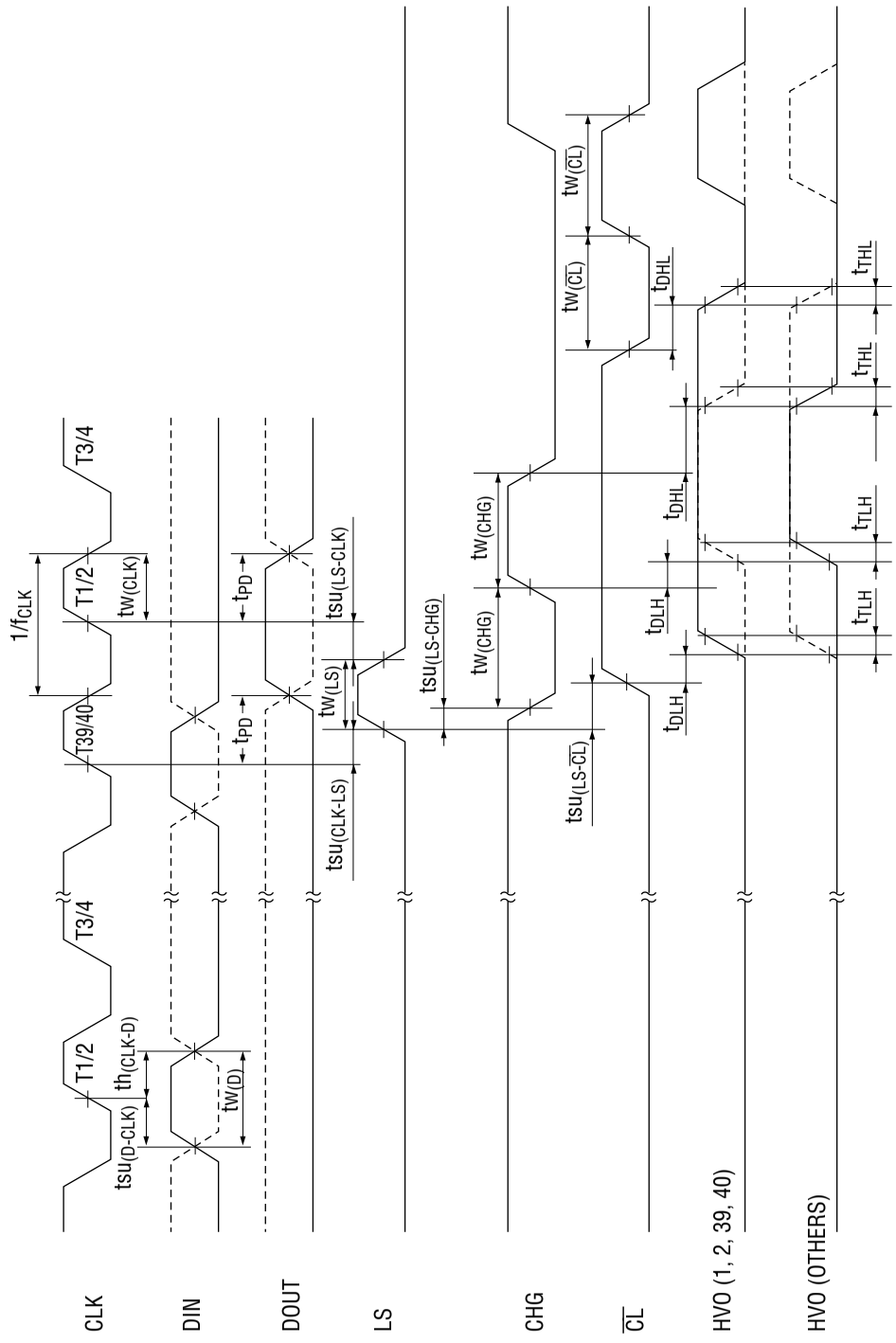
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Logic Supply Current	I_{CC1}	No load V_{CC}=5.5V	All input: Low	—	4.3	6.65	mA
	I_{CC2}		All input: High, Ta=25°C	—	0.5	1.0	
Driver Supply Current	I_{HV1}	No load V_{CC}=5.5V	All input: Low	—	—	1.0	µA
	I_{HV2}		All input: High Ta=25°C		2.45	3.8	mA
High Level Input Current	I_{IH}	V_{CC}=5.5V, V_{IN}=5.5V Inputs excluding CHG		–1	—	1	µA
		V_{CC}=5.5V, V_{IN}=5.5V CHG input		5	—	80	µA
Low Level Input Current	I_{IL}	V_{CC}=5.5V, V_{IN}=0V Inputs excluding $\overline{CL}$		–1	—	1	µA
		V_{CC}=5.5V, V_{IN}=0V $\overline{CL}$ input		–5	—	–80	µA
Input Capacitance	C_I	Ta=25°C		—	15	—	pF
High Level Data Output Voltage	V_{ODH}	I_{OH}=–0.1mA	V_{CC}=4.5V	3.5	—	—	V
			V_{CC}=5.5V	4.5	—	—	V
Low Level Data Output Voltage	V_{ODL}	I_{OL}=0.1mA	V_{CC}=4.5V	—	—	1.1	V
			V_{CC}=5.5V	—	—	1.1	V
High Level Driver Output Voltage	V_{OHVH1}	I_{OH}=–40mA		V_{HV}–4	—	—	V
	V_{OHVH2}	I_{OH}=–2mA		V_{HV}–4	—	—	V
Low Level Driver Output Voltage	V_{OHVL}	I_{OL}=1mA		—	—	3.0	V

AC Characteristics

(V_{CC}=5V, V_{HV}=65V, Ta=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLK-DOUT Delay Time	t_{PD}	—	—	—	300	ns
Delay Time Low to High	t_{DLH}	—	—	0.3	1.0	µs
Transit Time Low to High	t_{TLH}	—	—	2.0	5.0	µs
Delay Time High to Low	t_{DHL}	—	—	0.3	1.0	µs
Transit Time High to Low	t_{THL}	—	—	2.0	5.0	µs

TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

Function Table

Shift register

Input			Shift Register Parallel Out					Output
CLK	R/$\overline{L}$	DIN	PO1	PO2		PO39	PO40	DOUT
↓	X	X	Not changed					Not changed
↑	H	L	L	PO1n		PO38n	PO39n	PO40
↑	H	H	H	PO1n		PO38n	PO39n	PO40
↑	L	L	PO2n	PO3n		PO40n	L	PO1
↑	L	H	PO2n	PO3n		PO40n	H	PO1

X: Don't Care
PO1n to PO40n : PO1 to PO40 data just before CLOCK rises.

Latch

Input	Shift Register Parallel Out	Latch Output
LS	POm	Om
I	X	Not changed
H	L	L
H	H	H

X: Don't Care, m: 1 to 40

Driver output

Input		Latch Output	Driver Output
$\overline{CL}$	CHG	Om	HVOm
L	X	X	L
H	H	X	H
H	L	L	L
H	L	H	H

X: Don't Care, m: 1 to 40

NOTES ON USE

1. Connect GND1 to GND2 externally to be an equal potential voltage.

2. The contents of the shift register are undefined when the power is applied.

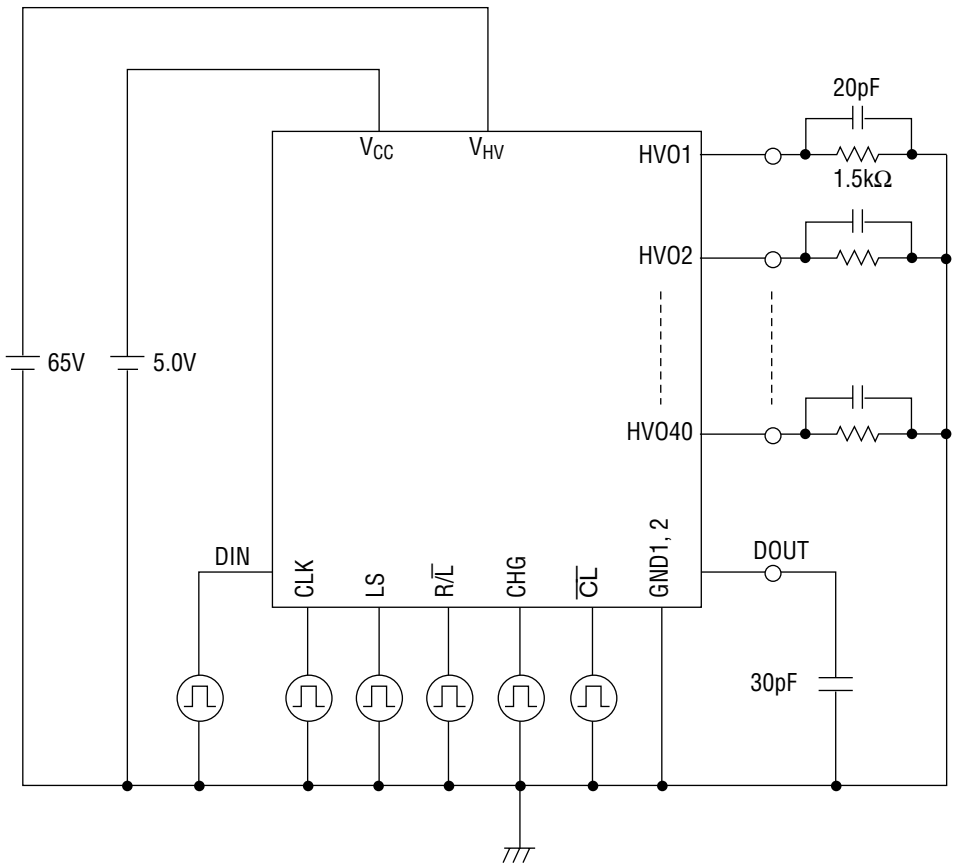
   Therefore, unnecessary driver outputs may be driven high just after power-on, and the VFD tube may flicker.

   To avoid this, follow the procedures:

   1) Apply the driver power supply after applying the logic power supply, with the $\overline{CL}$ pin remained low.

   2) Start displaying by setting the $\overline{CL}$ pin high after in putting display data the shift register through the DIN pin.

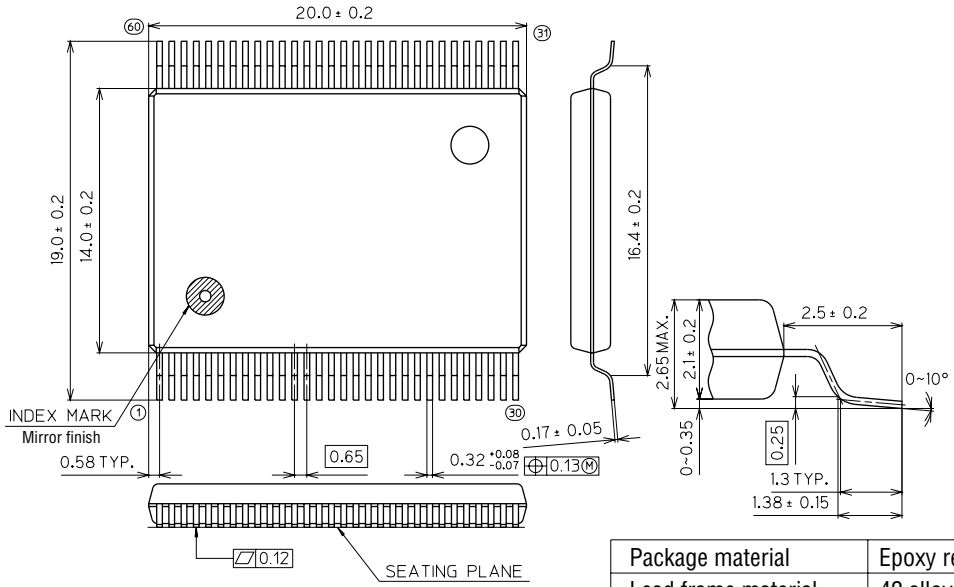
Test circuit



PACKAGE DIMENSIONS

(Unit : mm)

SSOP60-P-700-0.65-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.21 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).