



LCD Driver IC

Preliminary

PT6554

DESCRIPTION

PT6554 is a high performance Liquid Crystal Display (LCD) Driver IC utilizing CMOS Technology specially designed with Key Input Function. It can drive up to a maximum of 164 segments and control up to 4 general purpose output ports. It includes a Key Scan Circuit that can support up to 30 key inputs and provides On-Chip Voltage Detection Type Reset Circuit which prevents incorrect display. Display Data can be directly displayed without using any decoder. PT6554 also supports both 1/4 duty-1/2 bias and 1/4 duty-1/3 bias drive techniques. Pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

FEATURES

- CMOS Technology
- Up to 164 Segment Drivers (4 Com x 41 Seg)
- Up to 4 General Purpose Output Ports
- Key Input Function
- 1/4 Duty-1/2 Bias and 1/4 Duty-1/3 Bias Drive Techniques
- Sleep Mode & All Segment OFF Function
- On-Chip Voltage Detection Type Reset Circuit
- RC Oscillation Circuit
- Available in 64 pins, QFP or LQFP Package

APPLICATION

- Electronic Equipment with LCD Display

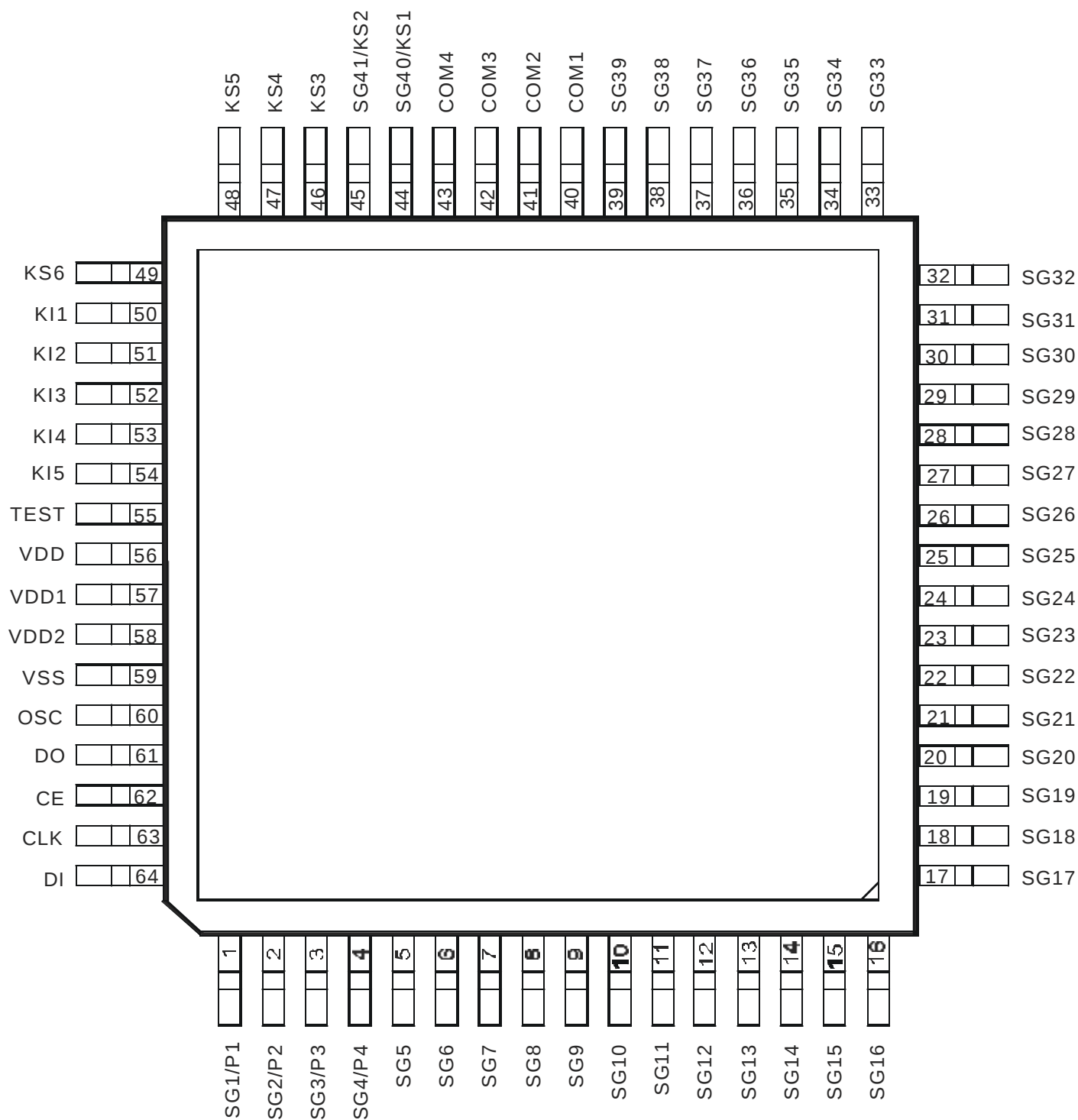


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PIN CONFIGURATION



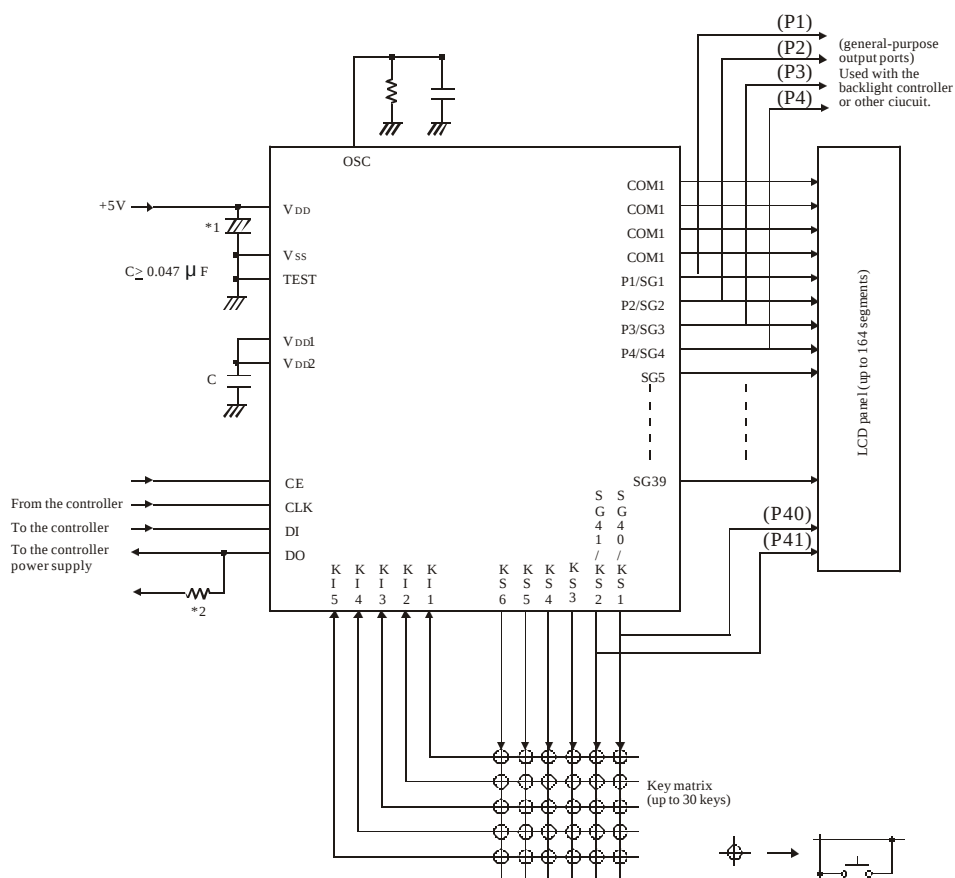


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APPLICATION CIRCUIT 1



- Notes:
1. A capacitor must be added to the power line so that both the power supply voltage (VDD) rise time when power is applied and the power supply voltage (VDD) fall time when power drops are at least 1 ms.
 2. DO is an open - drain output and requires a pull-high resistor between 1kΩ to 10kΩ. The pull-up resistor value must be appropriate to the capacitor of the external wiring so that the signal waveforms are not degraded.

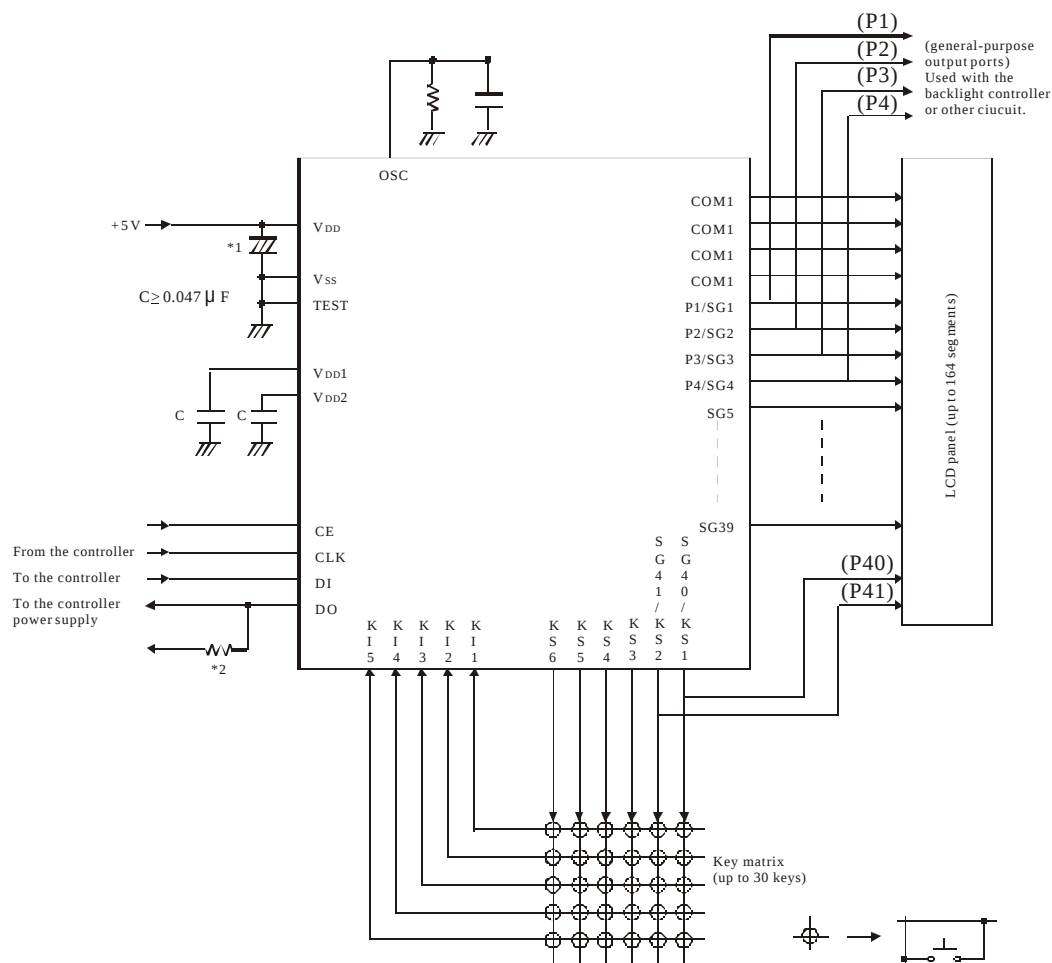


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APPLICATION CIRCUIT 2



- Notes:
1. A capacitor must be added to the power line so that both the power supply voltage (VDD) rise time when power is applied and the power supply voltage (VDD) fall time when power drops are at least 1 ms.
 2. DO is an open - drain output and requires a pull-high resistor between $1k\Omega$ to $10k\Omega$. The pull-up resistor value must be appropriate to the capacitor of the external wiring so that the signal wave forms are not degraded.

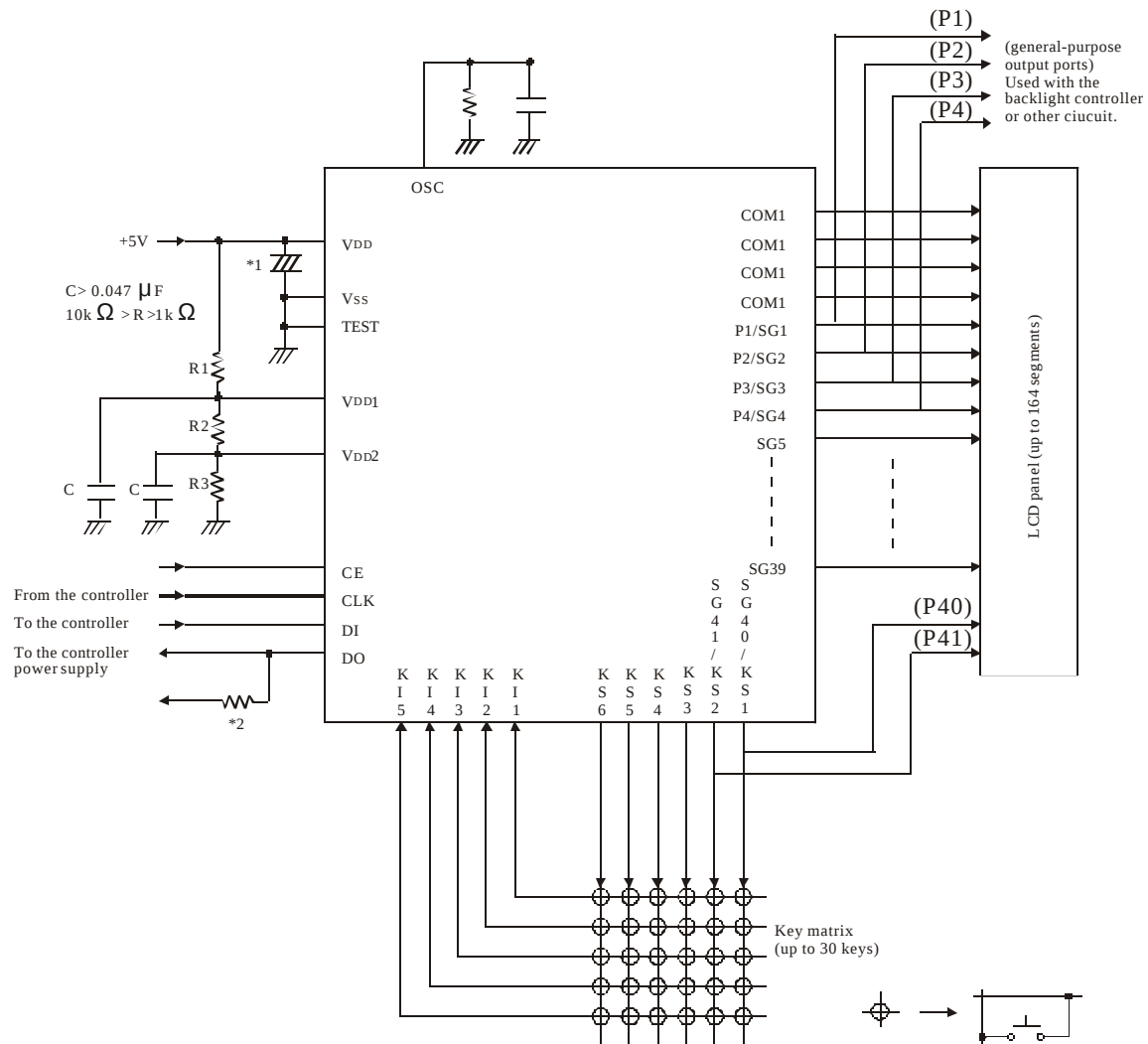


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APPLICATION CIRCUIT 3



- Notes:
1. A capacitor must be added to the power line so that both the power supply voltage (VDD) rise time when power is applied and the power supply voltage (VDD) fall time when power drops are at least 1 ms.
 2. DO is an open-drain output and requires a pull-high resistor between 1kΩ to 10kΩ. The pull-up resistor value must be appropriate to the capacitor of the external writing so that the signal waveforms are not degraded.
 3. R1=R2=R3, the resistance value must be decided by the LCD panel size.