REJ03B0034-0120Z
Rev.1.20
2003.10.31

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Outline

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Shortest instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2.
Peripheral function	Interrupt	Internal: 10 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels
	Watchdog timer	15 bits x 1 (with prescaler)
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel Circuits of input capture and output compare.
	Serial I/O	•1 channel Clock synchronous, UART •1 channel UART
	A-D converter	10-bit A-D converter: 1 circuit, 12 channels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •Ring oscillator (high speed, low speed) On High-speed ring oscillator the frequency adjustment function is usable.
	Oscillation stop detection function	Stop detection of main clock oscillation
	Voltage detection circuit	Included
	Power on reset circuit	Included
	Port	Input/Output: 22 (including LED drive port), Input: 2 (LED drive I/O port: 8, max. 20 mA)
Electrical characteristics	Power supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Power consumption	Typ. 9 mA (VCC = 5.0 V, (f(XIN) = 20 MHz, High-speed mode) Typ. 5 mA (VCC = 3.0 V, (f(XIN) = 10 MHz, High-speed mode) Typ. 35 µA (VCC = 3.0 V, Wait mode, Peripheral clock off) Typ. 0.7 µA (VCC = 3.0 V, Stop mode)
Flash memory	Program/erase voltage	VCC = 2.7 to 5.5 V
	Number of program/erase	100 times
Operating ambient temperature		-20 to 85 °C -40 to 85 °C (option)
Package		32-pin plastic mold LQFP

Option: If you require this option, please specify so.

1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

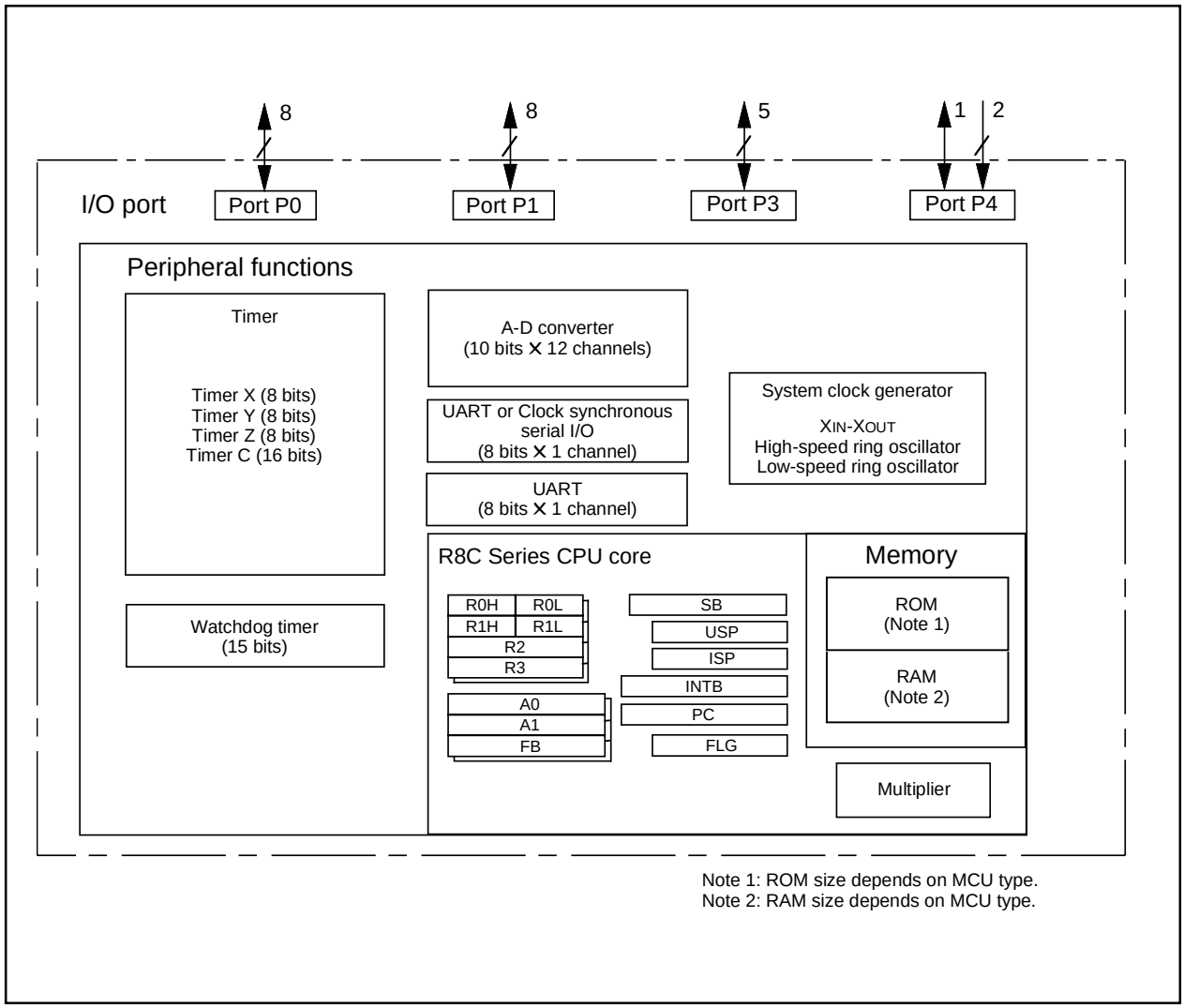


Figure 1.1 Block Diagram

1.4 Product List

Table 1.2 lists the products.

Table 1.2 Product List As of Oct. 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks
R5F21112FP **	8K bytes	512 bytes	32P6U-A	Flash memory version
R5F21113FP **	12K bytes	768 bytes	32P6U-A	
R5F21114FP **	16K bytes	1K bytes	32P6U-A	
R5F21112DFP **	8K bytes	512 bytes	32P6U-A	D version
R5F21113DFP **	12K bytes	768 bytes	32P6U-A	
R5F21114DFP **	16K bytes	1K bytes	32P6U-A	

** : Under development

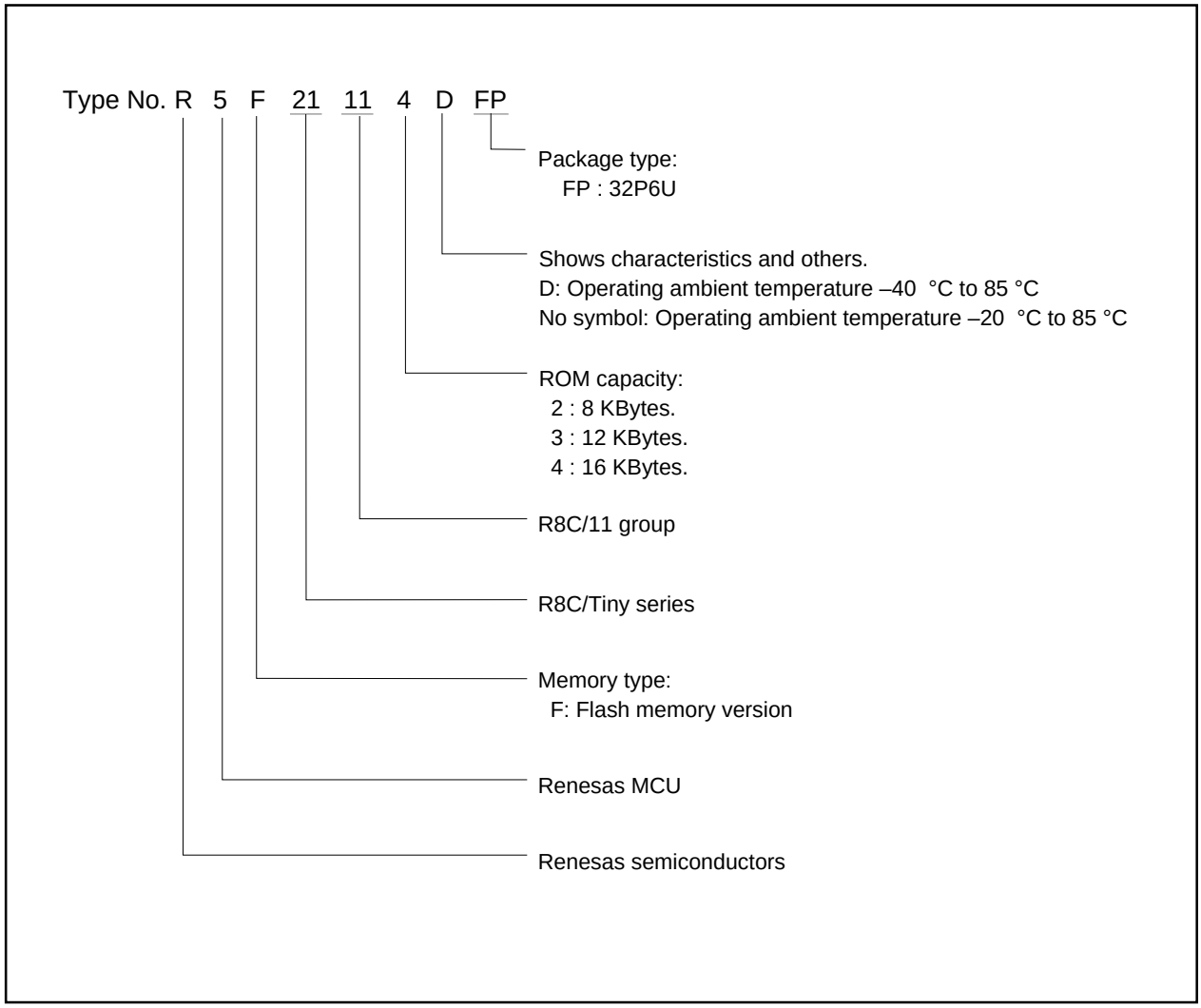


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Configuration

Figure 1.3 shows the pin configuration (top view).

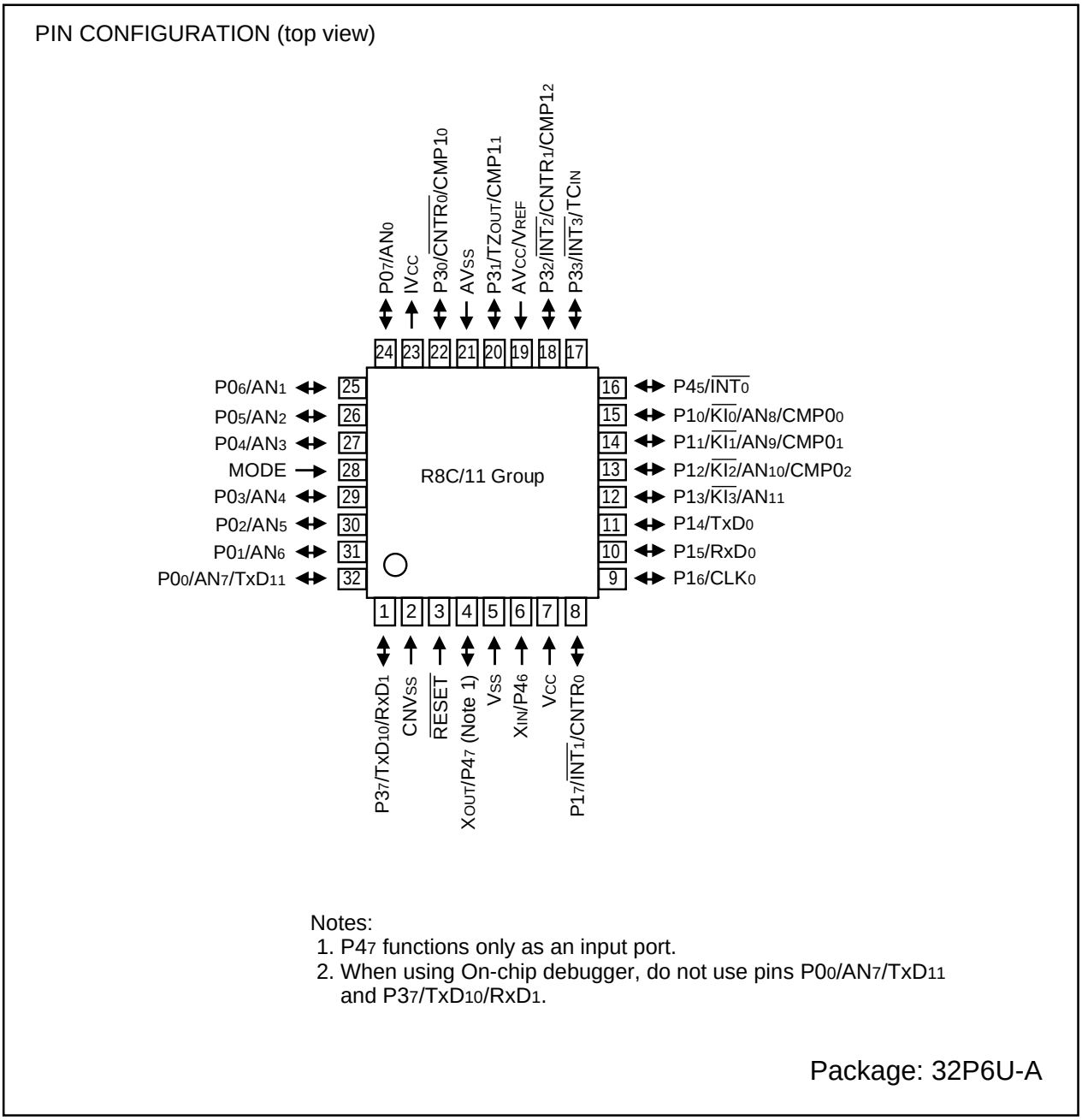


Figure 1.3 Pin Configuration (Top View)

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	Input	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	Output	Connect this pin to Vss via a capacitor (0.1 µF).
Analog power supply input	AVcc, AVss	Input	These are power supply input pins for A-D converter. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	$\overline{\text{RESET}}$	Input	"L" on this input resets the MCU.
CNVss	CNVss	Input	Connect this pin to Vss via a resistor.
MODE	MODE	Input	Connect this pin to Vcc via a resistor.
Main clock input	XIN	Input	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	Output	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	Input	These are $\overline{\text{INT}}$ interrupt input pins.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	Input	These are key input interrupt input pins.
Timer X	CNTR0	Input/Output	This is the timer X I/O pin.
	$\overline{\text{CNTR0}}$	Output	This is the timer X output pin.
Timer Y	CNTR1	Input/Output	This is the timer Y I/O pin.
Timer Z	TZOUT	Output	This is the timer Z output pin.
Timer C	TCIN	Input	This is the timer C input pin.
	CMP00 to CMP03, CMP10 to CMP13	Output	These are the timer C output pins.
Serial interface	CLK0	Input/Output	This is a transfer clock I/O pin.
	RxD0, RxD1	Input	These are serial data input pins.
	TxD0, TxD10, TxD11	Output	These are serial data output pins.
Reference voltage input	VREF	Input	This is a reference voltage input pin for A-D converter.
A-D converter	AN0 to AN11	Input	These are analog input pins for A-D converter.
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	Input/Output	These are 8-bit CMOS I/O ports. Each port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	Input	These are input only pins.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

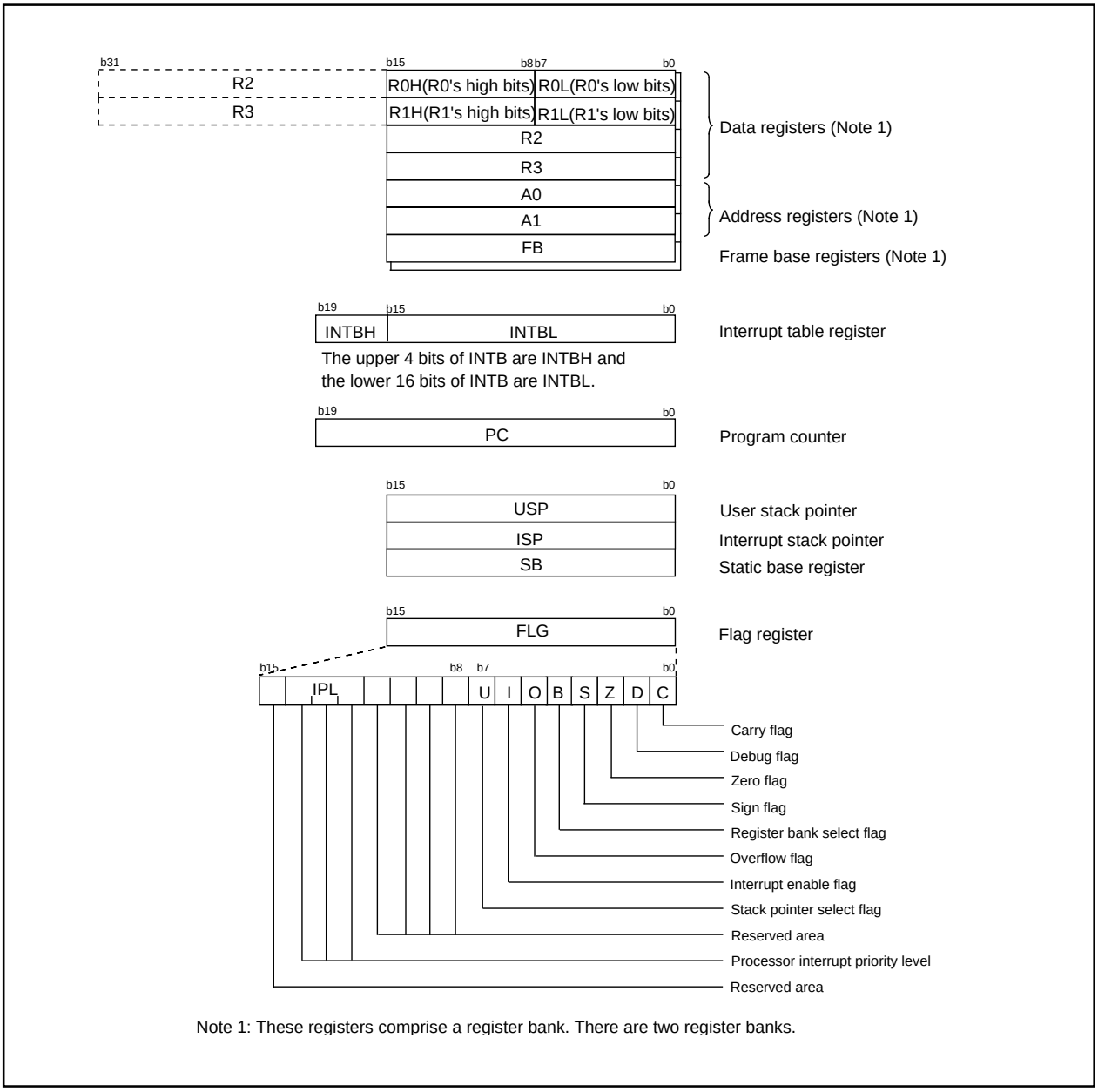


Figure 2.1. Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is cleared to “0” when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.

The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

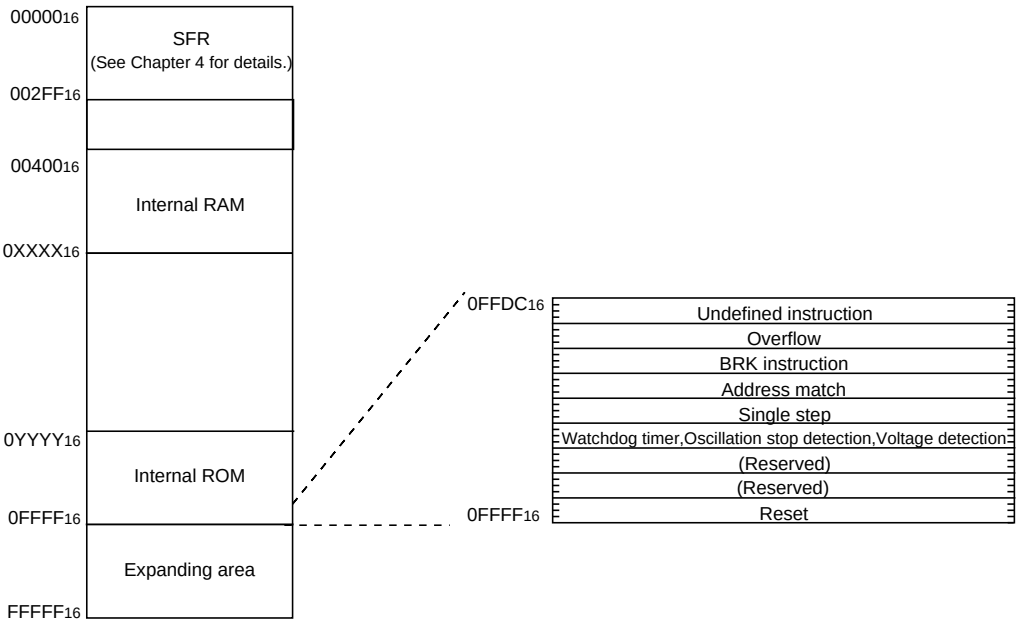
Figure 3.1 is a memory map of this MCU. The address space extends the 1M bytes from address 00000_{16} to $FFFFF_{16}$.

The internal ROM is allocated in a lower address direction beginning with address $0FFFF_{16}$. For example, a 16-Kbyte internal ROM is allocated to the addresses from $0C000_{16}$ to $0FFFF_{16}$.

The fixed interrupt vector table is allocated to the addresses from $0FFDC_{16}$ to $0FFFF_{16}$. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400_{16}. For example, a 1-Kbyte internal RAM is allocated to the addresses from 00400_{16} to $007FF_{16}$. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

Special function registers (SFR) are allocated to the addresses from 00000_{16} to $002FF_{16}$. Peripheral function control registers are located here. Of the SFR, any space which has no functions allocated is reserved for future use and cannot be used by users.



Type name	Internal ROM		Internal RAM	
	Size	Address 0YYYY₁₆	Size	Address 0XXXX₁₆
R5F21114FP, R5F21114DFP	16K bytes	0C000₁₆	1K bytes	007FF₁₆
R5F21113FP, R5F21113DFP	12K bytes	0D000₁₆	768 bytes	006FF₁₆
R5F21112FP, R5F21112DFP	8K bytes	0E000₁₆	512 bytes	005FF₁₆

Figure 3.1 Memory Map

4. Special Function Register (SFR)

Address	Register	Symbol	After reset
000016			
000116			
000216			
000316			
000416	Processor mode register 0 [1]	PM0	0016
000516	Processor mode register 1	PM1	0016
000616	System clock control register 0	CM0	011010002
000716	System clock control register 1	CM1	001000002
000816	High-speed ring control register 0	HR0	0016
000916	Address match interrupt enable register	AIER	XXXXXX002
000A16	Protect register	PRCR	00XXX0002
000B16	High-speed ring control register 1	HR1	4016
000C16	Oscillation stop detection register	OCD	000001002
000D16	Watchdog timer reset register	WDTR	XX16
000E16	Watchdog timer start register	WDTS	XX16
000F16	Watchdog timer control register	WDC	000XXXXX2
001016	Address match interrupt register 0	RMAD0	0016
001116			0016
001216			X016
001316			
001416	Address match interrupt register 1	RMAD1	0016
001516			0016
001616			X016
001716			
001816			
001916	Voltage detection register 1 [2]	VCR1	0016
001A16	Voltage detection register 2 [2]	VCR2	XXX0000016
001B16			
001C16			
001D16			
001E16	INT0 input filter select register	INT0F	XXXXX0002
001F16	Voltage detection interrupt register [2]	D4INT	0016 [3]
002016			
002116			
002216			
002316			
002416			
002516			
002616			
002716			
002816			
002916			
002A16			
002B16			
002C16			
002D16			
002E16			
002F16			
003016			
003116			
003216			
003316			
003416			
003516			
003616			
003716			
003816			
003916			
003A16			
003B16			
003C16			
003D16			
003E16			
003F16			

010000012 [4]

X : Undefined
Blank columns are all reserved space. No access is allowed.
Notes:

1. Software reset or the watchdog timer reset does not affect bits 0 to 1 of PM0 register.
2. Software reset or the watchdog timer reset does not affect this register.
3. Owing to Reset input.
4. In the case of $\overline{\text{RESET}}$ pin = “H” retaining.

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆			
0049₁₆			
004A₁₆			
004B₁₆			
004C₁₆			
004D₁₆	Key input interrupt control register	KUPIC	XXXXX000₂
004E₁₆	A-D conversion interrupt control register	ADIC	XXXXX000₂
004F₁₆			
0050₁₆	Compare 1 interrupt control register	CMP1IC	XXXXX000₂
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX000₂
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX000₂
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX000₂
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX000₂
0055₁₆	INT2 interrupt control register	INT2IC	XXXXX000₂
0056₁₆	Timer X interrupt control register	TXIC	XXXXX000₂
0057₁₆	Timer Y interrupt control register	TYIC	XXXXX000₂
0058₁₆	Timer Z interrupt control register	TZIC	XXXXX000₂
0059₁₆	INT1 interrupt control register	INT1IC	XXXXX000₂
005A₁₆	INT3 interrupt control register	INT3IC	XXXXX000₂
005B₁₆	Timer C interrupt control register	TCIC	XXXXX000₂
005C₁₆	Compare 0 interrupt control register	CMP0IC	XXXXX000₂
005D₁₆	INT0 interrupt control register	INT0IC	XX00X000₂
005E₁₆			
005F₁₆			
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

X : Undefined
Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	After reset
0080₁₆	Timer Y, Z mode register	TYZMR	00₁₆
0081₁₆	Prescaler Y	PREY	FF₁₆
0082₁₆	Timer Y secondary	TYSC	FF₁₆
0083₁₆	Timer Y primary	TYPR	FF₁₆
0084₁₆	Timer Y, Z waveform output control register	PUM	00₁₆
0085₁₆	Prescaler Z	PREZ	FF₁₆
0086₁₆	Timer Z secondary	TZSC	FF₁₆
0087₁₆	Timer Z primary	TZPR	FF₁₆
0088₁₆			
0089₁₆			
008A₁₆	Timer Y, Z output control register	TYZOC	00₁₆
008B₁₆	Timer X mode register	TXMR	00₁₆
008C₁₆	Prescaler X	PREX	FF₁₆
008D₁₆	Timer X register	TX	FF₁₆
008E₁₆	Count source set register	TCSS	00₁₆
008F₁₆			
0090₁₆ 0091₁₆	Timer C register	TC	00₁₆ 00₁₆
0092₁₆			
0093₁₆			
0094₁₆			
0095₁₆			
0096₁₆	External input enable register	INTEN	00₁₆
0097₁₆			
0098₁₆	Key input enable register	KIEN	00₁₆
0099₁₆			
009A₁₆	Timer C control register 0	TCC0	00₁₆
009B₁₆	Timer C control register 1	TCC1	00₁₆
009C₁₆ 009D₁₆	Capture, compare 0 register	TM0	XX₁₆ XX₁₆
009E₁₆ 009F₁₆	Compare 1 register	TM1	XX₁₆ XX₁₆
00A0₁₆	UART0 transmit/receive mode register	U0MR	00₁₆
00A1₁₆	UART0 bit rate generator	U0BRG	XX₁₆
00A2₁₆ 00A3₁₆	UART0 transmit buffer register	U0TB	XX₁₆ XX₁₆
00A4₁₆	UART0 transmit/receive control register 0	U0C0	00001000₂
00A5₁₆	UART0 transmit/receive control register 1	U0C1	00000010₂
00A6₁₆ 00A7₁₆	UART0 receive buffer register	U0RB	XX₁₆ XX₁₆
00A8₁₆	UART1 transmit/receive mode register	U1MR	00₁₆
00A9₁₆	UART1 bit rate generator	U1BRG	XX₁₆
00AA₁₆ 00AB₁₆	UART1 transmit buffer register	U1TB	XX₁₆ XX₁₆
00AC₁₆	UART1 transmit/receive control register 0	U1C0	00001000₂
00AD₁₆	UART1 transmit/receive control register 1	U1C1	00000010₂
00AE₁₆ 00AF₁₆	UART1 receive buffer register	U1RB	XX₁₆ XX₁₆
00B0₁₆	UART transmit/receive control register 2	UCON	00₁₆
00B1₁₆			
00B2₁₆			
00B3₁₆			
00B4₁₆			
00B5₁₆			
00B6₁₆			
00B7₁₆			
00B8₁₆			
00B9₁₆			
00BA₁₆			
00BB₁₆			
00BC₁₆			
00BD₁₆			
00BE₁₆			
00BF₁₆			

X : Undefined
Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	After reset
00C016	A-D register	AD	XX16
00C116			XX16
00C216			
00C316			
00C416			
00C516			
00C616			
00C716			
00C816			
00C916			
00CA16			
00CB16			
00CC16			
00CD16			
00CE16			
00CF16			
00D016			
00D116			
00D216			
00D316			
00D416	A-D control register 2	ADCON2	0016
00D516			
00D616	A-D control register 0	ADCON0	00000XXX2
00D716	A-D control register 1	ADCON1	0016
00D816			
00D916			
00DA16			
00DB16			
00DC16			
00DD16			
00DE16			
00DF16			
00E016	Port P0 register	P0	XX16
00E116	Port P1 register	P1	XX16
00E216	Port P0 direction register	PD0	0016
00E316	Port P1 direction register	PD1	0016
00E416			
00E516	Port P3 register	P3	XX16
00E616			
00E716	Port P3 direction register	PD3	0016
00E816	Port P4 register	P4	XX16
00E916			
00EA16	Port P4 direction register	PD4	0016
00EB16			
00EC16			
00ED16			
00EE16			
00EF16			
00F016			
00F116			
00F216			
00F316			
00F416			
00F516			
00F616			
00F716			
00F816			
00F916			
03FA16			
00FB16			
00FC16	Pull-up control register 0	PUR0	00XX00002
00FD16	Pull-up control register 1	PUR1	XXXXXX0X2
00FE16	Port P1 drivability control register	DRR	0016
00FF16	Timer C output control register	TCOUT	0016
01B316	Flash memory control register 4	FMR4	0100000X2
01B416			
01B516	Flash memory control register 1	FMR1	0100XX0X2
01B616			
01B716	Flash memory control register 0	FMR0	XX0000012

X : Undefined
Blank columns are all reserved space. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}	Supply voltage	V_{CC}=AV_{CC}	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage	V_{CC}=AV_{CC}	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	Topr=25 °C	300	mW
T_{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			2.7	5.0	5.5	V
AVcc	Analog supply voltage			—	V_{CC}	—	V
Vss	Supply voltage			—	0	—	V
AVss	Analog supply voltage			—	0	—	V
V_{IH}	"H" input voltage			0.8V_{CC}	—	V_{CC}	V
V_{IL}	"L" input voltage			0	—	0.2V_{CC}	V
$I_{OH\ (sum)}$	"H" peak all output currents	Sum of all pins' IOH (peak)		—	—	-60.0	mA
$I_{OH\ (peak)}$	"H" peak output current			—	—	-10.0	mA
$I_{OH\ (avg)}$	"H" average output current			—	—	-5.0	mA
$I_{OL\ (sum)}$	"L" peak all output currents	Sum of all pins' IOL (peak)		—	—	60	mA
$I_{OL\ (peak)}$	"L" peak output current	Except $P1_0$ to $P1_7$		—	—	10	mA
		$P1_0$ to $P1_7$	Drive ability HIGH	—	—	30	mA
			Drive ability LOW	—	—	10	mA
$I_{OL\ (avg)}$	"L" average output current	Except $P1_0$ to $P1_7$		—	—	5	mA
		$P1_0$ to $P1_7$	Drive ability HIGH	—	—	15	mA
			Drive ability LOW	—	—	5	mA
f (X_{IN})	Main clock input oscillation frequency		3.0V ≤ Vcc ≤ 5.5V	0	—	20	MHz
			2.7V ≤ Vcc < 3.0V	0	—	10	MHz

Note
1: Referenced to V_{CC} = AV_{CC} = 2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2: The mean output current is the mean value within 100ms.

Table 5.3 A-D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} =V_{CC}			10	Bit
–	Absolute accuracy	10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V			±3	LSB
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V			±2	LSB
		10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=3.3V			±5	LSB
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=3.3V			±2	LSB
R_{LADDER}	Ladder resistance		V_{REF}=V_{CC}	10		40	kΩ
t_{CONV}	Conversion time	10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V	3.3			µs
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V	2.8			µs
V_{REF}	Reference voltage			2.0		V_{CC}	V
V_{IA}	Analog input voltage			0		V_{ref}	V
–	A-D operation clock frequency[2]	Without sample & hold		0.25		10	MHz
		With sample & hold		1.0		10	MHz

Note
1: Referenced to V_{CC}=AV_{CC}=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2: When f_{AD} is 10 MHz more, divide the f_{AD} and make A-D operation clock frequency ($Ø_{AD}$) lower than 10 MHz.
3: When the Vcc is less than 4.2V, divide the f_{AD} and make A-D operation clock frequency ($Ø_{AD}$) lower than f_{AD}/2.

Table 5.4 Flash Memory Version Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Byte program time		—	75	TBD	µs
–	Block erase time		—	400	TBD	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program, Erase Temperature		0	—	60	°C

Note
1: Referenced to V_{CC1}=AVcc=2.7 to 5.5V at Topr = 0 to 60 °C unless otherwise specified.

Table 5.5 Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Voltage detection level		3.3	3.8	4.3	V
	Voltage detection interrupt request generating time[2]			40		V
	Voltage detection circuit self consumption current	VC27="1"		TBD		V
td(E-A)	Waiting time till voltage detection circuit operation starts[3]				20	V

Note
1: The measureing condition is Vcc=AVcc=5.0 V and Topr=25 °C.
2: This shows the time till the voltage detection interrupt request is generated since the voltage passes Vdet.
3: This shows the required time till the voltage detection circuit operates when setting to "1" again.

Table 5.6 Power-on Reset Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
	Power-on reset start time[2]	Vcc<0.5V	TBD			ms
	Power-on reset cancel operation start voltage		3.3	3.8	4.3	V
	Hardware reset 2 cancel operation start voltage		3.3	3.8	4.3	V
	Supply start up condition when using power-on reset circuit	Intergradation time to 0V<2.7V			TBD	ms

Note
1: The measuring condition is Vcc=AVcc=5.0 V and Topr=25 °C.
2: Keep Vcc<0.5V for over regulated time to execute the reset operation.

Table 5.7 High-speed Ring Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
	Settable high-speed ring oscillator minimum period	Set "00_{16}" in the HR1 register		TBD		ns
	High-speed ring oscillator adjusted unit	Differences when setting "01_{16}" and "00_{16}" in the HR register		1		ns

Note
1: The measuring condition is Vcc=AVcc=5.0 V and Topr=25 °C.

Table 5.8 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on[2]				2	ms
td(R-S)	STOP release time[3]				150	µs

Note
1: The measuring condition is Vcc=AVcc=2.7 to 5.0 V and Topr=25 °C.
2: This shows the wait time untill the internal power supply generating circuit is stabilized during power-on.
3: This shows the time till BCLK starts from the interrupt acknowledgement to cancel stop mode.

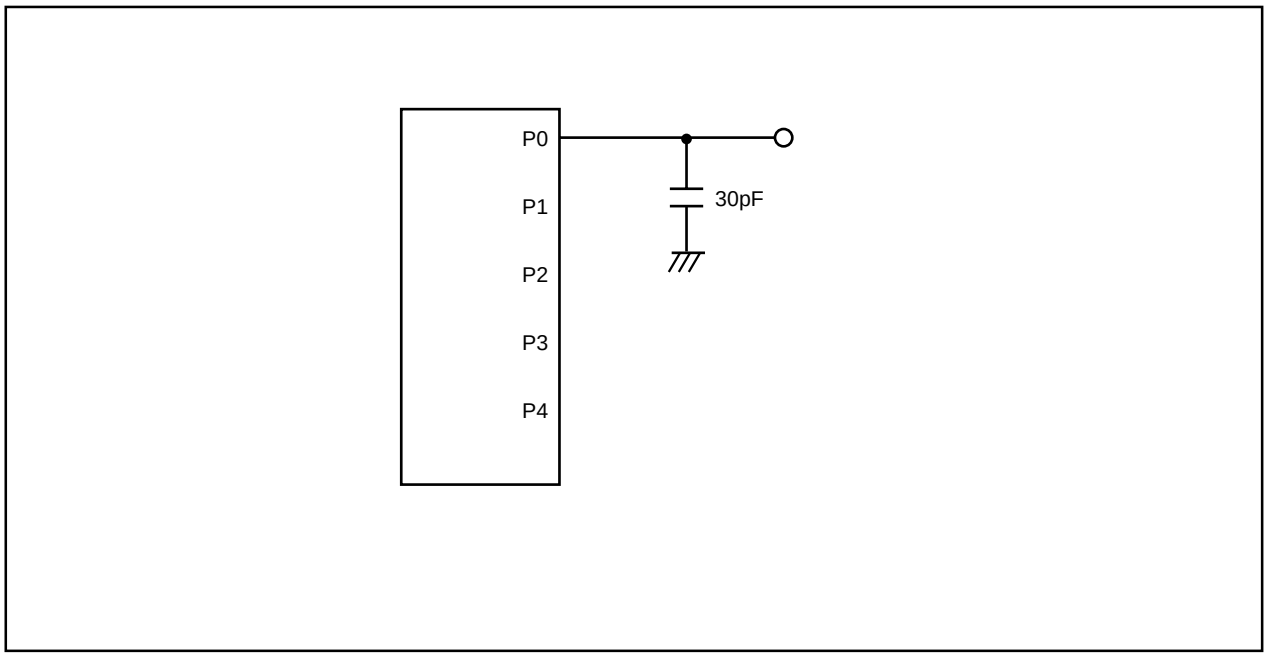


Figure 5.1 Port P0 to P4 measurement circuit

Table 5.9 Electrical Characteristics (1) [Vcc=5V]

Symbol	Parameter		Measuring condition	Standard Min.	Standard Typ.	Standard Max.	Unit
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-5mA	V_{CC}-2.0		V_{CC}	V
			I_{OH}=-200µA	V_{CC}-0.3		V_{CC}	V
		X_{OUT}	Drive ability HIGH I_{OH}=-1 mA	V_{CC}-2.0		V_{CC}	V
			Drive ability LOW I_{OH}=-500µA	V_{CC}-2.0		V_{CC}	V
V_{OL}	"L" output voltage	$P1_0$ to P17 Except X_{OUT}	I_{OH}= 5 mA			2.0	V
			I_{OH}= 200 µA			0.45	V
		$P1_0$ to P17	Drive ability HIGH I_{OH}= 10 mA			2.0	V
			Drive ability LOW I_{OH}= 5 mA			2.0	V
		X_{OUT}	Drive ability HIGH I_{OH}= 1 mA			2.0	V
			Drive ability LOW I_{OH}=500µA			2.0	V
V_{T+}-V_{T-}	Hysteresis	INT_0, INT_1, INT_2, INT_3, KI_0, KI_1, KI_2, KI_3, $CNTR_O$, $CNTR_1$, TC_{IN}, RxD_0, RxD_1		0.2		1.0	V
		RESET		0.2		2.2	V
I_{IH}	"H" input current		V_I=5V			5.0	µA
I_{IL}	"L" input current		V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V	30	50	167	kΩ
R_{fXIN}	Feedback resistance	X_{IN}			1.0		MΩ
f_{RING-S}	Low-speed ring oscillator frequency			40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode	2.0			V

Note
1 : Referenced to V_{CC}=AV_{CC}=4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=20MHz unless otherwise specified.

Table 5.10 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter	Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
I_{CC}	Power supply current (V_{CC}=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V_{SS}	High-speed mode	X_{IN}=20 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		9	15	mA
			X_{IN}=16 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		8	14	mA
			X_{IN}=10 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		5		mA
		Medium-speed mode	X_{IN}=20 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		4		mA
			X_{IN}=16 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		3		mA
			X_{IN}=10 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		2		mA
		High-speed ring oscillator mode	Main clock off High-speed ring oscillator on=8 MHz Low-speed ring oscillator on=125 kHz No division		4	8	mA
			Main clock off High-speed ring oscillator on=8 MHz Low-speed ring oscillator on=125 kHz Division by 8		1.5		mA
		Low-speed ring oscillator mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		0.4	2.0	mA
		Wait mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation		40	80	µA
		Wait mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off		38	76	µA
		Stop mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator off CM10="1" Peripheral clock off VC27="0"		0.8	3.0	µA

Note
1: The power supply current measuring is executed using the measuring program on frash memory.
2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: VCC = 5V, VSS = 0V at Ta = 25 °C) [VCC=5V]

Table 5.11 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(XIN)	XIN input cycle time	62.5		ns
twH(XIN)	XIN input HIGH pulse width	30		ns
twL(XIN)	XIN input LOW pulse width	30		ns

Table 5.12 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CNTR0)	CNTR0 input cycle time	100		ns
twH(CNTR0)	CNTR0 input HIGH pulse width	40		ns
twL(CNTR0)	CNTR0 input LOW pulse width	40		ns

Table 5.13 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TCIN)	TCIN input cycle time	400 [1]		ns
twH(TCIN)	TCIN input HIGH pulse width	200 [2]		ns
twL(TCIN)	TCIN input LOW pulse width	200 [2]		ns

Note
1 : Use the greater value,either (1/ digital filter clock frequency x 6) or min. value.
2 : Use the greater value,either (1/ digital filter clock frequency x 3) or min. value.

Table 5.14 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input HIGH pulse width	100		ns
tw(CKL)	CLKi input LOW pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	35		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.15 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INT0}$ input HIGH pulse width	250 [1]		ns
tw(INL)	$\overline{INT0}$ input LOW pulse width	250 [2]		ns

Note
1 : When the $\overline{INT0}$ input filter select bit selects the digital filter, use the $\overline{INT0}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or min. value.
2 : When the $\overline{INT0}$ input filter select bit selects the digital filter, use the $\overline{INT0}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or min. value.

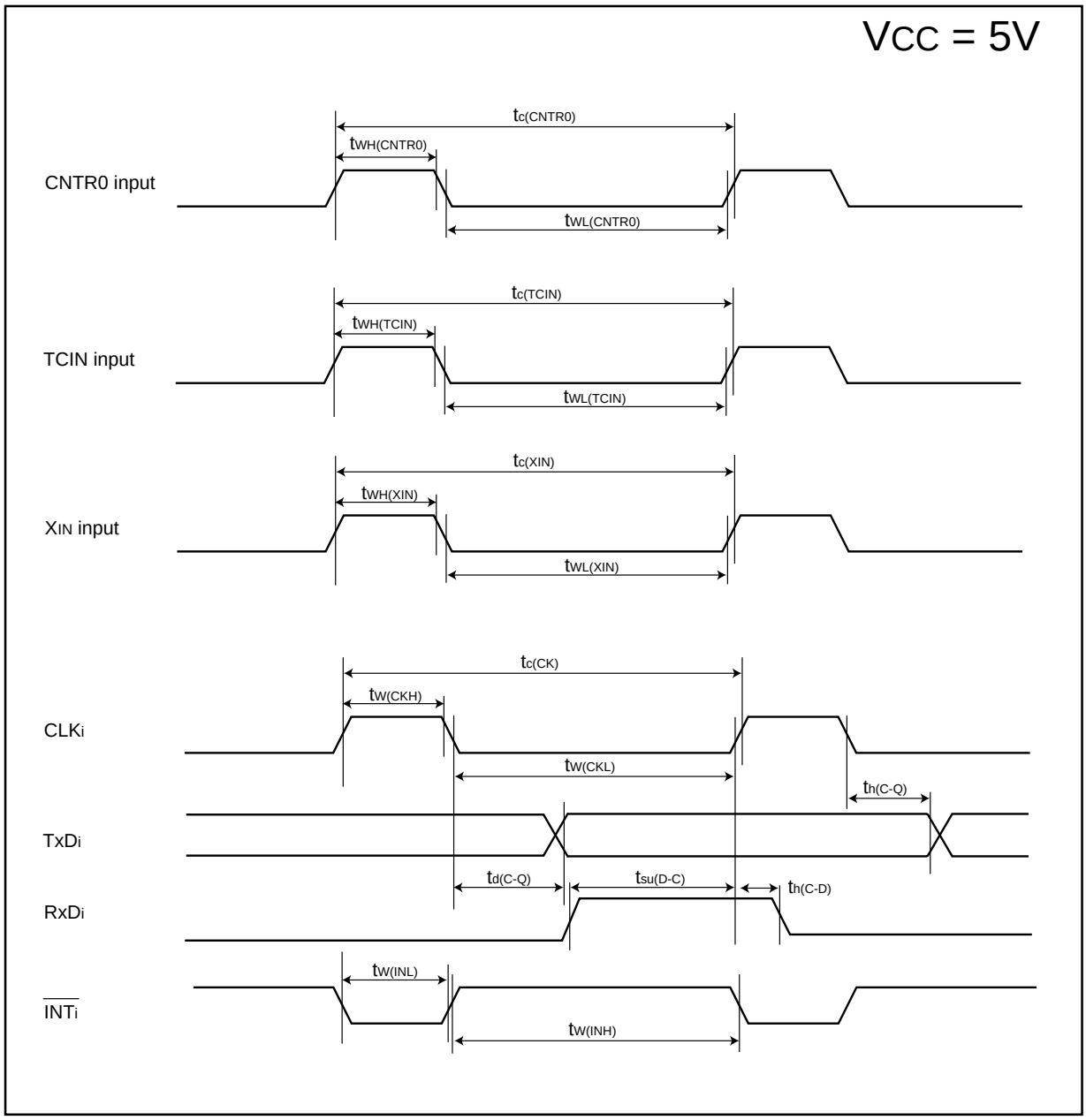


Figure 5.2 Vcc=5V timing diagram

Table 5.16 Electrical Characteristics (3) [Vcc=3V]

Symbol	Parameter		Measuring condition	Standard Min.	Standard Typ.	Standard Max.	Unit
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-1mA	V_{CC}-0.5		V_{CC}	V
		X_{OUT}	Drive ability HIGH I_{OH}=-0.1 mA	V_{CC}-0.5		V_{CC}	V
			Drive ability LOW I_{OH}=-50 µA	V_{CC}-0.5		V_{CC}	V
V_{OL}	"L" output voltage	P10 to P17 Except X_{OUT}	I_{OH}= 1 mA			0.5	V
		P10 to P17	Drive ability HIGH I_{OH}= 2 mA			0.5	V
			Drive ability LOW I_{OH}= 1 mA			0.5	V
		X_{OUT}	Drive ability HIGH I_{OH}= 0.1 mA			0.5	V
			Drive ability LOW I_{OH}=50 µA			0.5	V
V_{T+}-V_{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTRo, CNTR1, TCIN, RxD0, RxD1		0.2		0.8	V
		RESET		0.2		1.8	V
I_{IH}	"H" input current		V_I=3V			4.0	µA
I_{IL}	"L" input current		V_I=0V			-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V	66	160	500	kΩ
R_{fXIN}	Feedback resistance	X_{IN}			3.0		MΩ
f_{RING-S}	Low-speed ring oscillator frequency			40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode	2.0			V

Note
1 : Referenced to V_{CC}=AV_{CC}=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.

Table 5.17 Electrical Characteristics (4) [Vcc=3V]

Symbol	Parameter	Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
I_{CC}	Power supply current (V_{CC}=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V_{SS}	High-speed mode	X_{IN}=20 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		8	13	mA
			X_{IN}=16 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		7	12	mA
			X_{IN}=10 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		5		mA
		Medium-speed mode	X_{IN}=20 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		3		mA
			X_{IN}=16 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		2.5		mA
			X_{IN}=10 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		1.6		mA
		High-speed ring oscillator mode	Main clock off High-speed ring oscillator on=8 MHz Low-speed ring oscillator on=125 kHz No division		3.5	7.5	mA
			Main clock off High-speed ring oscillator on=8 MHz Low-speed ring oscillator on=125 kHz Division by 8		1.5		mA
		Low-speed ring oscillator mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		0.4	2.0	mA
		Wait mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation		37	74	µA
		Wait mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off		35	70	µA
		Stop mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator off CM10="1" Peripheral clock off VC27="0"		0.7	3.0	µA

Note
1: The power supply current measuring is executed using the measuring program on frash memory.
2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: VCC = 3V, VSS = 0V at Ta = 25 °C) [VCC=3V]

Table 5.18 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	143		ns
tWH(XIN)	XIN input HIGH pulse width	70		ns
tWL(XIN)	XIN input LOW pulse width	70		ns

Table 5.19 CNTR0 input, CNTR1 input, $\overline{\text{INT2}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	300		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	120		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	120		ns

Table 5.20 TCIN input, $\overline{\text{INT3}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	1200 [1]		ns
tWH(TCIN)	TCIN input HIGH pulse width	600 [2]		ns
tWL(TCIN)	TCIN input LOW pulse width	600 [2]		ns

Note
1 : Use the greater value,either (1/ digital filter clock frequency x 6) or min. value.
2 : Use the greater value,either (1/ digital filter clock frequency x 3) or min. value.

Table 5.21 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	300		ns
tW(CKH)	CLKi input HIGH pulse width	150		ns
tW(CKL)	CLKi input LOW pulse width	150		ns
td(C-Q)	TxDi output delay time		160	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	55		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.22 External interrupt $\overline{\text{INT0}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	$\overline{\text{INT0}}$ input HIGH pulse width	380 [1]		ns
tW(INL)	$\overline{\text{INT0}}$ input LOW pulse width	380 [2]		ns

Note
1 : When the $\overline{\text{INT0}}$ input filter select bit selects the digital filter, use the $\overline{\text{INT0}}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or min. value.
2 : When the $\overline{\text{INT0}}$ input filter select bit selects the digital filter, use the $\overline{\text{INT0}}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or min. value.

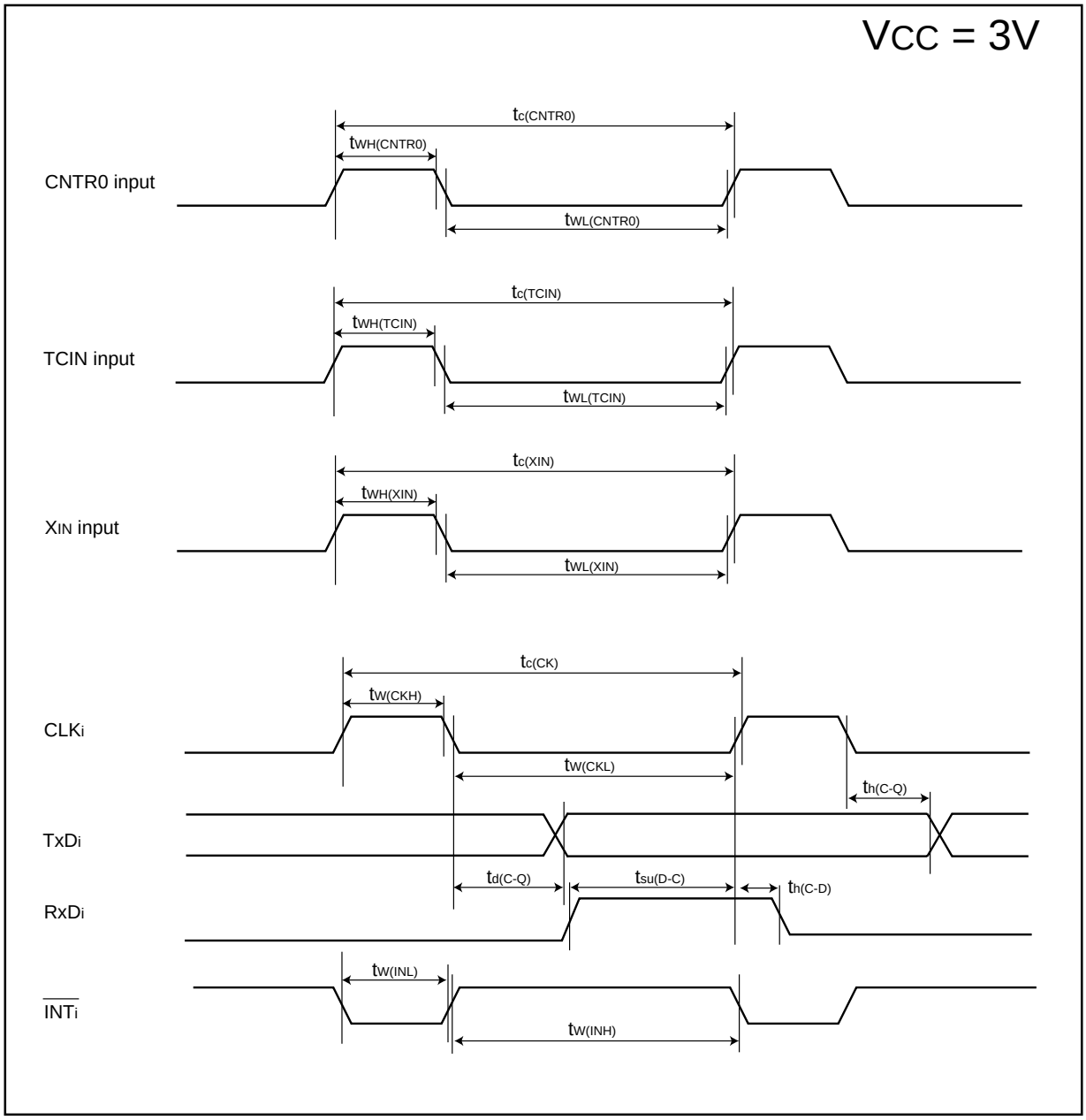
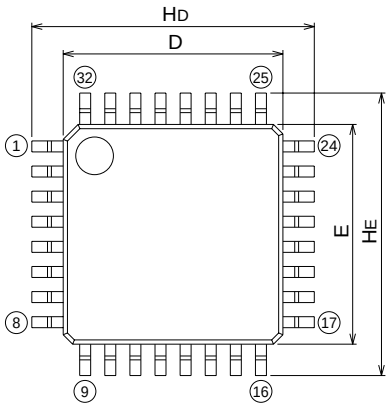


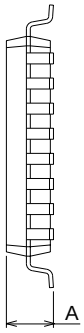
Figure 5.3 Vcc=3V timing diagram

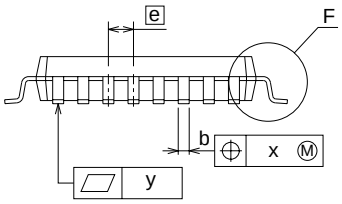
Package Dimensions

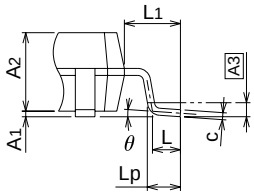
32P6U-A (MMP) **Plastic 32pin 7×7mm body LQFP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP32-P-0707-0.80	–		Cu Alloy









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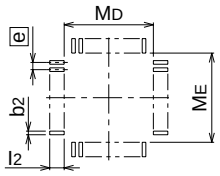

Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.8	–
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.2
y	–	–	0.1
θ	0°	–	10°
b2	–	0.5	–
I2	1.0	–	–
MD	–	7.4	–
ME	–	7.4	–

REVISION HISTORY	R8C/11 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 19, 2003		First edition issued
1.10	Sep. 08, 2003	2	Table 1.1: Shortest instruction execution time and f(X_{IN}) changed
		5	Figure 1.3: Pin name changed from TX_{OUT} to $\overline{CNTR_0}$
		6	Table 1.3: Pin name changed from TX_{OUT} to $\overline{CNTR_0}$
		10	The value of HR1 register after reset changed
		12	The value of TC register after reset changed
		14	Chapter “5. Electrical Characteristics” added
1.20	Oct. 31, 2003	2	Table 1.1: Power consumption values added
		6	Table 1.3: Resistor value for CNVss and MODE deleted
		11	Register name of address 0050_{16} modified from CMP2IC to CMP1IC, register name of address $005C_{16}$ modified from CMP1IC to CMP0IC
		14	Table 5.2: Note 3 and Note 4 deleted
		15	t_{samp} in Table 5.3 deleted
		17	Figure 5.1 added
		19	Table 5.10: Vcc changed from “4.2 to 5.5V” to “3.3V to 5.5V”, low-power ring oscillator changed from “on 100kHz” to “125kHz”, X_{IN}=5MHz deleted and X_{IN}=10MHz added in high-speed mode and medium-speed mode, VC27=”0” added in stop mode measuring condition, data added and modified
		20	Table 11 to Table 15 added
		21	Figure 5.2 added
		22	Table 5.16: Note 1, $f_{(BCLK)}$=5 MHz changed to 10 MHz
		23	Table 5.17: low-power ring oscillator changed from “on 100kHz” to “125kHz”, X_{IN}=5MHz deleted and X_{IN}=10MHz added in high-speed mode and medium-speed mode, VC27=”0” added in stop mode measuring condition, data added and modified
		24	Table 5.18 to Table 5.22 added
		25	Figure 5.3 added

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