![ST logo]

STR71xF

ARM7TDMI™ 16/32-BIT MCU WITH FLASH, USB, CAN 5 TIMERS, ADC, 10 COMMUNICATIONS INTERFACES

PRODUCT PREVIEW

■ **Memories**
- Up to 272 Kbytes (256+16K) FLASH program memory (100,000 cycles endurance, data retention 20 years)
- Up to 64 Kbytes RAM
- External Memory Interface (EMI) for up to 4 banks of SRAM, Flash, ROM.
- Multi-boot capability

■ **Clock, Reset and Supply Management**
- 3.3V application supply and I/O interface
- Embedded 1.8V voltage regulator for core supply
- 0 to 16 MHz external main oscillator
- 32 kHz external backup oscillator
- Internal PLL for CPU clock
- Up to 50 MHz CPU operating frequency when executing from flash
- Realtime Clock for clock-calendar function
- 4 power saving modes: SLOW, WAIT, STOP and STANDBY modes

■ **Nested interrupt controller**
- Fast interrupt handling with multiple vectors
- 32 vectors with 16 IRQ priority levels
- 2 maskable FIQ sources

■ **Up to 48 I/O ports**
- 30/32/48 multifunctional bidirectional I/O lines
- 14 ports with interrupt capability

■ **5 Timers**
- 16-bit watchdog timer
- Four 16-bit timers each with: 2 input captures, 2 output compares, PWM and pulse counter modes

TQFP64
10 x 10

TQFP144
20 x 20
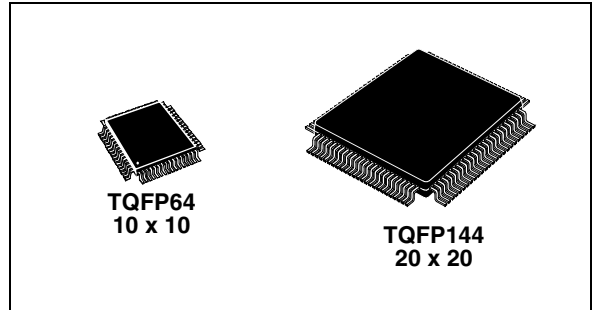
■ **10 Communications Interfaces**
- 2 I²C interfaces (1 multiplexed with SPI)
- 4 UART asynchronous serial communications interfaces
- Smart Card ISO7816-3 interface on UART1
- 2 BSPI synchronous serial interfaces
- CAN interface (2.0B Active)
- USB v 2.0 Full Speed (12Mbit/s) Device Function with Suspend and Resume support
- HDLC synchronous communications interface

■ **4-channel 12-bit A/D Converter**
- Conversion time:
  - 4 channels: up to 500 Hz (2 ms)
  - 1 channel: up to 1 kHz (1 ms)
- Conversion range: 0 to 2.5V

■ **Development Tools Support**
- JTAG with debug mode trigger request

Table 1. Device Summary

Features	STR710F		STR711F		STR712F	
	Z1T6	**Z2T6**	**R1T6**	**R2T6**	**R1T6**	**R2T6**
FLASH memory - Kbytes	128+16	256+16	128+16	256+16	128+16	256+16
RAM - Kbytes	16	64	16	64	16	64
Peripheral Functions	CAN, EMI, USB, 48 I/Os		USB, 30 I/Os		CAN, 32 I/Os	
Operating Voltage	3.0 to 3.6V (optional 1.8V for core)					
Operating Temperature	-40 to +85°C					
Packages	TQFP144 20x20		TQFP64 10x10			

Rev. 4

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Table of Contents

Note: For detailed information on the STR71xF Microcontroller memory, registers and peripherals. please refer to the STR71xF Reference Manual.

1 INTRODUCTION

This Product Preview provides the STR71x Ordering Information, Mechanical and Electrical Device Characteristics.

For complete information on the STR71xF Microcontroller memory, registers and peripherals. please refer to the STR71xF Reference Manual.

For information on the ARM7TDMI core please refer to the ARM7TDMI Technical Reference Manual.

1.1 Overview

ARM® core with embedded Flash & RAM

The STR71xF series is a family of ARM-powered 16/32bit Micro-controllers with embedded Flash and RAM. It combines the high performance ARM7TDMI CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage FLASH memory and high-speed RAM. The STR71xF family has an embedded ARM core and is therefore compatible with all ARM tools and software.

For information on the **ARM Realview Developer Kit for ST** and third-party development tools, please refer to the http://www.st.com website

Package Choice: Low Pin-Count TQFP64 or Feature-Rich TQFP144

The STR71xF family is available in 2 package sizes. The 144-pin version has the full set of all features including CAN, USB and External Memory Interface. The two 64-pin versions do not include External Memory Interface and give you the choice of either CAN or USB.

Optional External Memory (STR710F)

The non-multiplexed 16-bit data/24-bit address bus available on the STR710F (TQFP144) supports four 16-Mbyte banks of external memory. Wait states are programmable individually for each bank allowing different memory types (Flash, EPROM, ROM, SRAM etc.) to be used to store programs or data.

Figure 1 shows the general block diagram of the device family.

Flexible Power Management

To minimize power consumption, you can program the STR71xF to switch to SLOW, WAIT FOR INTERRUPT, STOP or STANDBY mode depending on the current system activity in the application.

Flexible Clock Control

Two external clock sources can be used, a main clock and a 32 kHz backup clock. The embedded PLL allows the internal system clock (up to 50 MHz) to be generated from a main clock frequency of 16 MHz or less. The PLL output frequency can be programmed using a wide selection of multipliers and dividers.

Voltage Regulators

The STR71xF requires an external 3.0-3.6V power supply. There are two internal Voltage Regulators for generating the 1.8V power supply for the core and peripherals. The main VR is switched off and the Low Power VR switched on when the application puts the STR71xF in Standby or Low Power Wait for Interrupt (LPWFI) mode.

Low Voltage Detectors

Each voltage regulator has an embedded LVD that monitors the internal 1.8V supply. If the voltage drops below a certain threshold, the LVD will reset the STR71xF.

On-Chip Peripherals

CAN Interface (STR710F and STR712F)

The CAN module is compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud.

USB Interface (STR710F and STR711F)

The full-speed USB interface is USB V2.0 compliant and provides up to 8 bidirectional/16 unidirectional endpoints, up to 12 Mb/s (full-speed), support for bulk transfer and USB Suspend/Resume functions.

Standard Timers

Each of the four timers have a 16-bit free-running counter with 7-bit prescaler, up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency.

Realtime Clock (RTC)

The RTC provides a set of continuously running counters driven by a low power 32kHz internal oscillator. The RTC can be used as a general timebase or clock/calendar/alarm function. When the STR71xF is in Standby mode the RTC can be kept running, powered by the low power voltage regulator and driven by the 32kHz internal oscillator.

UARTs

The 4 UARTs allow full duplex, asynchronous, communications with external devices with independently programmable TX and RX baud rates up to 625 kb/s.

Smart Card Interface

UART1 is configurable to function either as a general purpose UART or as an asynchronous Smart Card interface as defined by ISO 7816-3. It includes Smart Card clock generation and provides support features for synchronous cards.

Buffered Serial Peripheral Interfaces (BSPI)

Each of the two SPIs allow full duplex, synchronous communications with external devices, master or slave communication at up to 5.5Mb/s in Master mode and 4 Mb/s in Slave mode.

I^2C Interfaces

The two I^2C Interfaces provide multi-master and slave functions, support normal and fast I^2C mode (400 kHz) and 7 or 10-bit addressing modes.

One I^2C Interface is multiplexed with one SPI, so either 2xSPI+1x I^2C or 1xSPI+2x I^2C may be used at a time.

HDLC interface

The High Level Data Link Controller (HDLC) unit supports full duplex operation and NRZ, NRZI, FM0 or MANCHESTER protocols. It has an internal 8-bit baud rate generator.

A/D Converter

The Analog to Digital Converter, converts in single channel or up to 4 channels in single-shot or continuous conversion modes. Resolution is 12-bit with a sample rate of 0.5 kHz (1 kHz in single channel mode). The input voltage range is 0-2.5V.

Watchdog

The 16-bit Watchdog Timer protects the application against hardware or software failures and ensures recovery by generating a reset.

I/O Ports

The 48 I/O ports are programmable as Inputs or Outputs.

External Interrupts

Up to 14 external interrupts are available for application use or to wake-up the application from STOP mode.

Figure 1. STR71xF Block Diagram
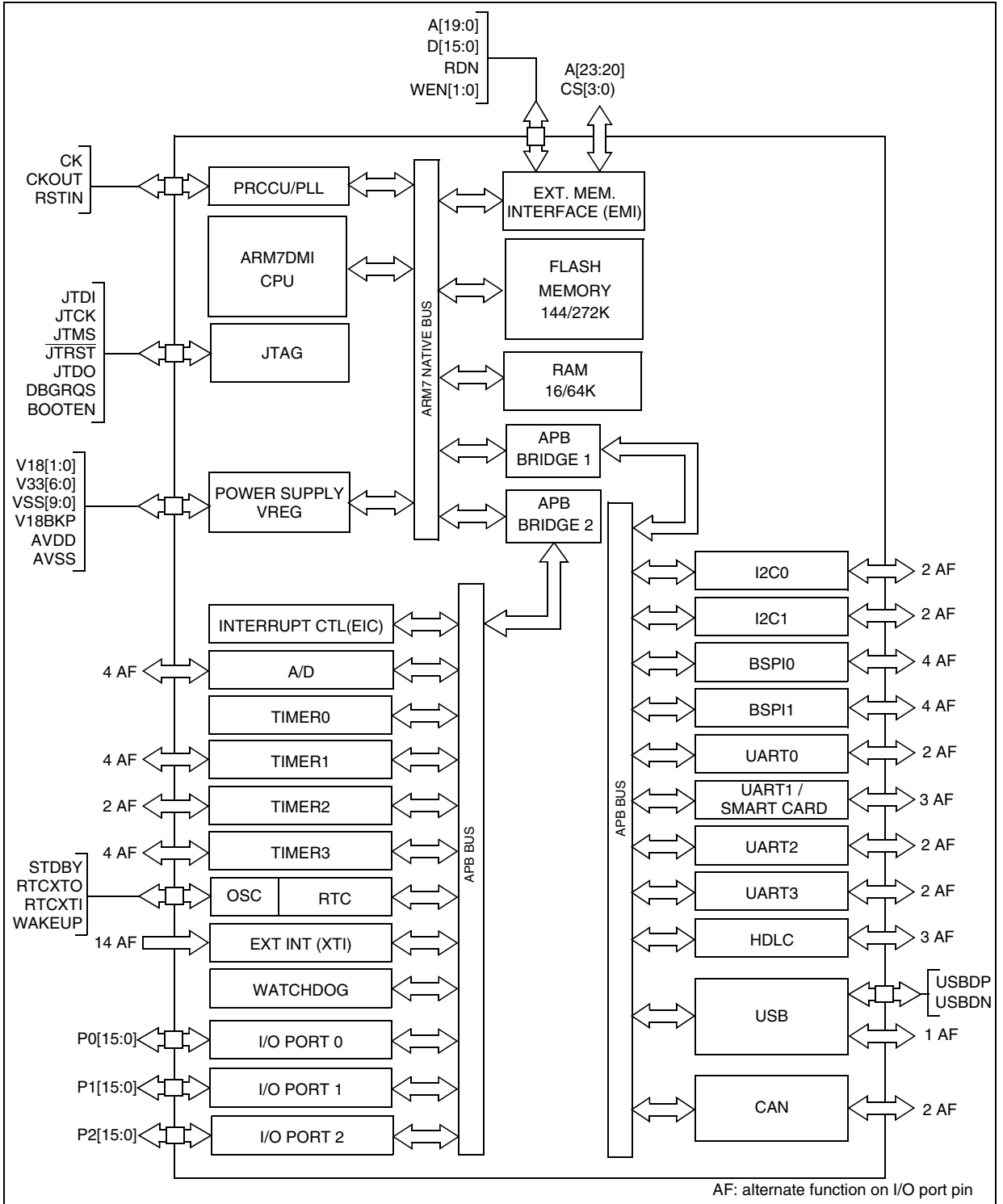
1.2 Related Documentation

Available from www.arm.com:

ARM7TDMI Technical Reference Manual

Available from http://www.st.com:

STR71x Reference Manual

AN1774 - Getting Started with STR71xF Software development

AN1775 - Getting Started with STR71xF Hardware development

AN1776 - STR71xF Enhanced Interrupt Controller

AN1777 - STR71xF Memory Mapping

AN1778 - STR71xF Multi-ICE Setup

AN1780 - Real Time Clock with STR71xF

AN1781 - Four 7 Segment Display Drive Using the STR71xF

The above is a selected list only, a full list STR71x application notes can be viewed at http://www.st.com.

1.3 Pin Description

Figure 2. STR710F Package Pinout

Figure 3. STR712F Package Pinout

Top pins (left to right, 64 to 49):
64 P0.9/U0.TX/BOOT.0
63 P0.8/U0.RX/U0.TX
62 P0.7/S1.SSN
61 P0.6/S1.SCLK
60 P0.5/S1.MOSI
59 VSS
58 V18
57 VSS18
56 P0.4/S1.MISO
55 P0.3/S0.SSN/I1.SDA
54 P0.2/S0.SCLK/I1.SCL
53 P0.1/S0.MOSI/U3.RX
52 P0.0/S0.MISO/U3.TX
51 V33
50 VSS
49 P1.15/HTXD

Left side pins (1 to 16):
P0.10/U1.RX/U1.TX/SCDATA 1
P0.11/U1.TX/BOOT.1 2
P0.12/SCCLK 3
VSS 4
P0.13/U2.RX/T2.OCMPA 5
P0.14/U2.TX/T2.ICAPA 6
BOOTEN 7
VSS 8
V33 9
JTDI 10
JTMS 11
JTCK 12
JTDO 13
nJTRST 14
NU 15
TEST 16

TQFP64

Right side pins (48 to 33):
48 P1.14/HRXD/I0.SDA
47 P1.13/HCLK/I0.SCL
46 P1.10
45 P1.9
44 VSS
43 P1.12/CANTX
42 P1.11/CANRX
41 P1.8
40 P1.7/T1.OCMPA
39 VSSIO-PLL
38 V33IO-PLL
37 P1.6/T1.OCMPB
36 P1.5/T1.ICAPB
35 P1.4/T1.ICAPA
34 P1.3/T3.ICAPB/AIN.3
33 P1.2/T3.OCMPA/AIN.2

Bottom pins (17 to 32):
17 V33IO-PLL
18 VSSIO-PLL
19 CK
20 P0.15/WAKEUP
21 RTCXTI
22 RTCXTO
23 nSTDBY
24 nRSTIN
25 VSSBKP
26 V18BKP
27 V18
28 VSS18
29 AVDD
30 AVSS
31 P1.0/T3.OCMPB/AIN.0
32 P1.1/T3.ICAPA/AIN.1

Figure 4. STR711F Package Pinout

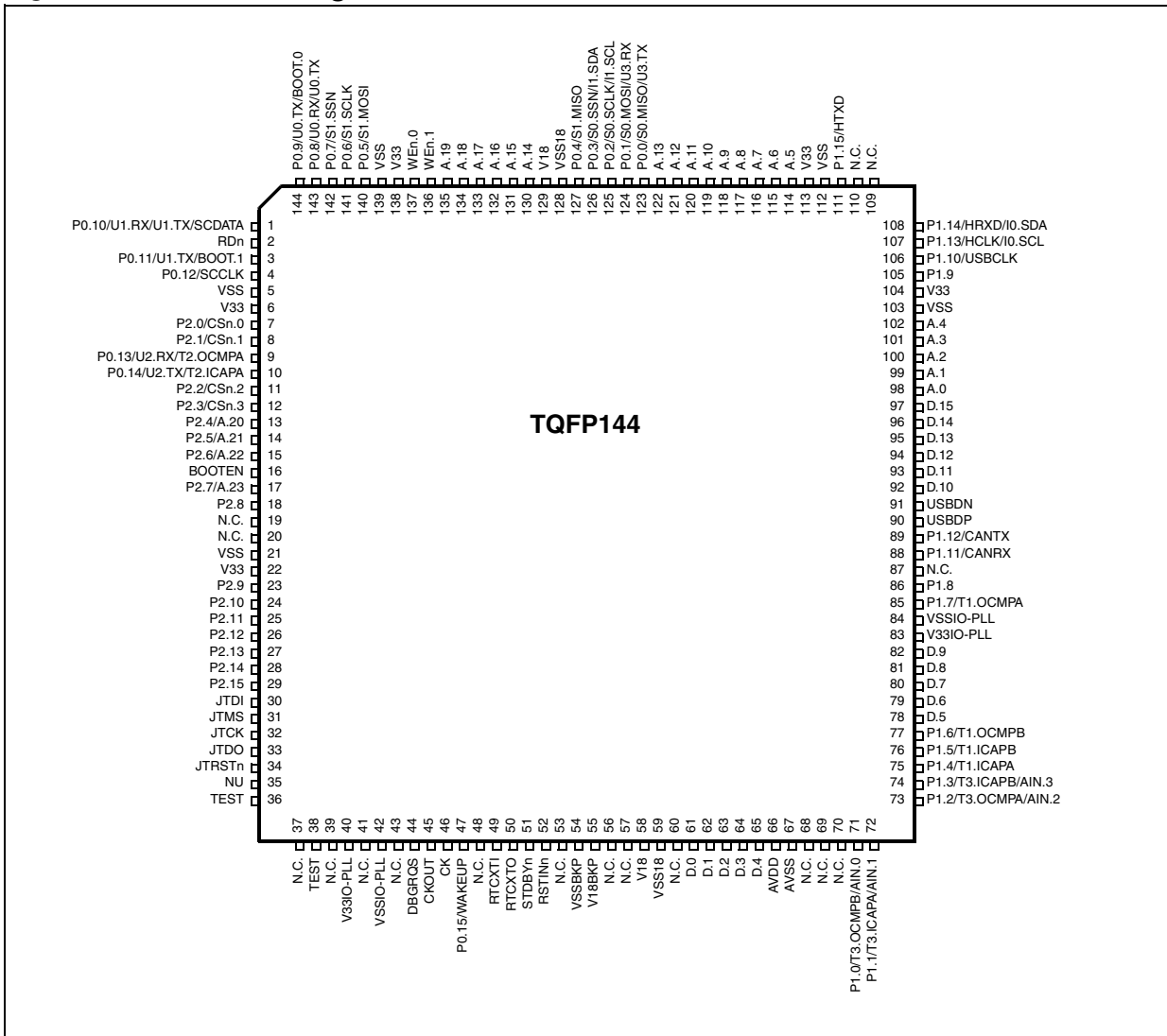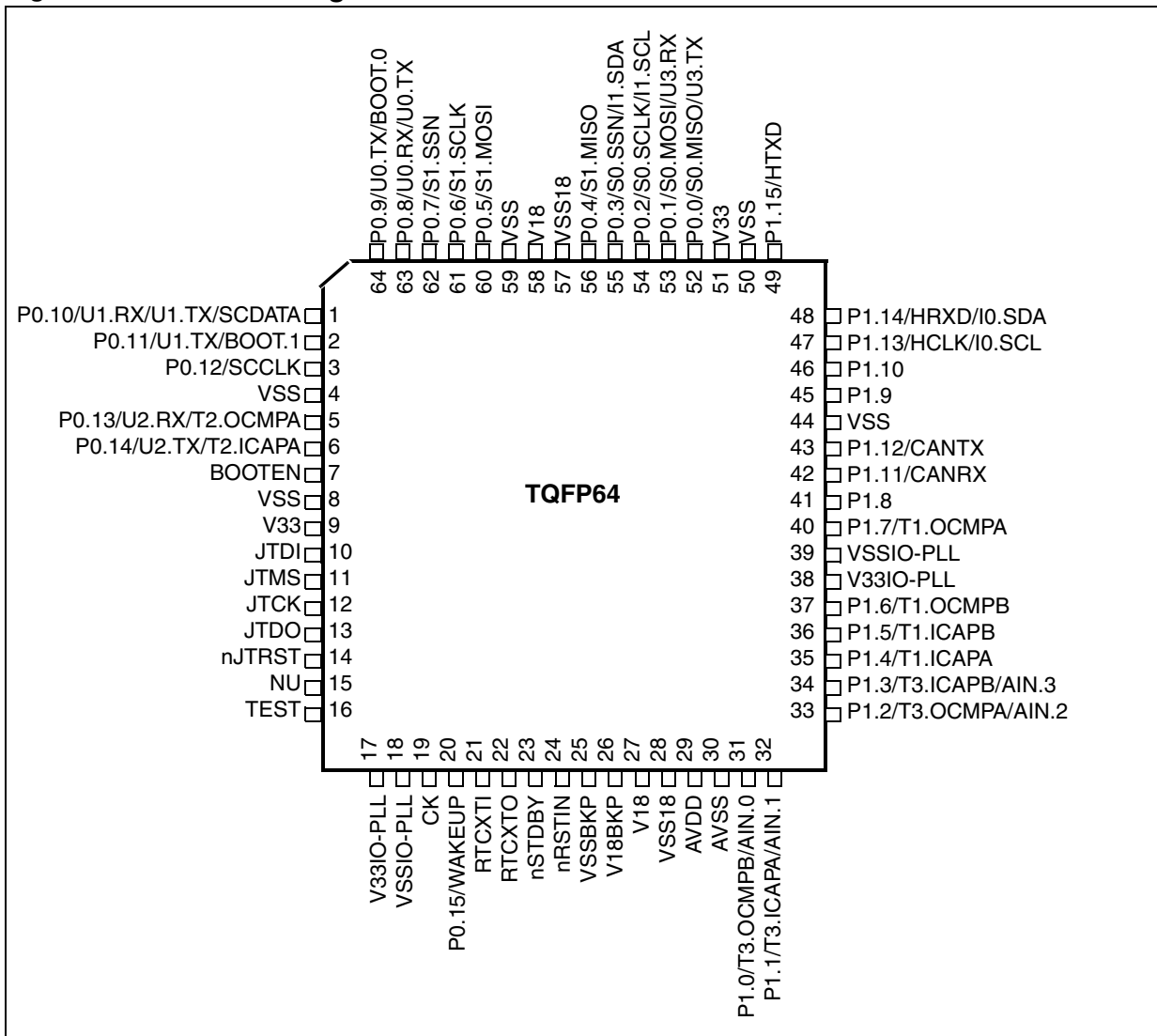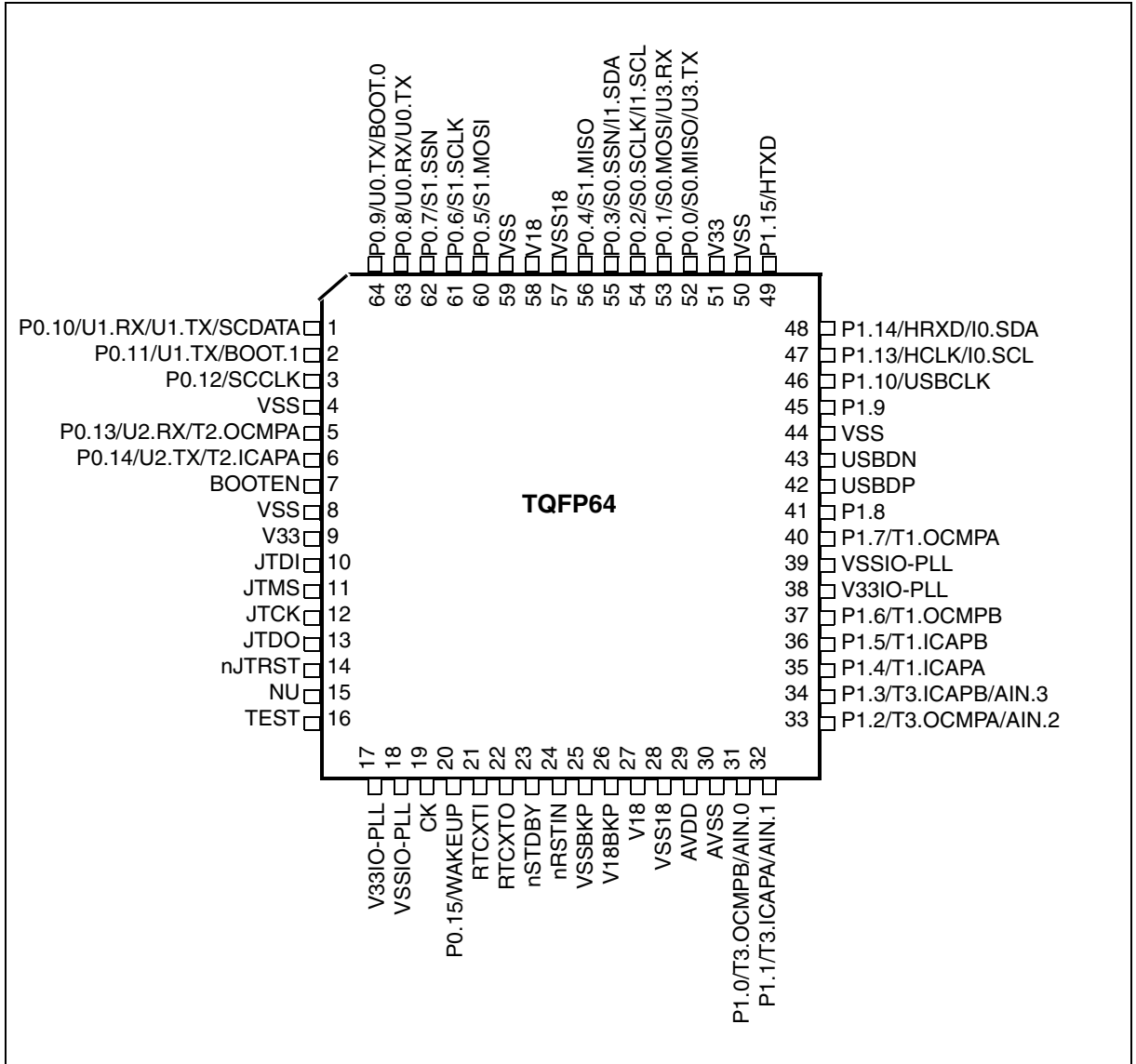**Legend / Abbreviations for** Table 2**:**

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
          C_T= CMOS 0.8V / 2V with input trigger
          T_T= TTL $0.3V_{DD}/0.7V_{DD}$ with input trigger
          C/T = Programmable levels: CMOS $0.3V_{DD}/0.7V_{DD}$ or TTL 0.8V / 2V

Port and control configuration:

– Input: pu/pd= software enabled internal pull-up or pull down
          pu= in reset state, the internal 100kΩ weak pull-up is enabled.
          pd = in reset state, the internal 100kΩ weak pull-down is enabled.

– Output: OD = open drain (logic level)
          PP = push-pull
          T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5V tolerant.

Note: The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to Table 3, "Port Bit Configuration Table," on page 18. The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column in Table 2 below, which specifies whether the pull-up or pull-down is enabled at reset

Table 2. Device Pin Description

Pin n°		Pin Name	Type	Input			Output			Active in Stdby	Main function (after reset)	Alternate function	
TQFP144	TQFP64			InputLevel	pu/ pd	interrupt	Capability	OD	PP				
1	1	P0.10/U1.RX/ U1.TX/ SC.DATA	I/O	C_T	pd 2)	X	4mA	T			Port 0.10	UART1: Receive Data input	UART1: Transmit data output.
												Note: This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress	
2	-	$\overline{RD}$	O						X		External Memory Interface: Active low read signal for external memory. It maps to the OE_N input of the external components.		
3	2	P0.11/ BOOT.1/ U1.TX	I/O	C_T	pd 2)		4mA	X	X		Port 0.11	Select Boot Configuration input	UART1: Transmit data output.
4	3	P0.12/SC.CLK	I/O	C_T	pd 2)		4mA				Port 0.12	Smartcard reference clock output	
5	4	V_{SS}	S								Ground voltage for digital I/Os		
6	-	V_{33}	S								Supply voltage for digital I/Os		
7	-	P2.0/$\overline{CS}$.0	I/O	C_T	pu		8mA	X	X		Port 2.0	External Memory Interface: Select Memory Bank 0 output	
												Note: This pin is forced to output mode at reset to allow boot from external memory	
8	-	P2.1/$\overline{CS}$.1	I/O	C_T	pu 1)		8mA	X	X		Port 2.1	External Memory Interface: Select Memory Bank 1 output	
9	5	P0.13/U2.RX/ T2.OCMPA	I/O	C_T	pu	X	4mA	X	X		Port 0.13	UART2: Receive Data input	Timer2: Output Compare A output

| Pin n° | | Pin Name | Type | Input | | | | Output | | Active in Stdby | Main function (after reset) | Alternate function | |
TQFP144	TQFP64			InputLevel	pu/ pd	interrupt	Capability	OD	PP				
10	6	P0.14/U2.TX/ T2.ICAPA	I/O	C_T	pu		4mA	X	X		Port 0.14	UART2: Transmit data output	Timer2: Input Capture A input
11	-	P2.2/$\overline{CS}$.2	I/O	C_T	pu 1)		8mA	X	X		Port 2.2	External Memory Interface: Select Memory Bank 3 output	
12	-	P2.3/$\overline{CS}$.3	I/O	C_T	pu 1)		8mA	X	X		Port 2.3	External Memory Interface: Select Memory Bank 4 output	
13	-	P2.4/A.20	I/O	C_T	pd 2)		8mA	X	X		Port 2.4	External Memory Interface: address bus	
14	-	P2.5/A.21	I/O	C_T	pd 2)		8mA	X	X		Port 2.5		
15	-	P2.6/A.22	I/O	C_T	pd 2)		8mA	X	X		Port 2.6		
16	7	BOOTEN	I	C_T							Boot control input. Enables sampling of BOOT[1:0] pins		
17	-	P2.7/A.23	I/O	C_T	pd 2)		8mA	X	X		Port 2.7	External Memory Interface: address bus	
18	-	P2.8	I/O	C_T	pu	X	4mA	X	X		Port 2.8	External interrupt INT2	
19	-	N.C.									Not connected (not bonded)		
20	-	N.C.									Not connected (not bonded)		
21	8	V_{SS}	S								Ground voltage for digital I/Os		
22	9	V_{33}	S								Supply voltage for digital I/Os		
23	-	P2.9	I/O	C_T	pu	X	4mA	X	X		Port 2.9	External interrupt INT3	
24	-	P2.10	I/O	C_T	pu	X	4mA	X	X		Port 2.10	External interrupt INT4	
25	-	P2.11	I/O	C_T	pu	X	4mA	X	X		Port 2.11		
26	-	P2.12	I/O	C_T	pu		4mA	X	X		Port 2.12		
27	-	P2.13	I/O	C_T	pu		4mA	X	X		Port 2.13		
28	-	P2.14	I/O	C_T	pu		4mA	X	X		Port 2.14		
29	-	P2.15	I/O	C_T	pu		4mA	X	X		Port 2.15		
30	10	JTDI	I	T_T							JTAG Data input. External pull-up required.		
31	11	JTMS	I	T_T							JTAG Mode Selection Input. External pull-up required.		
32	12	JTCK	I	C							JTAG Clock Input. External pull-up or pull-down required.		
33	13	JTDO	O					8mA		X		JTAG Data output. **Note:** Reset state = HiZ.		
34	14	$\overline{JTRST}$	I	T_T							JTAG Reset Input. External pull-up required.		
35	15	NU									Reserved, must be forced to ground.		
36	16	TEST									Reserved, must be forced to ground.		
37	-	N.C.									Not connected (not bonded)		

Pin n° TQFP144	Pin n° TQFP64	Pin Name	Type	Input InputLevel	Input pu/pd	Input interrupt	Input Capability	Output OD	Output PP	Active in Stdby	Main function (after reset)	Alternate function
38	-	TEST									Reserved, must be forced to ground.	
39	-	N.C.									Not connected (not bonded)	
40	17	$V_{33IO\text{-}PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference	
41	-	N.C.									Not connected (not bonded)	
42	18	$V_{SSIO\text{-}PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference	
43	-	N.C.									Not connected (not bonded)	
44	-	DBGRQS	I	C_T							Debug Mode request input (active high)	
45	-	CKOUT	O				8mA		X		Clock output (f_{PCLK2}) **Note:** Enabled by CKDIS register in APB Bridge 2	
46	19	CK	I	C							Reference clock input	
47	20	P0.15/WAKE-UP	I	T_T	pu	X	4mA			X	Port 0.15	Wakeup from Standby mode input.
48	-	N.C.									Not connected (not bonded)	
49	21	RTCXTI									Realtime Clock input and input of 32 kHz oscillator amplifier circuit	
50	22	RTCXTO									Output of 32 kHz oscillator amplifier circuit	
51	23	$\overline{STDBY}$	I/O	C_T			4mA	X		X	Input: Hardware Standby mode entry input active low. **Caution:** External pull-up to V_{33} required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. **Note**: In Standby mode all pins are in high impedance except those marked Active in Stdby	
52	24	$\overline{RSTIN}$	I	C_T						X	Reset input	
53	-	N.C.									Not connected (not bonded)	
54	25	V_{SSBKP}		S						X	Stabilisation for low power voltage regulator.	
55	26	V_{18BKP}		S						X	Stabilisation for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and $V_{SS18BKP}$. See Figure 5. **Note:** If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.	
56	-	N.C.									Not connected (not bonded)	
57	-	N.C.									Not connected (not bonded)	
58	27	V_{18}		S							Stabilisation for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See Figure 5.	
59	28	V_{SS18}		S							Stabilisation for main voltage regulator.	
60	-	N.C.									Not connected (not bonded)	

Pin n°		Pin Name	Type	Input				Output		Active in Stdby	Main function (after reset)	Alternate function	
TQFP144	TQFP64			InputLevel	pu/ pd	interrupt	Capability	OD	PP				
61	-	D.0	I/O				8mA				External Memory Interface: data bus		
62	-	D.1	I/O				8mA						
63	-	D.2	I/O				8mA						
64	-	D.3	I/O				8mA						
65	-	D.4	I/O				8mA						
66	29	V$_{DDA}$	S								Supply voltage for A/D Converter		
67	30	V$_{SSA}$	S								Ground voltage for A/D Converter		
68	-	N.C.									Not connected (not bonded)		
69	-	N.C.									Not connected (not bonded)		
70	-	N.C.									Not connected (not bonded)		
71	31	P1.0/T3.OC-MPB/AIN.0	I/O	C$_T$	pu		4mA	X	X		Port 1.0	Timer 3: Output Compare B	ADC: Analog input 0
72	32	P1.1/T3.ICA-PA/T3.EXT-CLK/AIN.1	I/O	C$_T$	pu		4mA	X	X		Port 1.1	Timer 3: Input Capture A or External Clock input	ADC: Analog input 1
73	33	P1.2/T3.OCM-PA/AIN.2	I/O	C$_T$	pu		4mA	X	X		Port 1.2	Timer 3: Output Compare A	ADC: Analog input 2
74	34	P1.3/T3.ICAPB/AIN.3	I/O	C$_T$	pu		4mA	X	X		Port 1.3	Timer 3: Input Capture B	ADC: Analog input 3
75	35	P1.4/T1.ICA-PA/T1.EXT-CLK	I/O	C$_T$	pu		4mA	X	X		Port 1.4	Timer 1: Input Capture A	Timer 1: External Clock input
76	36	P1.5/T1.ICAPB	I/O	C$_T$	pu		4mA	X	X		Port 1.5	Timer 1: Input Capture B	
77	37	P1.6/T1.OC-MPB	I/O	C$_T$	pu		4mA	X	X		Port 1.6	Timer 1: Output Compare B	
78	-	D.5	I/O				8mA				External Memory Interface: data bus		
79	-	D.6	I/O				8mA						
80	-	D.7	I/O				8mA						
81	-	D.8	I/O				8mA						
82	-	D.9	I/O				8mA						
83	38	V$_{33IO-PLL}$		S							Supply voltage for digital I/O circuitry and for PLL reference		
84	39	V$_{SSIO-PLL}$		S							Ground voltage for digital I/O circuitry and for PLL reference		
85	40	P1.7/T1.OCM-PA	I/O	C$_T$	pu		4mA	X	X		Port 1.7	Timer 1: Output Compare A	
86	41	P1.8	I/O	C$_T$	pd		4mA	X	X		Port 1.8		
87	-	N.C.									Not connected (not bonded)		
88	42	P1.11/CANRX	I/O	C$_T$	pu	X	4mA	X	X		Port 1.11	CAN: receive data input **Note:** On STR710 and STR712 only	

Pin n° TQFP144	TQFP64	Pin Name	Type	Input InputLevel	pu/pd	interrupt	Output Capability	OD	PP	Active in Stdby	Main function (after reset)	Alternate function	
89	43	P1.12/CANTX	I/O	C_T	pu	X	4mA	X	X		Port 1.12	CAN: Transmit data output **Note:** On STR710 and STR712 only	
90	42	USBDP	I/O	C_T								USB bidirectional data (data +). Reset state = HiZ **Note:** On STR710 and STR711 only This pin requires an external pull-up to V_{33} to maintain a high level.	
91	43	USBDN	I/O	C_T								USB bidirectional data (data -). Reset state = HiZ **Note:** On STR710 and STR711 only.	
92	-	D.10	I/O				8mA					External Memory Interface: data bus	
93	-	D.11	I/O				8mA						
94	-	D.12	I/O				8mA						
95	-	D.13	I/O				8mA						
96	-	D.14	I/O				8mA						
97	-	D.15	I/O				8mA						
98	-	A.0	O				8mA					External Memory Interface: address bus	
99	-	A.1	O				8mA						
100	-	A.2	O				8mA						
101	-	A.3	O				8mA						
102	-	A.4	O				8mA						
103	44	V_{SS}	S									Ground voltage for digital I/O circuitry	
104	-	V_{33}	S									Supply voltage for digital I/O circuitry	
105	45	P1.9	I/O	C_T	pd		4mA	X	X		Port 1.9		
106	46	P1.10/USB-CLK	I/O	C/T	pu		4mA	X	X		Port 1.10	USB: 48 MHZ clock input	
107	47	P1.13/HCLK/I0.SCL	I/O	C_T	pu	X	4mA	X	X		Port 1.13	HDLC: reference clock input	I2C clock
108	48	P1.14/HRXD/I0.SDA	I/O	C_T	pu	X	4mA	X	X		Port 1.14	HDLC: Receive data input	I2C serial data
109	-	N.C.										Not connected (not bonded)	
110	-	N.C.										Not connected (not bonded)	
111	49	P1.15/HTXD	I/O	C_T	pu	X	4mA	X	X		Port 1.15	HDLC: Transmit data output	
112	50	V_{SS}	S									Ground voltage for digital I/O circuitry	
113	51	V_{33}	S									Supply voltage for digital I/O circuitry	

Pin n°		Pin Name	Type	Input			Output			Active in Stdby	Main function (after reset)	Alternate function	
TQFP144	TQFP64			InputLevel	pu/ pd	interrupt	Capability	OD	PP				
114	-	A.5	O				8mA				External Memory Interface: address bus		
115	-	A.6	O				8mA						
116	-	A.7	O				8mA						
117	-	A.8	O				8mA						
118	-	A.9	O				8mA						
119	-	A.10	O				8mA						
120	-	A.11	O				8mA						
121	-	A.12	O				8mA						
122	-	A.13	O				8mA						
123	52	P0.0/S0.MISO/U3.TX	I/O	C_T	pu		4mA	X	X		Port 0.0	SPI0 Master in/Slave out data	UART3 Transmit data output
												Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
124	53	P0.1/S0.MOSI/U3.RX	I/O	C_T	pu	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data	UART3: Receive Data input
												Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
125	54	P0.2/S0.SCLK/I1.SCL	I/O	C_T	pu	X	4mA	X	X		Port 0.2	BSPI0: Serial Clock	I2C1: Serial clock
												Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
126	55	P0.3/S0.$\overline{SS}$/I1.SDA	I/O	C_T	pu		4mA	X	X		Port 0.3	SPI0: Slave Select input active low.	I2C1: Serial Data
												Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
127	56	P0.4/S1.MISO	I/O	C_T	pu		4mA	X	X		Port 0.4	SPI1: Master in/Slave out data	
128	57	V_{SS18}	S								Stabilisation for main voltage regulator.		
129	58	V_{18}	S								Stabilisation for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See Figure 5.		
130	-	A.14	O				8mA				External Memory Interface: address bus		
131	-	A.15	O				8mA						
132	-	A.16	O				8mA						
133	-	A.17	O				8mA						
134	-	A.18	O				8mA						
135	-	A.19	O				8mA						
136	-	$\overline{WE}$.1	O				8mA				External Memory Interface: active low MSB write enable output		

Pin n°		Pin Name	Type	Input			Output			Active in Stdby	Main function (after reset)	Alternate function	
TQFP144	TQFP64			InputLevel	pu/ pd	interrupt	Capability	OD	PP				
137	-	$\overline{WE}$.0	O				8mA				External Memory Interface: active low LSB write enable output		
138	-	V_{33}	S								Supply voltage for digital I/Os		
139	59	V_{SS}	S								Ground voltage for digital I/Os		
140	60	P0.5/S1.MOSI	I/O	C_T	pu		4mA	X	X		Port 0.5	SPI1: Master out/Slave In data	
141	61	P0.6/S1.SCLK	I/O	C_T	pu	X	4mA	X	X		Port 0.6	SPI1: Serial Clock	
142	62	P0.7/S1.$\overline{SS}$	I/O	C_T	pu		4mA	X	X		Port 0.7	SPI1: Slave Select input active low	
143	63	P0.8/U0.RX/ U0.TX	I/O	C_T	pd	X	4mA	T			Port 0.8	UART0: Receive Data input	UART0: Transmit data output.
											Note: This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress		
144	64	P0.9/U0.TX/ BOOT.0	I/O	C_T	pd		4mA	X	X		Port 0.9	Select Boot Configuration input	UART0: Transmit data output

1. In reset state, these pins configured as Input PU/PD with weak pull-up enabled. They must be configured by software as Alternate Function (see Table 3, "Port Bit Configuration Table," on page 18) to be used by the External Memory Interface.

2. In reset state, these pins configured as Input PU/PD with weak pull-down enabled to output Address 0x0000 0000 using the External Memory Interface. To access memory banks greater than 1Mbyte, they need to be configured by software as Alternate Function (see Table 3, "Port Bit Configuration Table," on page 18).

Figure 5. Recommended External Connection of $V_{18\ and}$ V_{18BKP} pins
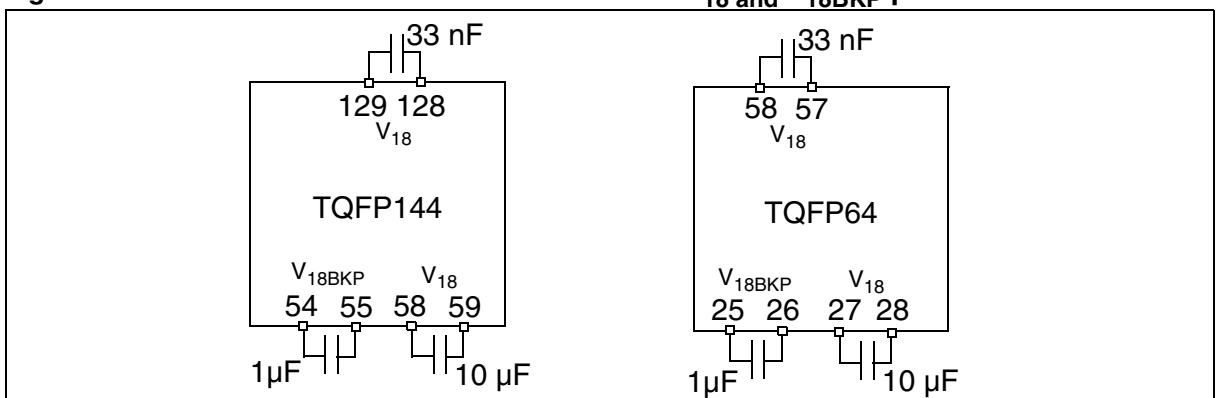
Table 3. Port Bit Configuration Table

Port Configuration Registers (bit)	Values							
PC0(n)	0	1	0	1	0	1	0	1
PC1(n)	0	0	1	1	0	0	1	1
PC2(n)	0	0	0	0	1	1	1	1
Configuration	HiZ/AIN	IN	IN	IPUPD	OUT	OUT	AF	AF
Output	TRI	TRI	TRI	WP	OD	PP	OD	PP
Input	AIN	TTL	CMOS	CMOS	N.A.	N.A.	CMOS	CMOS

Notes:

AF: Alternate Function

AIN: Analog Input

IPUPD: Input Pull Up /Pull Down

CMOS: CMOS Input levels

HiZ: High impedance

IN: Input

N.A. not applicable. In Output mode, a read access to the port gets the output latch value).

OD: Open Drain

OUT: Output

PP: Push-Pull

TRI: Tristate

TTL: TTL Input levels

WP: Weak Push-Pull
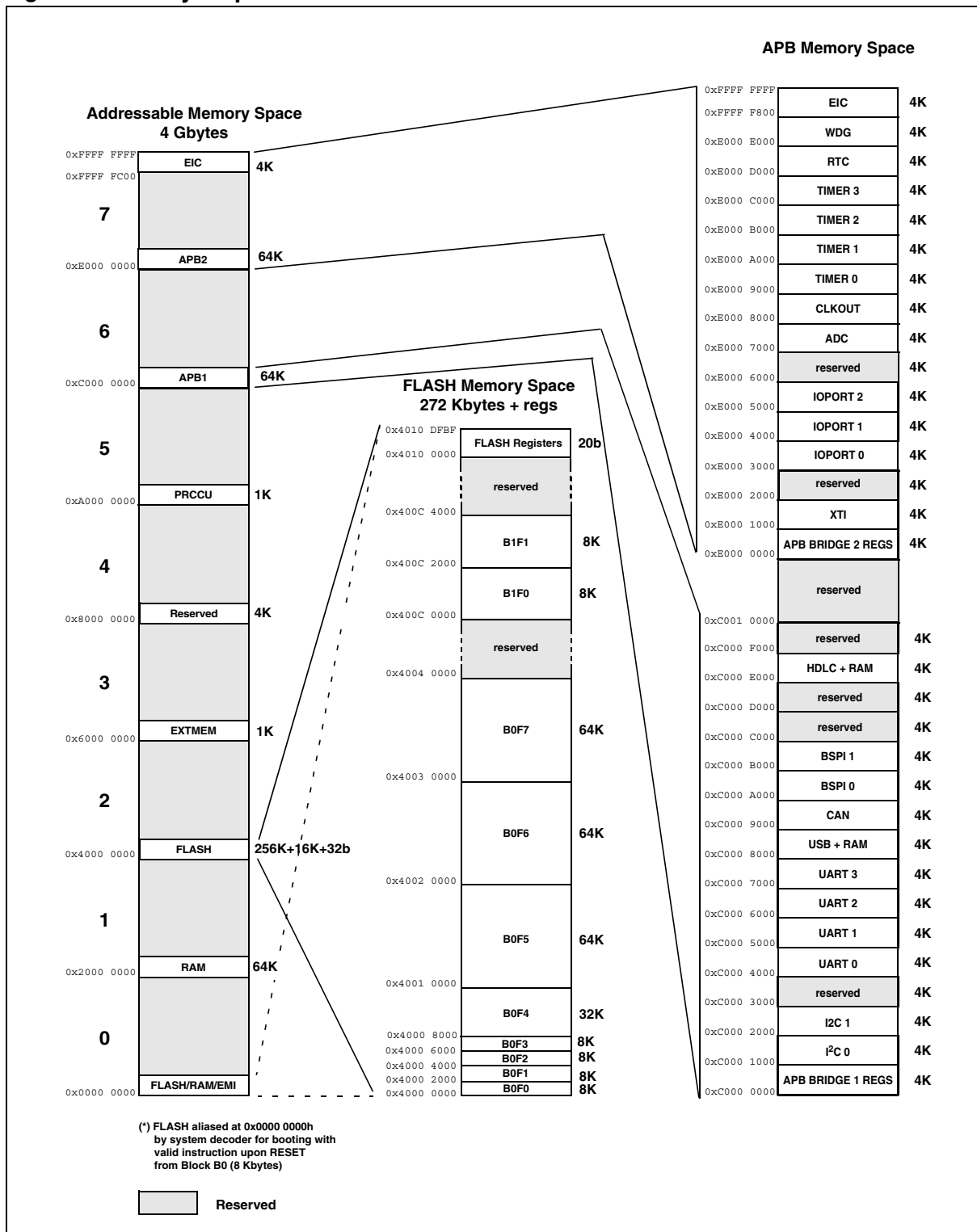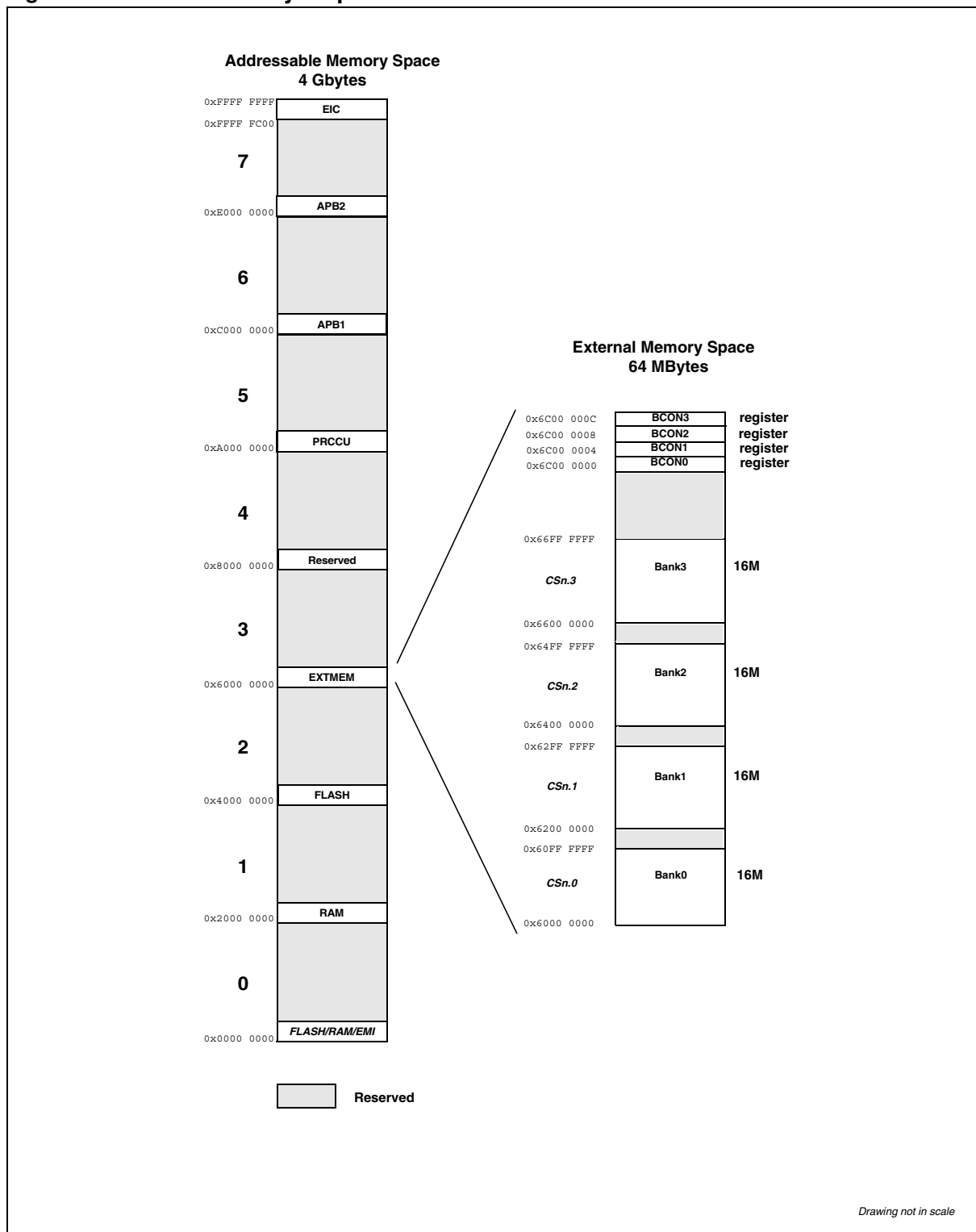
1.4 Memory Mapping

Figure 6. Memory Map

APB Memory Space

0xFFFF FFFF	EIC	4K
0xFFFF F800		
0xE000 E000	WDG	4K
0xE000 D000	RTC	4K
0xE000 C000	TIMER 3	4K
0xE000 B000	TIMER 2	4K
0xE000 A000	TIMER 1	4K
0xE000 9000	TIMER 0	4K
0xE000 8000	CLKOUT	4K
0xE000 7000	ADC	4K
0xE000 6000	reserved	4K
0xE000 5000	IOPORT 2	4K
0xE000 4000	IOPORT 1	4K
0xE000 3000	IOPORT 0	4K
0xE000 2000	reserved	4K
0xE000 1000	XTI	4K
0xE000 0000	APB BRIDGE 2 REGS	4K

**Addressable Memory Space
4 Gbytes**

0xFFFF FFFF	EIC	4K
0xFFFF FC00		
	7	
0xE000 0000	APB2	64K
	6	
0xC000 0000	APB1	64K
	5	
0xA000 0000	PRCCU	1K
	4	
0x8000 0000	Reserved	4K
	3	
0x6000 0000	EXTMEM	1K
	2	
0x4000 0000	FLASH	256K+16K+32b
	1	
0x2000 0000	RAM	64K
	0	
0x0000 0000	FLASH/RAM/EMI	

**FLASH Memory Space
272 Kbytes + regs**

0x4010 DFBF	FLASH Registers	20b
0x4010 0000	reserved	
0x400C 4000		
0x400C 2000	B1F1	8K
0x400C 0000	B1F0	8K
0x4004 0000	reserved	
0x4003 0000	B0F7	64K
0x4002 0000	B0F6	64K
0x4001 0000	B0F5	64K
0x4000 8000	B0F4	32K
0x4000 6000	B0F3	8K
0x4000 4000	B0F2	8K
0x4000 2000	B0F1	8K
0x4000 0000	B0F0	8K

0xC001 0000	reserved	
0xC000 F000	reserved	4K
0xC000 E000	HDLC + RAM	4K
0xC000 D000	reserved	4K
0xC000 C000	reserved	4K
0xC000 B000	BSPI 1	4K
0xC000 A000	BSPI 0	4K
0xC000 9000	CAN	4K
0xC000 8000	USB + RAM	4K
0xC000 7000	UART 3	4K
0xC000 6000	UART 2	4K
0xC000 5000	UART 1	4K
0xC000 4000	UART 0	4K
0xC000 3000	reserved	4K
0xC000 2000	I2C 1	4K
0xC000 1000	I²C 0	4K
0xC000 0000	APB BRIDGE 1 REGS	4K

(*) FLASH aliased at 0x0000 0000h
by system decoder for booting with
valid instruction upon RESET
from Block B0 (8 Kbytes)

Reserved

Figure 7. External Memory Map

2 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages.

For proper operation, it is recommended that V_{IN} and V_O be higher than V_{SS} and lower than V_{33}. Reliability is enhanced if unused inputs are connected to an appropriate logic voltage level (V_{33} or V_{SS}).

Table 4. Absolute Maximum Ratings.

Symbol	Parameter	Value		Unit
		Min	Max	
V_{33}	Voltage on V_{33} with respect to ground (V_{SS})	-0.3	+4.0	V
$V_{33IO-PLL}$	Voltage on $V_{33IO-PLL}$ with respect to ground (V_{SS})	-0.3	+4.0	V
V_{18}	Voltage on V_{18} with respect to ground (V_{SS})	-0.3	+2.0	V
V_{18BKP}	Voltage on V_{18BKP} with respect to ground (V_{SS})	-0.3	+2.0	V
AV_{DD}	Voltage on AV_{DD} pin with respect to ground (V_{SS})	-0.3	+4.0	V
AV_{SS}	Voltage on AV_{SS} with respect to ground (V_{SS})	-0.1	V_{33} + 0.1	V
V_{IN}	Voltage on true open drain pin (P0.10) with respect to ground (V_{SS})	-0.3	+5.5	V
	Voltage on any other pin with respect to ground (V_{SS})	-0.3	+4.0	
I_{OV}	Input current on any pin during overload condition	-10	+10	mA
I_{TDV}	Absolute sum of all input currents during overload condition		|200|	mA
T_{ST}	Storage Temperature	–55	+150	°C
ESD	ESD Susceptibility (Human Body Model)	2000		V

Note   Stresses exceeding above listed recommended "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{33}$ or $V_{IN} < V_{SS}$) the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

2.2 Operating Conditions

Symbol	Parameter	Value		Unit
		Min	**Max**	
V_{33}	Digital Supply Voltage for I/O circuitry	3.0	3.6	V
$V_{33IO\text{-}PLL}$	Digital Supply Voltage for I/O circuitry and for PLL reference	3.0	3.6	V
V_{18BKP}	External Supply Voltage for Backup block (Voltage Regulator off)	1.4	1.8	V
AV_{DD}	Analog Supply Voltage for the A/D converter	V_{33}	V_{33}	V
T_A	Ambient temperature under bias	−40	+85	°C
T_J	Junction temperature under bias	−40	+105	°C

Note   *RAM data retention is guaranteed with V_{33} not below 2.7 Volt, with the device in low power mode (Stop or Wait for Interrupt).*

2.3 LVD Electrical Characteristics

V_{33} = 3.3 ± 10%, T_A = -40 / 85 °C unless otherwise specified.

Table 5. LVD Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	**Typ**	**Max**	
V_{IT}	LVD Threshold	Main and LP LVDs		1.3	1.45	V

2.4 DC Electrical Characteristics

V_{33} = 3.3V $\pm$ 10%, T_A = -40 / 85 °C unless otherwise specified.

Table 6. DC Electrical Characteristics

Symbol	Parameter	Comment	Value			Unit
			Min	Typ	Max	
V_{IH}	Input High Level CMOS	With or w/o hysteresis	$0.7V_{33}$			V
	Input High Level	P0.15 (WAKEUP) only	1.8			V
V_{IL}	Input Low Level CMOS	With or w/o hysteresis			$0.3V_{33}$	V
	Input Low Level	P0.15 (WAKEUP) only			0.7	V
V_{HYS}	Input Hysteresis CMOS Schmitt Trigger		0.4	0.8	1.2	V
	Input Hysteresis Schmitt Trigger	P0.15 (WAKEUP) only	0.3	0.5		V
V_{OH}	Output High Level High Current Pins	Push Pull, I_{OH}= 8mA	$V_{33} - 0.8$			V
	Output High Level Standard Current Pins	Push Pull, I_{OH}= 4mA	$V_{33} - 0.8$			V
V_{OL}	Output Low Level High Current Pins	Push Pull, I_{OL}= 8mA			0.4	V
	Output Low Level Standard Current Pins	Push Pull, I_{OL}= 4mA			0.4	V
R_{WPU}	Weak Pull-Up Resistor	Measured at $0.5V_{33}$		100		kΩ
R_{WPD}	Weak Pull-Down Resistor	Measured at $0.5V_{33}$		100		kΩ

2.5 AC Electrical Characteristics

$V_{33} = 3.3V \pm 10\%$, $T_A = 27$ °C unless otherwise specified.

Table 7. Power Consumption

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{DDRUN}	RUN Mode current	MCLK=50 MHz		See Table 8	100	mA
I_{DDWFI}	WFI Mode current	1 MHz System Clock		3	6	mA
I_{DDLP}	LPWFI Mode current	32 kHz System Clock		200		μA
I_{DDSTP}	STOP Mode current	Main VReg off, Flash in Power-Down		100		μA
I_{DDSB1}	STANDBY Mode current	LP VReg and 32kHz Osc on		15	30	μA
I_{DDSB0}	STANDBY Mode current	LP VReg, LVD, 32kHz Osc bypassed		3	10	μA

Note   *I_{DDRUN} is the power consumption in applications exploiting the full performances of the core (running at the maximum frequency).*

Note   *I_{DDWFI} is the power consumption with PLLs off, VReg and Flash on. This guarantees the minimum interrupt response time.*

Note   *I_{DDLP} is the power consumption with PLLs, Main VReg and Flash off.*

Table 8. I_{DDRUN} Typical Data measurements, T_A=25°C

Frequency	All Peripheral clocks enabled[1] (Reset Configuration)		All Peripheral clocks disabled[1]		Unit
	RAM Execution	Flash Execution	RAM Execution	Flash Execution	
MCLK=1 MHz PCLK=1 MHz	15	15	11	11	mA
MCLK=8 MHz PCLK=8 MHz	19	20	15	17	
MCLK=16 MHz PCLK=8 MHz	23	27	19	23	
MCLK=48 MHz PCLK=6 MHz	43	53	40	50	
MCLK=64 MHz PCLK=8 MHz	53	N/A	48	N/A	

[1]Refer to APBn_CKDIS register description.

V_{33} = 3.3V $\pm$ 10%, T_A = -40 / 85 °C unless otherwise specified.

Table 9. AC Electrical Characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{MCLK}	CPU Frequency	Executing from RAM or external memory			66	MHz
		Executing from Flash			50	
		Executing from Flash with RWW			45	
		Burst Mode disabled (FLASHLP bit =1)			33	
f_{PCLK}	Peripheral Clock for APB				33	
f_{CK}	Clock input pin				16	

2.6 nRSTIN Input Filter Characteristics

V_{33} = 3.3V $\pm$ 10%, T_A = -40 / 85 °C unless otherwise specified.

Table 10. nRSTIN input Filter Characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
t_{FR}	nRSTIN Input Filtered Pulse				500	ns
t_{NFR}	nRSTIN Input Not Filtered Pulse		1.2			μs

2.7 Oscillator Electrical Characteristics

V_{33} = 3.3 $\pm$ 10%, T_A = -40 / 85 °C unless otherwise specified.

Figure 8. Crystal Oscillator and Resonator
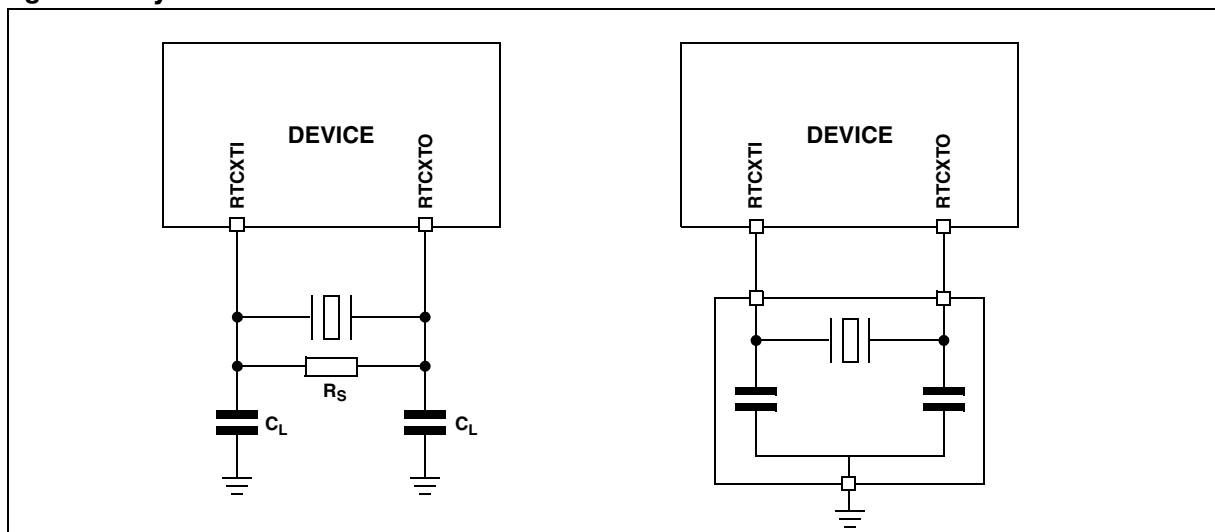
Table 11. Oscillator Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
g_m	Oscillator Transconductance			8		μA/V
t_{STUP}	Oscillator Start-up Time	Stable V_{33}			2.5	s

2.8 PLL Electrical Characteristics

V_{33} = 3.3 $\pm$ 10%, $V_{33IOPLL}$ = 3.3 $\pm$ 10%, T_A = -40 / 85 °C unless otherwise specified.

Table 12. PLL1 Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK1}$	PLL output clock	f_{PLL1}x 24			165	MHz
f_{PLL1}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1 MX[1:0]='00' or '01'	3.0		8.25	MHz
		FREF_RANGE = 1 MX[1:0]='10' or '11'	3.0		6	MHz

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
f_{FREE1}	PLL free running frequency	FREF_RANGE = 0 MX[1:0]='01' or '11'		1		MHz
		FREF_RANGE = 0 MX[1:0]='00' or '10'		2		MHz
		FREF_RANGE = 1 MX[1:0]='01' or '11'		2		MHz
		FREF_RANGE = 1 MX[1:0]='00' or '10'		4		MHz
t_{LOCK1}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	μs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	μs
$\Delta t_{JITTER1}$	PLL jitter (peak to peak)	t_{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz)		0.7	2	ns

Table 13. **PLL2 Electrical Characteristics**

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK2}$	PLL output clock	f_{PLL} x 28			140	MHz
f_{PLL2}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1	3.0		5	MHz
t_{LOCK2}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	μs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	μs
$\Delta t_{JITTER2}$	PLL jitter (peak to peak)	t_{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz)		0.7	2	ns

2.9 Flash Electrical characteristics

$V_{33} = 3.3 \pm 10\%$, T_A = -40 / 85 °C unless otherwise specified.

Table 14. Flash Program/Erase Characteristics 1

Symbol	Parameter	Test Conditions	Value			Unit
			Typ	Max(C_0)	Max(C_{max})	
t_{PW}	Word Program		40			μs
t_{PDW}	Double Word Program		60			μs
t_{PB0}	Bank 0 Program (256K)	Double Word Program	1.6	2.1	4.3	s
t_{PB1}	Bank 1 Program (16K)	Double Word Program	130	170	300	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed Preprogrammed	2.3 1.9	4.0 3.3	4.9 4.1	s
t_{ES}	Sector Erase (8K)	Not preprogrammed Preprogrammed	0.7 0.6	1.1 1.0	1.36 1.26	s
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed Preprogrammed	8.0 6.6	13.7 11.2	17.2 14.0	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed Preprogrammed	0.9 0.8	1.5 1.3	1.87 1.66	s
t_{RPD}	Recovery from Power-Down				20	μs
t_{PSL}	Program Suspend Latency				10	μs
t_{ESL}	Erase Suspend Latency				300	μs

Note C_0: T_A = 85 °C *after 0 cycles*

         C_{max}: T_A = 85 °C *after max number of cycles*

Table 15. Flash Program/Erase Characteristics 2

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
	Endurance		10			kcycles
	Endurance (Bank1 sectors)		100			kcycles
	Data Retention		20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

2.10 External Memory Bus Timing

$V_{33} = 3.3 \pm 10\%$, T_A = -40 / 85 °C unless otherwise specified.

The tables below use a variable which is derived from the EMI_BCONn registers (described in the STR71x Reference Manual) and represents the special characteristics of the programmed memory cycle.

Symbol	Parameter	Value
t_{MCLK}	CPU clock period	$1 / f_{MCLK}$
t_C	Memory cycle time wait states	$t_{MCLK} \times (1 + [C\_LENGTH])$

Table 16. EMI Read Operation

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
t_{RCR}	Read to CSn Removal Time			t_{MCLK}		ns
t_{RP}	Read Pulse Time			t_C		ns
t_{RDS}	Read Data Setup Time			3		ns
t_{RDH}	Read Data Hold Time			3		ns
t_{RAS}	Read Address Setup Time			$1.3{*}t_{MCLK}$		ns
t_{RAH}	Read Address Hold Time			3		ns
t_{RAT}	Read Address Turnaround Time			3		ns
t_{RRT}	RDn Turnaround Time			t_{MCLK}		ns

See Figure 9, Figure 10, Figure 11and Figure 12 for related timing diagams.

Table 17. EMI Write Operation

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
t_{WCR}	WEn to CSn Removal Time			t_{MCLK}		ns
t_{WP}	Write Pulse Time			t_C		ns
t_{WDS}	Write Data Setup Time			3		ns
t_{WDH}	Write Data Hold Time			3		ns
t_{WAS}	Write Address Setup Time			$1.3{*}t_{MCLK}$		ns
t_{WAH}	Write Address Hold Time			3		ns
t_{WAT}	Write Address Turnaround Time			3		ns
t_{WWT}	WEn Turnaround Time			t_{MCLK}		ns

See Figure 13, Figure 14, Figure 15 and Figure 16 for related timing diagrams.

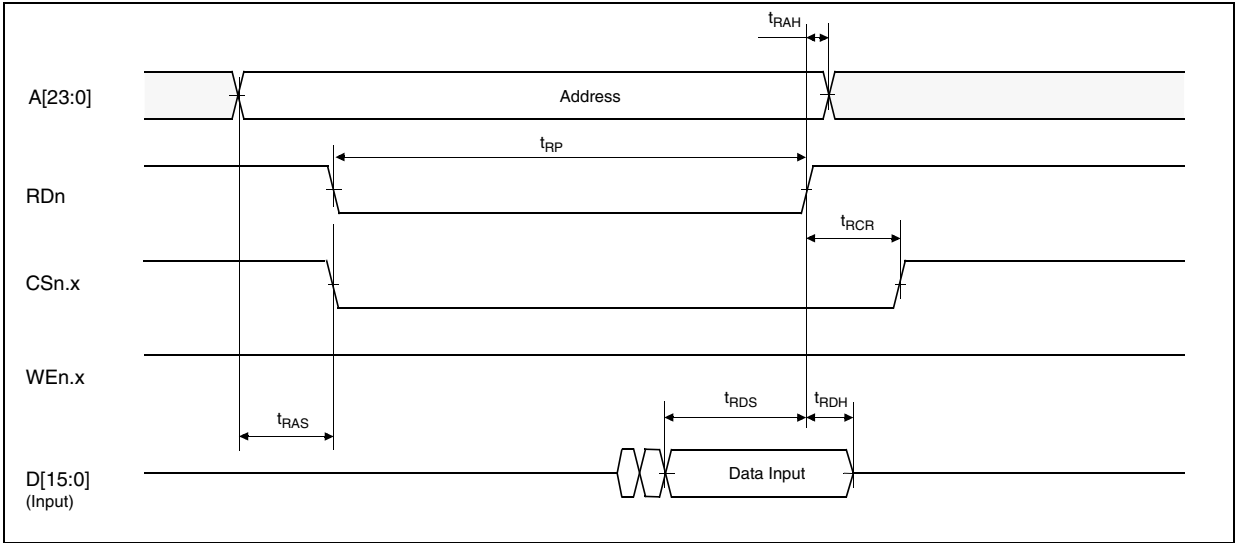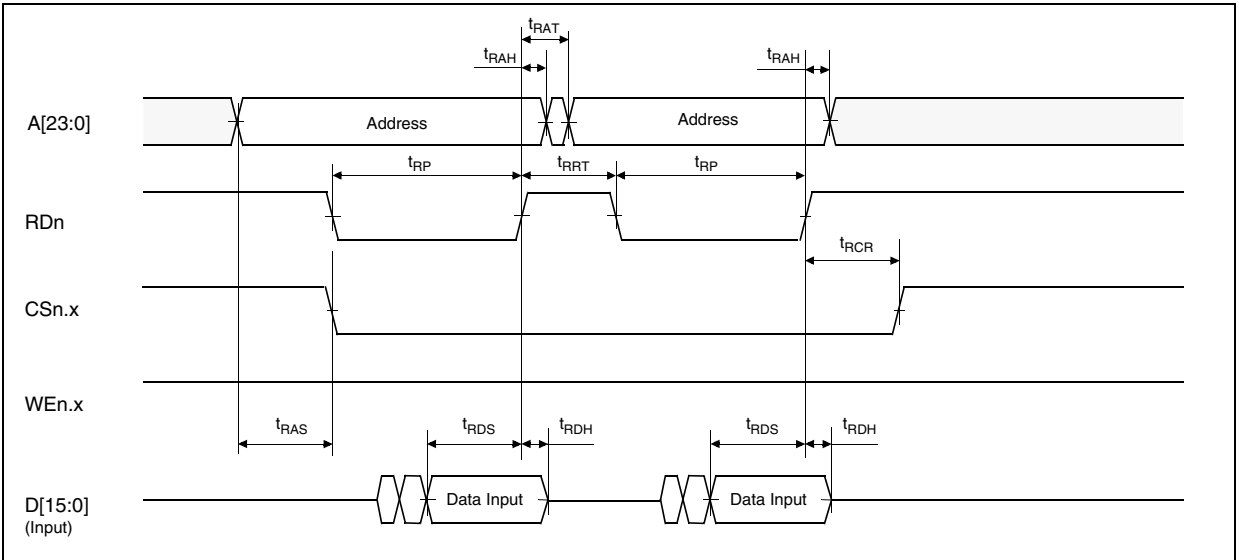**Figure 9. Read Cycle Timing: 16-bit READ on 16-bit Memory**

Figure 10. Read Cycle Timing: 32-bit READ on 16-bit Memory

See Table 16 for read timing data.

Figure 11. **Read Cycle Timing: 16-bit READ on 8-bit Memory**
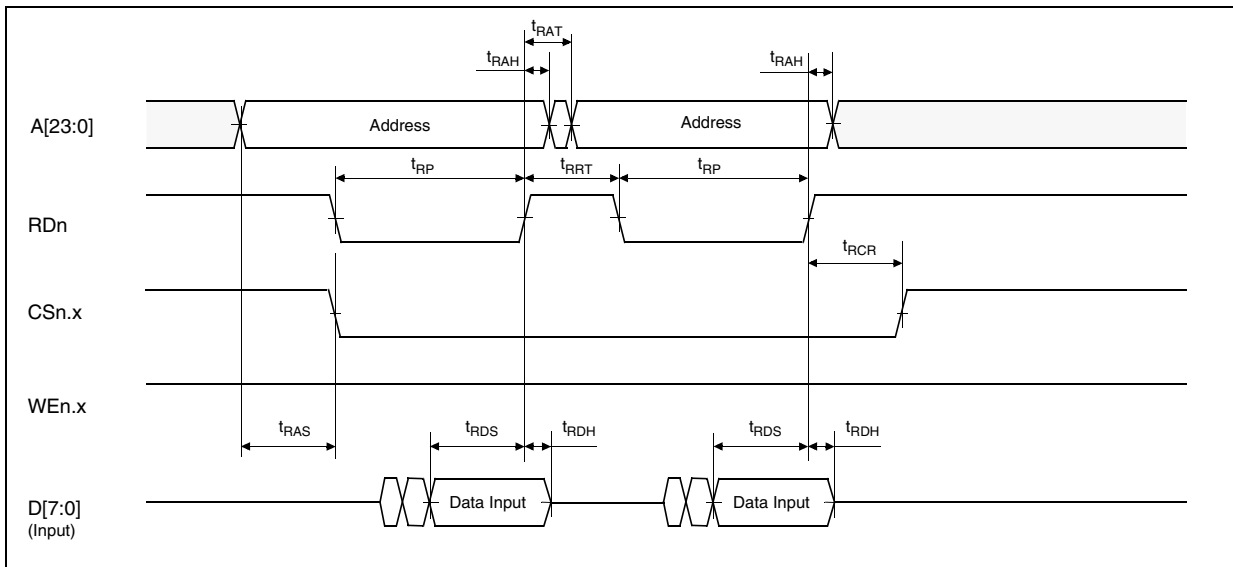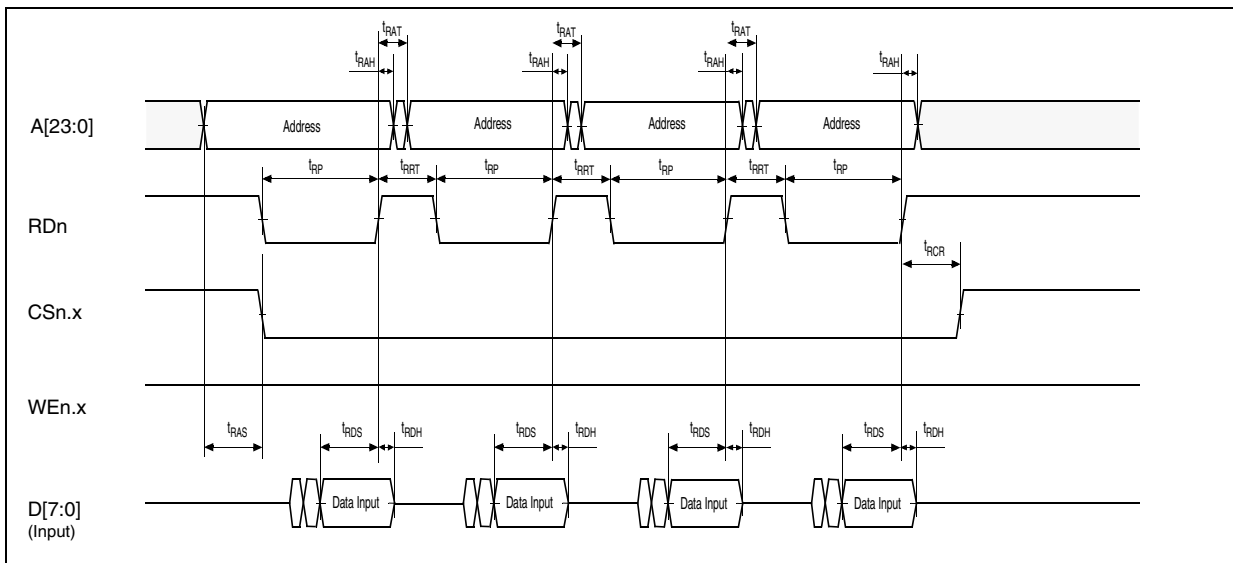

Figure 12. **Read Cycle Timing: 32-bit READ on 8-bit Memory**

See Table 16 for read timing data.

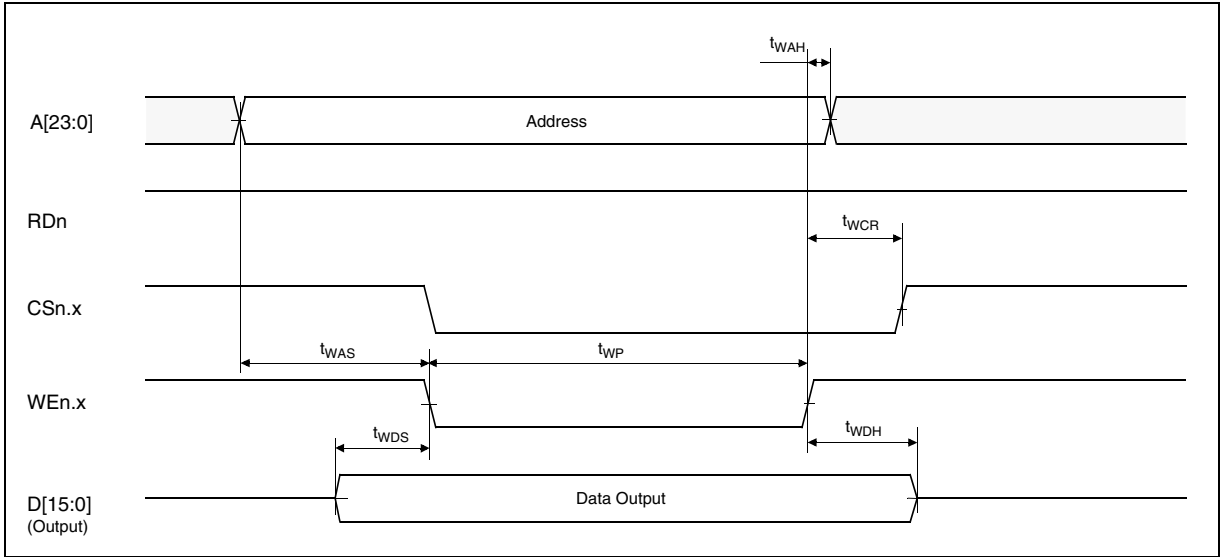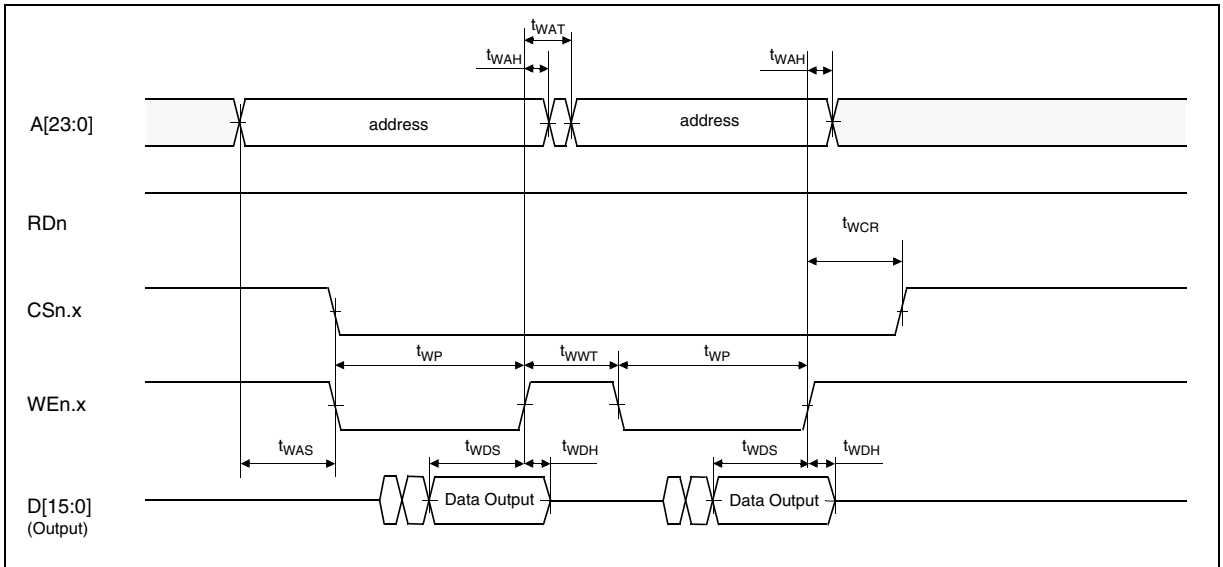**Figure 13. Write Cycle Timing: 16-bit WRITE on 16-bit Memory**

Figure 14. Write Cycle Timing: 32-bit WRITE on 16-bit Memory

See Table 17 for write timing data.

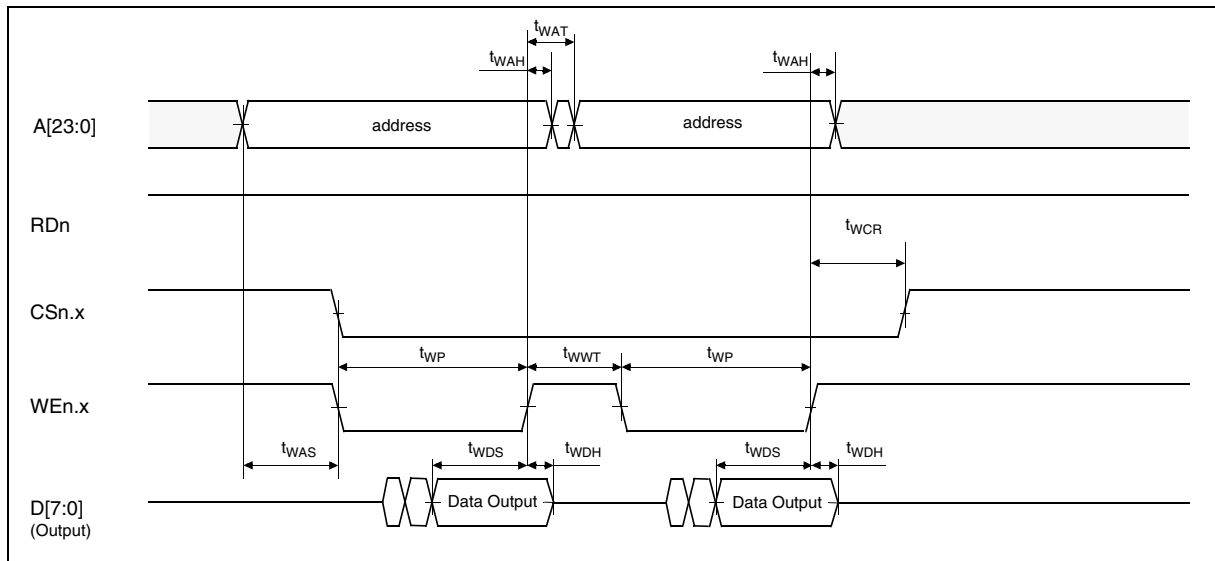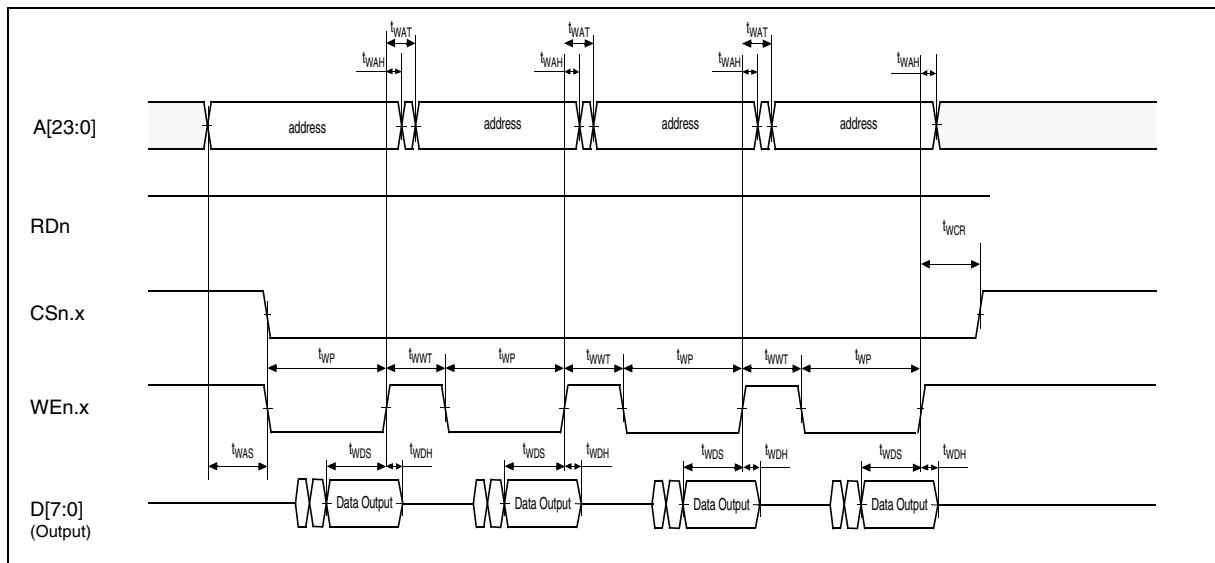**Figure 15. Write Cycle Timing: 16-bit WRITE on 8-bit Memory**

Figure 16. Write Cycle Timing: 32-bit WRITE on 8-bit Memory

See Table 17 for write timing data.

2.11 ADC Electrical Characteristics

$V_{33} = 3.3 \pm 10\%$, $AV_{DD} = 3.3 \pm 10\%$, $T_A = -40 / 85\ °C$ unless otherwise specified.

Table 18. ADC Electrical Characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max	
RES	Resolution	Sinewave with ΔV_{IN} amplitude		12		bits
ΔV_{IN}	Input Voltage Range		0		2.5	V
f_{MOD}	Modulator Oversampling Frequency				2.1	MHz
IBW	Input Bandwidth				$f_{MOD}/4096$	kHz
N_{ch}	Number of Input Channels				4	n
PBR	Passband Ripple				0.1	dB
SINAD	S/N and Distortion		56	63		dB
THD	Total Harmonic Distortion		60	74		dB
Z_{IN}	Input Impedance	$f_{MOD} = 2$ MHz	1			$M\Omega$
C_{IN}	Input Capacitance				5	pF
I_{ADC}	Power Consumption	$T_A = 27\ °C$		2.5	3.0	mA
I_{STBY}	Standby Power Consumption	$T_A = 27\ °C$			1	μA

3 PACKAGE CHARACTERISTICS

3.1 Package Mechanical Data

Figure 17. 64-Pin Thin Quad Flat Package (10x10)

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
E		12.00			0.472	
E1		10.00			0.394	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
Number of Pins						
N	64					
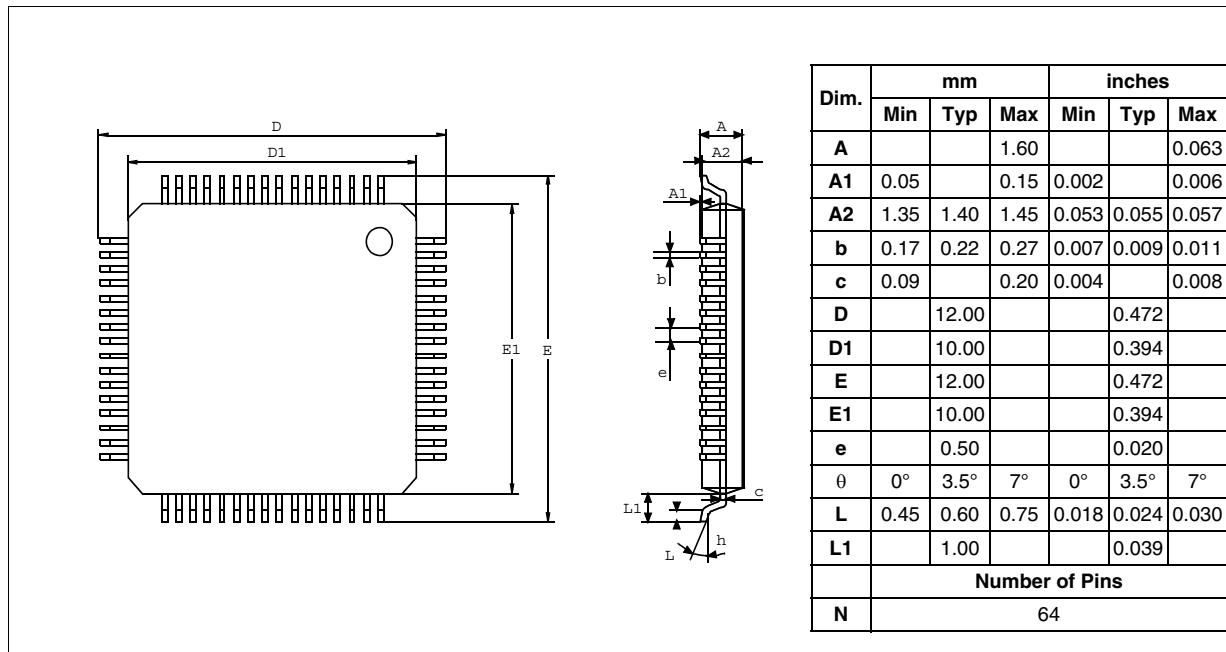
Figure 18. 144-Pin Thin Quad Flat Package

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053		0.057
b	0.17	0.22	0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
D	21.80	22.00	22.20	0.858	0.867	0.874
D1	19.80	20.00	20.20	0.780	0.787	0.795
D3		17.50			0.699	
E	21.80	22.00	22.20	0.858	0.867	0.874
E1	19.80	20.00	20.20	0.780	0.787	0.795
E3		17.50			0.699	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
Number of Pins						
N	144					
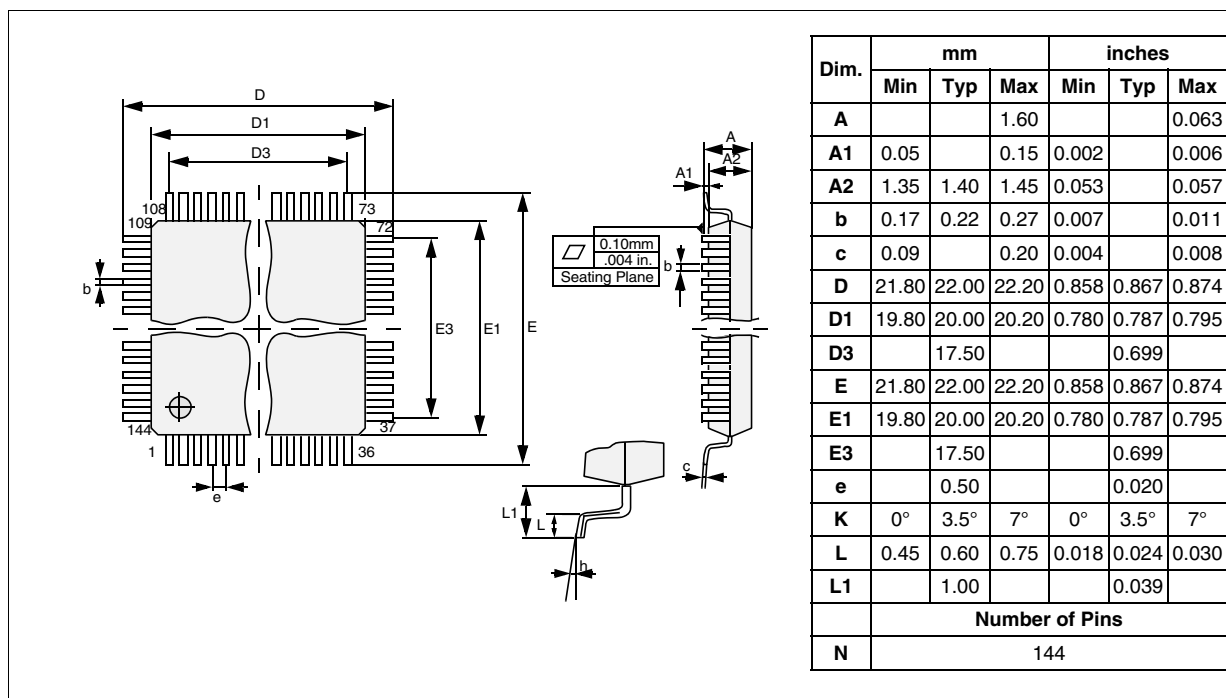
3.2 Thermal Characteristics

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \tag{1}$$

Where:

- T_A is the Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power.
- $P_{I/O}$ represents the Power Dissipation on Input and Output Pins;

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) \tag{2}$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D{}^2 \tag{3}$$

where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 19. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal Resistance Junction-Ambient** TQFP 144 - 20 x 20 mm / 0.5 mm pitch	42	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** TQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W

4 ORDER CODES

Table 20. Order Codes

Partnumber	FLASH Kbytes	RAM Kbytes	EMI	USB	CAN	I/O Ports	Package	Temp. Range
STR710FZ1T6	128+16	16	Yes	Yes	Yes	48	TQFP144 20x20	-40 to +85°C
STR710FZ2T6	256+16	64	Yes	Yes	Yes	48		
STR711FR1T6	128+16	16	No	Yes	No	30	TQFP64 10x10	
STR711FR2T6	256+16	64		Yes	No	30		
STR712FR1T6	128+16	16		No	Yes	32		
STR712FR2T6	256+16	64		No	Yes	32		

5 REVISION HISTORY

Table 21. Revision history

Date	Revision	Description of Changes
17-Mar-2004	1	First Release
05-Apr-2004	2	Updated "ELECTRICAL CHARACTERISTICS" on page 21
08-Apr-2004	2.1	Corrected STR712F Pinout. Pins 43/42 swapped.
15-Apr-2004	2.2	PDF hyperlinks corrected.
7-Jul-2004	3	Corrected description of STDBY, V18, VSS18 V18BKP VSSBKP pins Added IDDrun typical data Updated BSPI max. baudrate. Updated "External Memory Bus Timing" on page 29
29-Oct-2004	4	Corrected Flash sector B1F0/F1 address in <zap>Figure 6 on page 19 Corrected Table 2, "Device Pin Description," on page 11 TQFP64 TEST pin is 16 instead of 17. Added to TQPFP64 column: pin 7 BOOTEN, pin 17 $V_{33IO-PLL}$ Changed description of JTCK from 'External pull-down required' to 'External pull-up or pull down required'.

Notes:

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