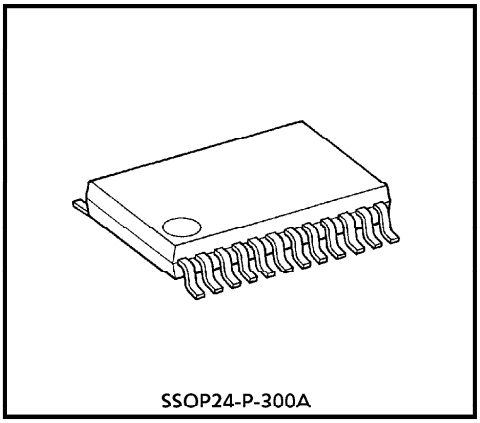
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9418FN

PLL FOR DIGITAL TUNING SYSTEM (DTS)

The TC9418FN is a PLL LSI for digital tuning system (DTS) incorporating a 2-modulus prescaler.
Each function is controlled through four serial bus lines, allowing you to configure a high-performance digital tuning system.



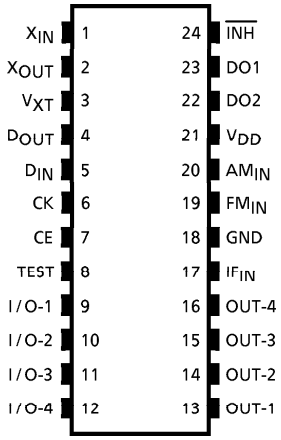
SSOP24-P-300A

Weight : 0.31g (Typ.)

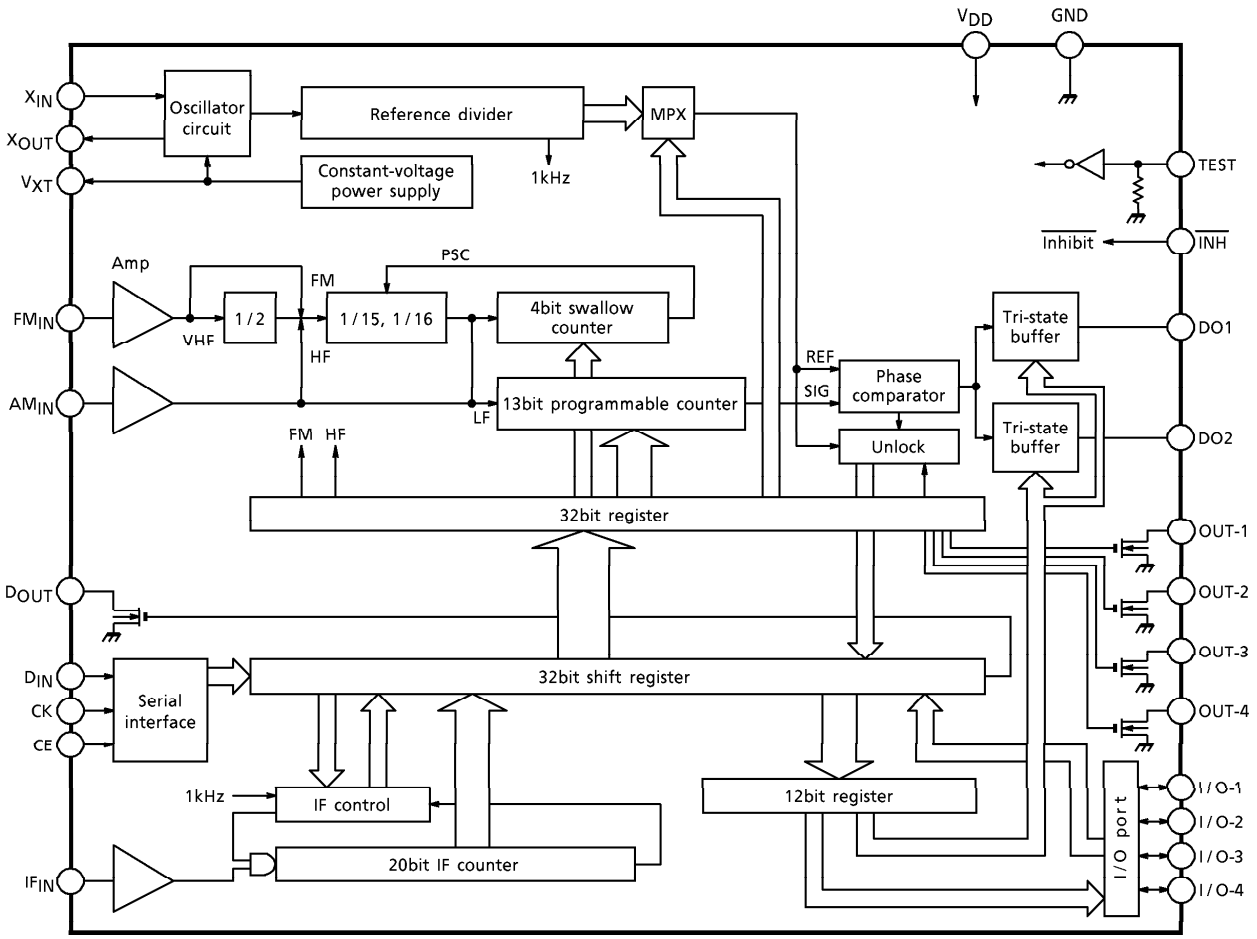
FEATURES

- Ideal for configuring a digital tuning system in headphone stereos and portable radios.
- Incorporating a prescaler, the device can operate at VHF : 50~230MHz (1/2 + pulse swallow mode) and FM : 50~130MHz (pulse swallow mode) during FM_{IN} input, and at HF : 1~20MHz (pulse swallow mode) and LF : 0.5~10MHz (direct divide mode) during AM_{IN} input.
- Comes with a 17bit programmable counter, two parallel output phase comparators, a 75kHz crystal oscillator, a reference counter, and a 20bit IF counter.
- Consisting of a 75kHz crystal resonator (X'tal), the oscillator circuit is powered by a constant-voltage power supply to generate consistently stable oscillation.
- The reference frequency can be selected from seven frequencies available (fref = 1kHz, 3k, 3.125k, 5k, 6.25k, 12.25k, 25k).
- Inhibit input ($\overline{INH}$) places the device in low-power backup mode ($I_{HD} \leqq 10\mu A$).
- Comes with four lines of I/O ports and four lines of N-channel open-drain outputs (OFF withstand voltage : 5.5V).
- Operates over a voltage range of V_{DD} = 1.8~3.6V (Ta = – 10~60°C).
- The package is a 24pin SSOP (0.65 pitch).

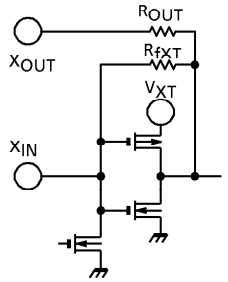
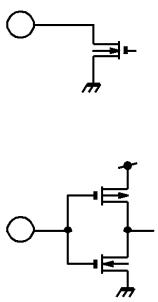
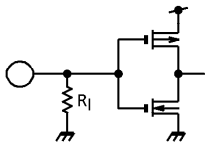
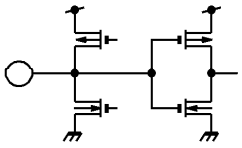
PIN CONNECTION

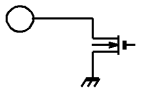
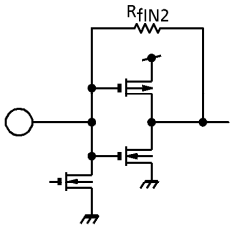
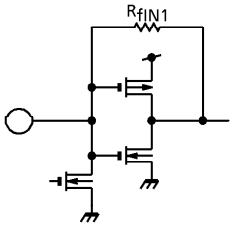


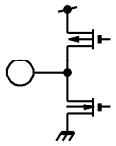
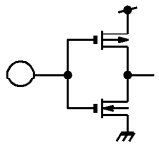
BLOCK DIAGRAM



PIN DESCRIPTION

PIN No.	SYMBOL	PIN NAME	DESCRIPTION	EQUIVALENT CIRCUIT
1	X_{IN}	Crystal Resonator	These pins are used for a crystal resonator. connect a 75kHz reference crystal resonator to the X_{IN} and X_{OUT} pins. Oscillation stops and remains idle when the $\overline{INH}$ input is low. Use the X_{XT} pin for a crystal oscillator power supply. Insert a stabilizing capacitor (0.47μF Typ.) between this pin and GND.	
2	X_{OUT}			
3	V_{XT}			
4	D_{OUT}	Serial Data Output	These are serial interface pins. These pins are used to send and receive data to set the divide number and divide mode and control the IF counter and I/O ports to and from a controller. To allow the device to be easily interfaced to a controller operating with a different supply voltage, the D_{IN}, Ck, and CE input pins have their input threshold levels set to 0.3 through 0.8V (0.5V Typ.), and the D_{OUT} pin is an N-channel open-drain output. Data outputs are placed in the high-impedance state and inputs are turned off when the $\overline{INH}$ input is held low.	
5	D_{IN}	Serial Data Input		
6	CK	Clock Input		
7	CE	Chip Enable Input		
8	TEST	Test Mode Control Input	This input contains a pull-down resistor, and can normally be used with GND or NC.	
9 ~ 12	I/O-1 ~ I/O-4	I/O Port	These are 4bit I/O ports. These ports can be set for input or output in units of one bit. At power-on, their input/output state and output state are indeterminate. The bits set for output are pulled low when the $\overline{INH}$ input is low.	

PIN No.	SYMBOL	PIN NAME	DESCRIPTION	EQUIVALENT CIRCUIT
13 ~ 16	OUT-1 ~ OUT-4	N-Channel Open-Drain Output	These are 4bit I/O ports. Because these ports are built with an N-channel open-drain structure, they can be used for control signals operating with different supply voltages. At power-on, their output state is indeterminate. The N-channel transistors are turned off when the $\overline{INH}$ input is low.	
17	IF_{IN}	IF Signal Input	This is an IF signal input for the IF counter. Its input frequency is 0.35 to 12MHz ($0.2V_{p-p}$ min.). Incorporating an input amp, it operates with a C-coupled small amplitude. This input is pulled down when the $\overline{INH}$ input is held low.	
18	GND	Power Supply Input	These are power supply input pins. Normally input a voltage V_{DD} = 1.8~3.6V (3.0 Typ.) to these pins. When the $\overline{INH}$ input is pulled low, the device is placed in a low current consumption mode (10μA or less).	—
21	V_{DD}			
19	FM_{IN}	FM/VHF Band Local Oscillator Signal Input	This is a VCO (voltage-controlled oscillator) input during FM and VHF bands. It operates at 50~130MHz during FM (pulse swallow mode) and 50~230MHz during VHF (1/2 + pulse swallow mode). Incorporating and input amp, it operates with a C-coupled small amplitude ($0.2V_{p-p}$ min.). This input is pulled down when the $\overline{INH}$ input is held low.	
20	AM_{IN}	AM Band Local Oscillator Signal Input	This is a VCO input during AM band. It operates at 0.5~10MHz during LF (direct divide mode) and 1~20MHz during HF (pulse swallow mode). Incorporating an input amp, it operates with a C-coupled small amplitude ($0.2V_{p-p}$ min.). This input is pulled down when the $\overline{INH}$ input is held low.	

PIN No.	SYM-BOL	PIN NAME	DESCRIPTION	EQUIVALENT CIRCUIT
22 23	DO2 DO1	Phase Comparator Output	These are the PLL's phase comparator outputs. DO1 and DO2 are output in parallel. Therefore, filter constants can be set to an optimum value in each FM and AM band. Furthermore, since these pins each can be driven high and low and placed in the high-impedance state, lock-up time improvements can be easily accomplished. These outputs are placed in the high-impedance state when the $\overline{INH}$ input is held low.	
24	$\overline{INH}$	Inhibit Input	This is an inhibit input. When this input is driven high, all functions of the device are enabled. When this input is driven low, all functions are disabled, with the device placed in low-power backup mode (10μA or less). At this time, the data transferred to the device through the serial interface is retained, so that when the power is turned back on again, the device can be operated normally until data is transferred.	

DEVICE OPERATION

○ Serial I/O port

As shown in the block diagram, the TC9418FN has 32bit and 12bit registers providing a total of 44bits to set data for control of each function. Each data in these registers is transferred to and from the controller through serial ports using the D_{IN}, D_{OUT}, CK, and CE pins. The data serially transferred in one operation consists of eight address bits and 32 data bits, 40bits in total. However, the serially transferred data to set the I/O and DO pins (input mode 2) consists of eight address bits and 16 data bits, 24bits in total.

Some of the eight address bits above can be omitted, to a minimum of four bits. In this case, use these four bits to specify the address. (Clock can also be omitted.)

Thus, all functions can be controlled in units of registers. The following describes mainly the eight address bits and the functions of each register.

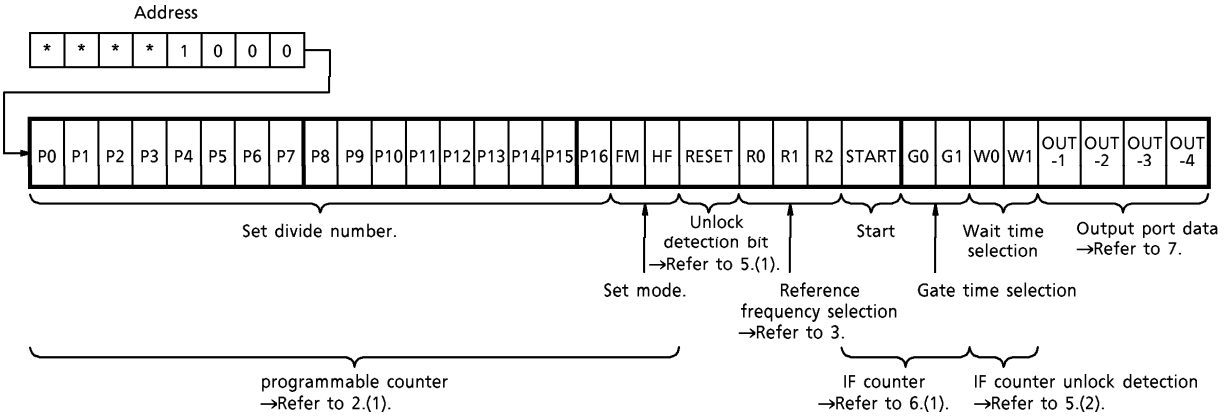
These registers are configured in units of 32bits and 12bits, each selected by an 8bit address. The next pages shows the address map of each register as "Register Assignments."

REGISTER	ADDRESS	CONFIGURATION OF 32BITS	NUMBER OF BITS
Input register	****1000	Set PLL's divide number. Set PLL's input and mode. Detect lock state. Set reference frequency. Start IF counter. Start IF counter gate time. Set wait time. Output data.	17 2 1 3 1 2 2 4 Total 32bits
Input register	****0100	I/O control data. I/O port output data. Set DO output state. Unused.	4 4 4 4 Total 16bits
Output register	****1100	IF counter data. IF counter overflow data. Monitor IF counter operation. PLL unlock enable bit. PLL unlock data. I/O port input data. Unused	20 1 1 1 1 4 4 Total 32bits

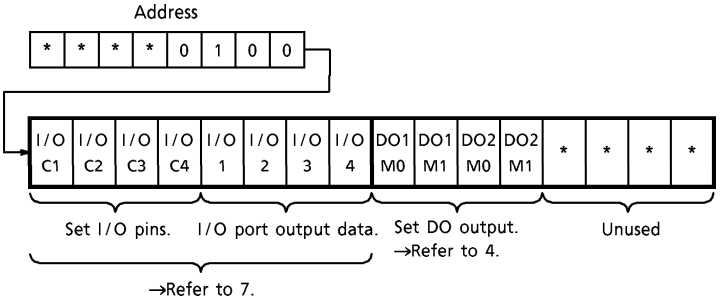
* Don't care ; it can be 0 or 1 or can be omitted.

REGISTER ASSIGNMENTS (Input)

Input mode 1

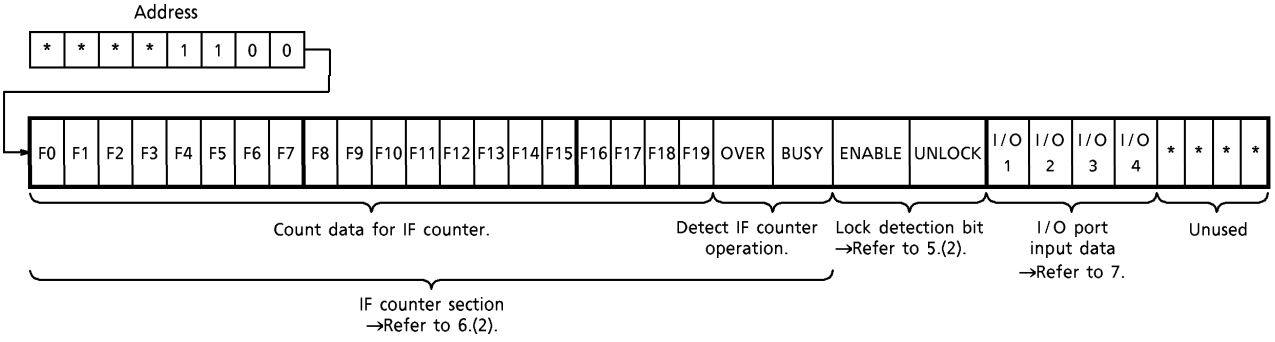


Input mode 2



(Note) Bits marked with * are Don't care ; they can be 0 or 1.

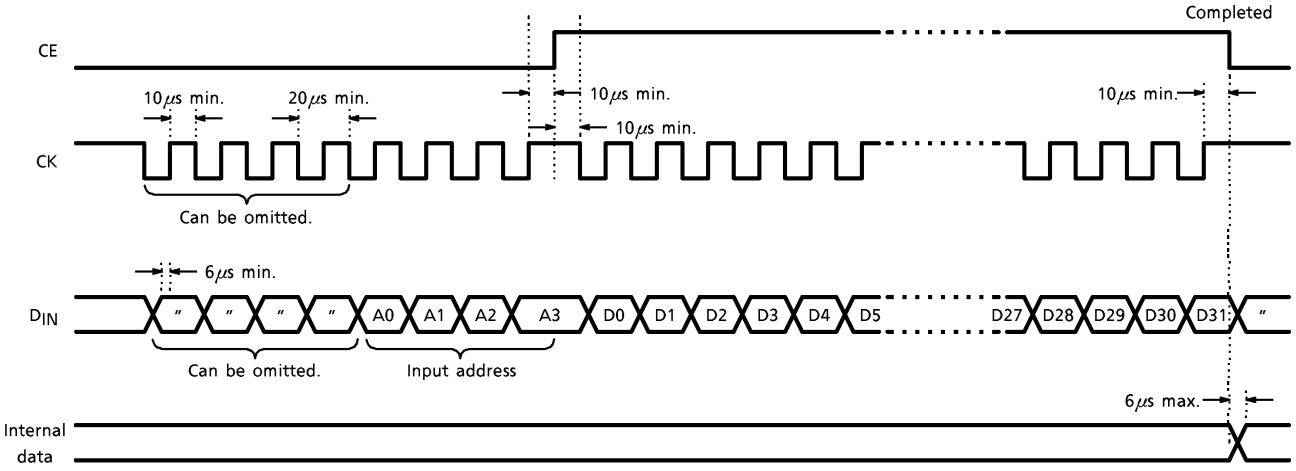
Output mode



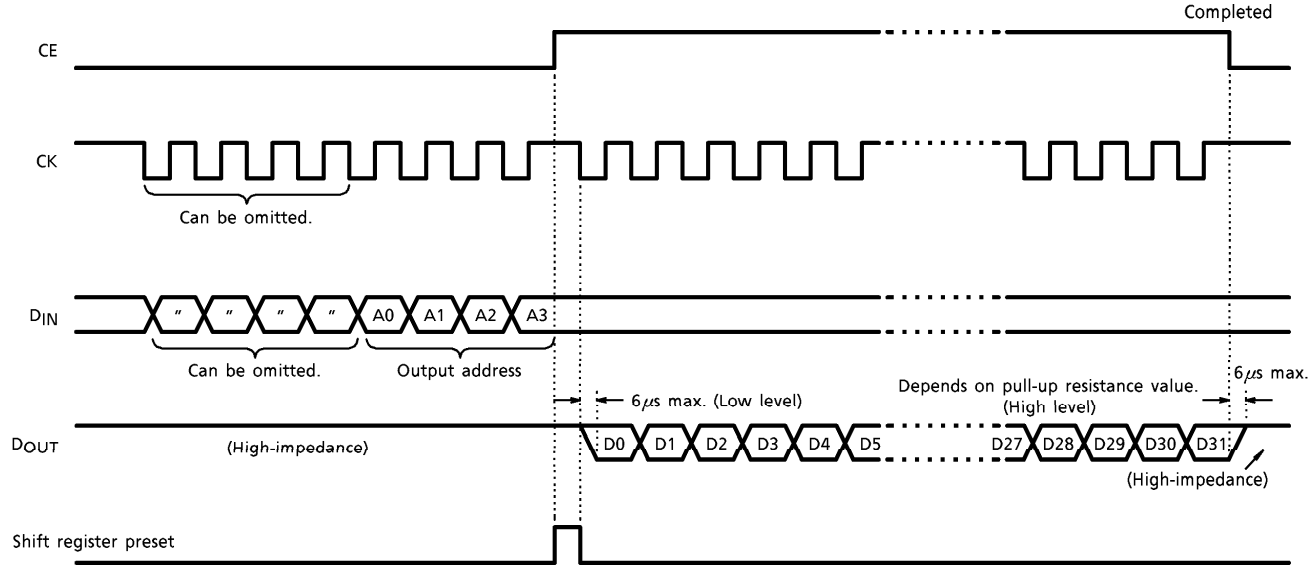
(Note) Bits marked with * are indeterminate.

○ Serial transfer format

- Data input mode (D_{OUT} is placed in high-impedance state during input.)



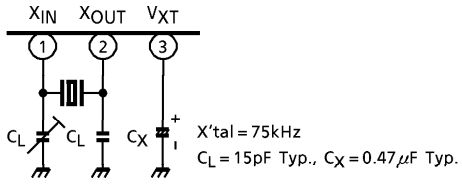
- Data output mode



(Note) D_{OUT} normally is placed in the high-impedance state.

1. Connecting crystal resonator

Connect a 75kHz crystal resonator to the device's crystal oscillator pins (X_{IN}, X_{OUT}) as shown below. This oscillation signal is fed to the clock generator and reference frequency divider to generate the reference frequency for device operation. Furthermore, this crystal oscillator circuit is operated with the voltage V_{XT} = 1.4V Typ.) supplied by an internal constant-voltage circuit. This configuration helps to stabilize crystal oscillation and reduce the current consumption.



2. Programmable counter

The programmable counter block consists of a 1/2 prescaler, 2-modulus prescaler, and 4bit + 13bit programmable binary counters.

(1) Setting up the programmable counter block

Use 17bits for the divide number and two bits for the divide mode.

① Setting the divide mode

Use the FM and HF bits to choose the input pins and the divide mode (pulse swallow or direct divide mode). There are four combinations of these bits as shown below. Choose your desired setting depending on the frequency bands used.

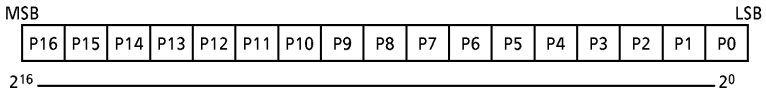
MODE	FM	HF	DIVIDE MODE	TYP. RECEIVE BAND	INPUT FREQUENCY RANGE	INPUT PIN	DIVIDE NUM-BER
LF	0	0	Direct divide mode	LW·MW	0.5~10MHz	AM_{IN}	n
HF	0	1	Pulse swallow mode	SW	1~20MHz	AM_{IN}	n
FM	1	0	Pulse swallow mode	FM	50~130MHz	FM_{IN}	n
VHF	1	1	1/2 + pulse swallow mode	VHF	50~230MHz	FM_{IN}	2·n

(Note) 'n' denotes a divide number.

② Setting divide number

Set the programmable counter's divide number in binary by using the P0 to P16 bits.

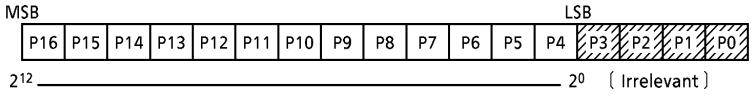
- Pulse swallow mode (17bits ; HF, FM, and VHF bands)



The range of divide numbers that can be set (pulse swallow mode) n = 210H to 1FFFFH (528~131071)

(Note) For the 1/2 + pulse swallow mode, the actual divide number is twice the programmed number.

- Direct divide mode (13bits)

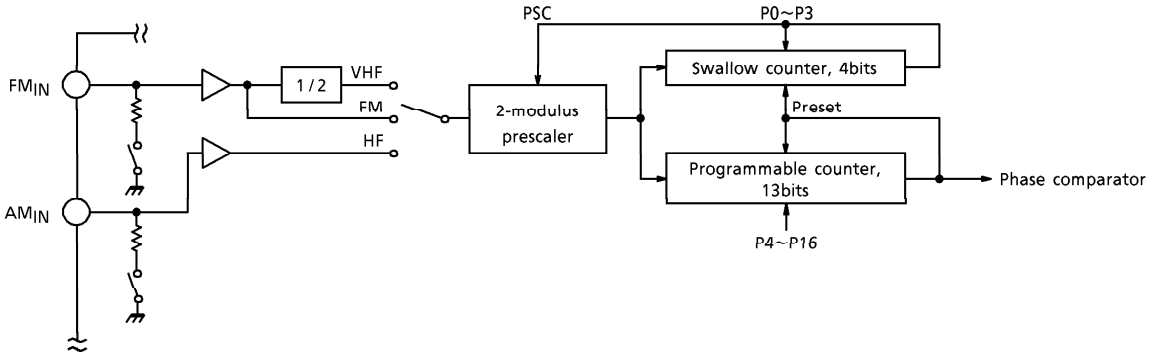


The range of divide numbers that can be set (direct divide mode) n = 10H~1FFFH (16~8191)

(Note) In direct divide mode, the data in P0~P3 does not have any effect, with P4 being the LSB.

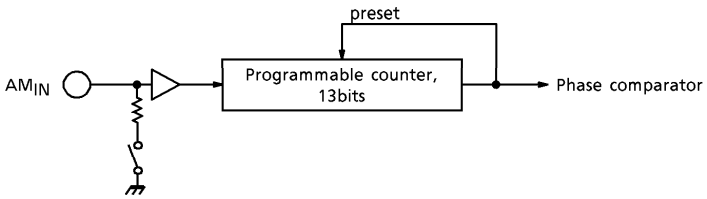
(2) Circuit configuration of prescaler and programmable counter

① Circuit configuration in pulse swallow mode



This circuit is configured with a 2-modulus prescaler, 4bit swallow counter, and 13bit programmable counter.
During VHF, a 1/2 prescaler is added in the preceding stage.

② Circuit configuration in direct divide mode



In direct divide mode, the prescaler is bypassed, and only the 13bit programmable counter is used.

③ The FM-IN and AM-IN inputs each contain an amp, so they can operate with a capacitor-coupled, small amplitude.

3. Reference frequency divider

This divider can generate 7 kinds of reference frequencies by dividing the oscillation frequency of an external 75kHz crystal resonator.

(1) Setting reference frequency

Use the R0~R2 bits for this setting.

R2	R1	R0	REFERENCE FREQUENCY
0	0	0	1kHz
0	0	1	3kHz
0	1	0	3.125kHz
0	1	1	5kHz
1	0	0	6.25kHz
1	0	1	12.5kHz
1	1	0	25kHz
1	1	1	Inhibited

4. Phase comparator

The phase comparator compares phases between the reference frequency signal supplied by the reference frequency divider and the programmable counter's divide-by-n output signal and outputs the difference. In this way, it controls the VCO via a low-pass filter so that the frequencies and phases of these two signals are matched.
Since this phase comparator has two tri-state buffer DO1 and DO2 pins output in parallel, filter constants can be set to an optimum value in each FM, VHF, and AM band.
These outputs also can be used for general-purpose output as set by the DO control bits. Moreover, the DO1 and DO2 pins can be placed in the high-impedance state. Thus, using the DO1 and DO2 pins, it is possible to improve the PLL loop's lock-up time and other characteristics.

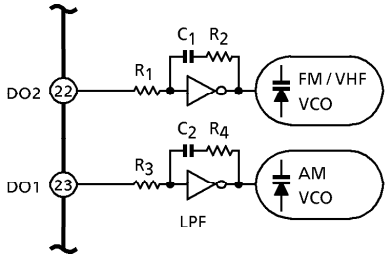
(1) DO control bits

DO CONTROL BITS

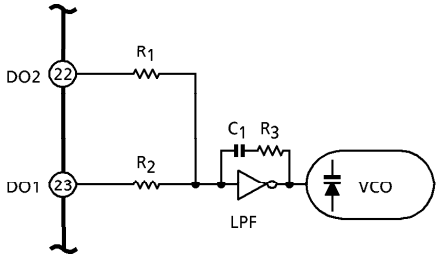
DO1	DO1	DO2	DO2
M0	M1	M0	M1

⇒

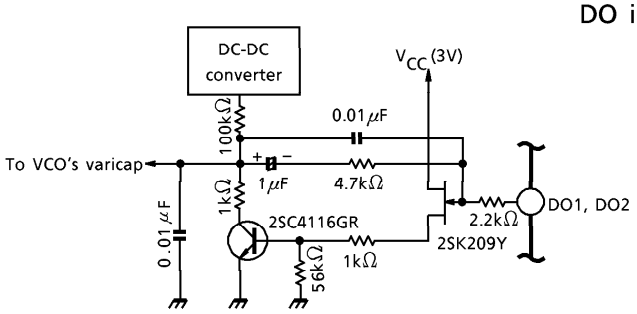
M0	M1	DO OUTPUT STATE
0	0	Phase comparator output
1	0	Output driven low
0	1	Output driven high
1	1	Output in high impedance



When setting time constant in each band



When using LPF in common
(filter constants switched over by placing DO in high-impedance state)



Example of active-low bus filter (reference)

(Note) The filter circuits shown above are merely examples for your reference. The actual circuit must be designed after considering your system's band configuration and required characteristics.

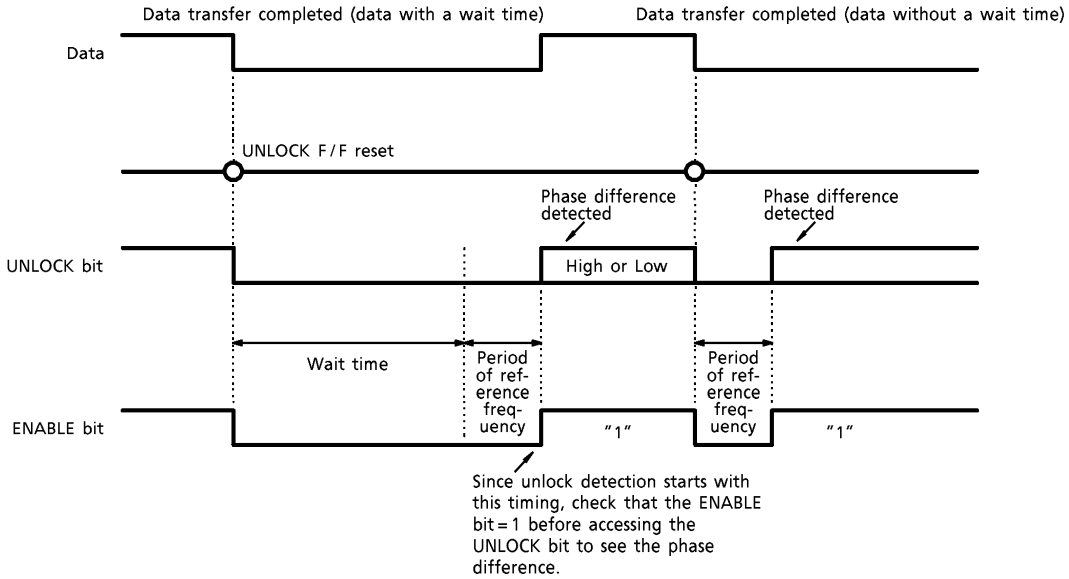
5. Unlock detection bit

This bit is used to detect the PLL's lock condition. Specifically, this is accomplished by using the UNLOCK bit. It detects the phase difference between the reference frequency and the programmable counter's divide-by-n output in periods of the reference frequency.

(1) Unlock detection bit

Unlock detect operation detects the phase difference between the reference frequency and the programmable counter's divide-by-n output at falling edges of the reference frequency signal. If the phases are found unmatched, that is, not locked in phase, the UNLOCK F/F is set (UNLOCK bit = 1).
The UNLOCK F/F is reset each time the RESET bit is set to 1.
Since the divide number setup and RESET bit are sent in the same data, a wait time is provided. Any desired wait time can be selected by wait time bits. Unlock detect operation is begun a wait time after the data is transferred.
Therefore, make sure that the wait time is set in relation to the lock-up time.
Furthermore, since the phase difference is detected in periods of the reference frequency, the UNLOCK bit must be waited for a duration of (period of reference frequency) + (wait time) after the UNLOCK F/F is reset before the bit can be accessed. For this purpose, an ENABLE bit is provided. Check to see that the ENABLE bit = 1 before you access the UNLOCK bit.
This ENABLE bit is reset each time the RESET bit is set to 1, as is the UNLOCK F/F. When the ENABLE bit = 1, you are assured that the lock condition is detected correctly.

UNLOCK DETECTION TIMING



(2) Lock detection bit and wait time bits

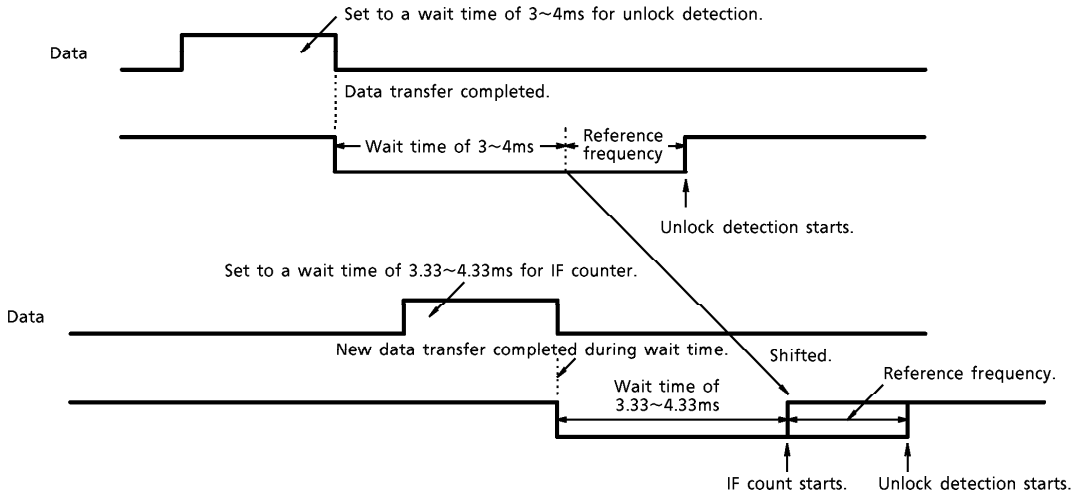
- Lock detection bit

ENABLE	UNLOCK	STATE
0	Invalid data	—
1	0	Lock
	1	Unlock

- Wait time bits

W1	W0	UNLOCK	IF COUNTER
0	0	None	0~1ms
0	1	1~2ms	1.33~2.33ms
1	0	3~4ms	3.33~4.33ms
1	1	7~8ms	7.33~8.33ms

(Note) These bits are used in common to set a wait time for the IF counter and unlock detection. Therefore, in cases when they are set to any combination other than W1 = W0 = 0, if either function is restarted during a wait time for the IF counter or unlock detection, the wait time for the function restarted now has priority and the function in a wait time is postponed. Then each function starts after the wait time for the function restarted elapses.



6. IF counter

This is a 20bit general-purpose IF counter that can be used, for example, to detect an auto stop signal by counting the intermediate frequency (IF) of FM or AM during auto tuning.
Measurement with a general-purpose IF counter is accomplished by setting a gate time according to the IF input's frequency band and then setting the START bit to 1 to start the IF counter.
In this case, since the PLL's divide number data and the START bit are in the same data, a wait time is provided. To set this wait time, the same W1 and W0 bits are used that are used to set a wait time for unlock detection.
Thus, a wait time after data transfer is completed, clock is input from the IF pin to the 20bit binary counter at the gate time you have set, and and the counter counts the number of clock pulses input until count expires. You can reference the BUSY bit to determine when the IF counter has finished counting.
Next that the OVER bit is set to 1 when the count value exceeds 2^{20} pulses that have been input.
The frequency fed to the IF input pin can be measures by taking in the IF data from F_0~F_{19} when both BUSY and OVER bits = 0.

(1) General-purpose counter control bits

① G0, G1 bits ..... Bits to choose a gate time

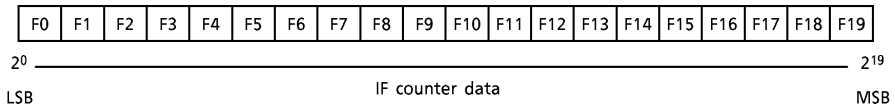
G1	G0	GATE TIME
0	0	1ms
0	1	4ms
1	0	16ms
1	1	64ms

② START bit ..... Each time the START bit is set to 1, measurement is started after resetting the general-purpose IF counter.

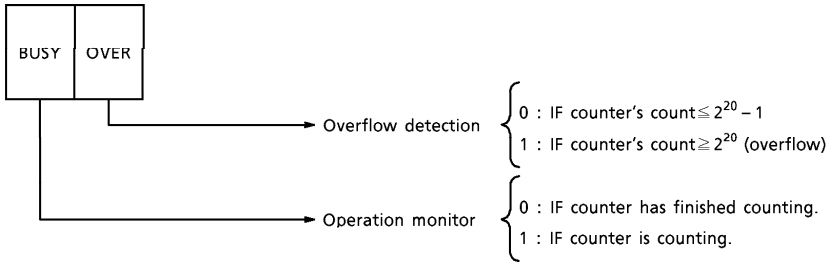
(2) General-purpose counter output bits

① General-purpose counter data output bits (F_0~F_{19})

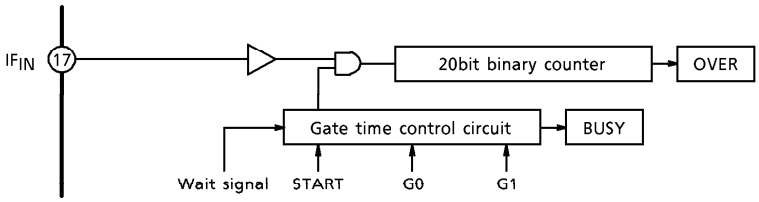
The result of counts counted by the general-purpose counter can be read out in binary from the output register bits F_0~F_{19}.



② General-purpose counter operation detect bits

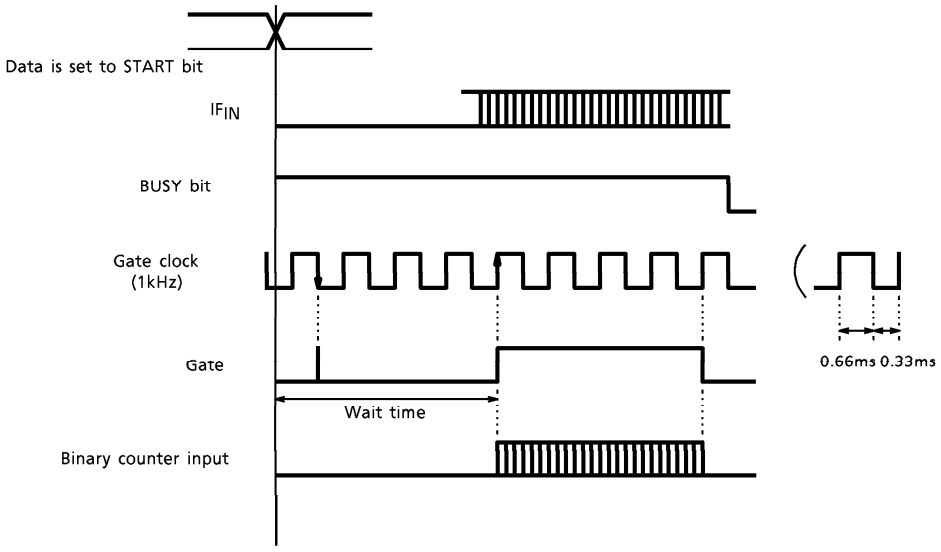


(3) Circuit configuration of IF counter



The IF counter block consists of an input amp, gate time control circuit, and a 20bit binary counter.

(Note) The IF_{IN} pin contains an amp, and can operate with a capacitor-coupled small amplitude.



7. General-purpose I/O ports

The device has general-purpose I/O ports controlled by a serial interface.

Input mode

I/O port input/output setup bits

I/O C1	I/O C2	I/O C3	I/O C4

I/OC1~4 { 0 : I/O1 thru 4 are set for input
1 : I/O1 thru 4 are set for output

I/O port output setup bits (when I/O ports are set for input)

I/O 1	I/O 2	I/O 3	I/O 4

I/O1~4 { 0 : I/O1 thru 4 output are driven low
1 : I/O1 thru 4 output are driven high

OUT port output setup bits

OUT -1	OUT -2	OUT -3	OUT -4

OUT1~4 { 0 : OUT1 thru 4 outputs are pulled low (N-channel open-drain ON).
1 : OUT1 thru 4 outputs are placed in the high-impedance state (N-channel open-drain OFF).

Output mode

I/O port input data read bits

I/O 1	I/O 2	I/O 3	I/O 4

I/O1~4 { 0 : Input level is low
1 : Input level is high

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~4.0	V
Input Voltage 1	V_{IN1}	−0.3~V_{DD} + 0.3	V
Input Voltage 2	V_{IN2}	−0.3~6.0 (Note 1)	V
N-channel Open-Drain Output Tolerance	V_{OUT}	−0.3~6.0	V
Power Dissipation	P_D	400	mW
Operating Temperature	T_{opr}	−10~60	°C
Storage Temperature	T_{stg}	−55~125	°C

(Note 1) D_{IN}, CK, and CE pins

ELECTRICAL CHARACTERISTICS (Unless otherwise specified Ta = 25°C, V_{DD} = 3V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V_{DD}	—	(*)	1.8	3.0	3.6	V
Data Retention Voltage	V_{HD}	—	INH = "L"	0.8	~	3.6	V
Operating Supply Current	I_{DD}	—	INH = "H", FM_{IN} = 230MHz, output non-loaded	—	9	15	mA
Data Retention Current	I_{HD}	—	INH = "L"	—	0.1	10	μA

CRYSTAL OSCILLATOR (X_{IN}, X_{OUT}, V_{XT})

Crystal Oscillation Frequency	f_{XT}	—	(*)	—	75	—	kHz
Crystal Oscillation Start Time	t_{ST}	—	75kHz crystal resonator (KF-38R5), C_L = 15pF	—	0.3	0.6	s
X_{IN} Input Feedback Resistance	R_{fXT}	—	Between X_{IN} and X_{OUT} pins	—	15	—	MΩ
X_{OUT} Output Resistance	R_{OUT}	—	X_{OUT} pin	—	4	—	kΩ
Constant Voltage Power Supply	V_{XT}	—		—	1.4	—	V

(*) Guaranteed at V_{DD} = 1.8~3.6V and Ta = −10~60°C

PROGRAMMABLE COUNTER, IF COUNTER, OPERATING FREQUENCY RANGE (FM_{IN}, AM_{IN}, IF_{IN})

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
FM_{IN}	f_{VHF}	—	Sine wave input during $V_{IN} = 0.2V_{p-p}$ input 1/2 + pulse swallow mode (*)	50	~	230	MHz
	f_{FM}	—	Sine wave input during $V_{IN} = 0.2V_{p-p}$ input pulse swallow mode (*)	50	~	130	
AM_{IN}	f_{HF}	—	Sine wave input during $V_{IN} = 0.2V_{p-p}$ input pulse swallow mode (*)	1	~	20	MHz
	f_{LF}	—	Sine wave input during $V_{IN} = 0.2V_{p-p}$ input direct divide mode (*)	0.5	~	10	
IF_{IN}	f_{IF}	—	Sine wave input during $V_{IN} = 0.2V_{p-p}$ input direct divide mode (*)	0.35	~	12	MHz
Input Amplitude Range	V_{IN}	—	FM_{IN}, AM_{IN}, and IF_{IN} pins (*)	0.2	~	V_{DD} − 0.5	V_{p-p}
AM_{IN}, FM_{IN} Input Feedback Resistance	R_{f1}	—	FM_{IN}, and AM_{IN} pins	150	300	600	kΩ
IF_{IN} Input Feedback Resistance	R_{f2}	—	IF_{IN} pin	500	1000	2000	kΩ

SERIAL INTERFACE (D_{OUT}, D_{IN}, CK, CE)

Input Leakage Current		I_{LI}	—	$V_{IH} = 5.5V$, $V_{IL} = 0V$, D_{IN}, CK, CE pins	—	—	± 1.0	μA
Input Voltage	High Level	V_{IH}	—	D_{IN}, CK, and CE pins	0.8	~	5.5	V
	Low Level	V_{IL}	—	D_{IN}, CK, and CE pins	0	~	0.3	
Low Level Output Current		I_{OL1}	—	$V_{OL} = 0.3V$, D_{OUT} pin	0.7	1.4	—	mA
Output OFF Leakage Current		I_{OFF}	—	$V_{IH} = 5.5V$, D_{OUT} pin	—	—	1.0	μA

OUTPUT PORTS (OUT-1~OUT-4)

Low Level Output Current		I_{OL1}	—	$V_{OL} = 0.3V$	0.7	1.4	—	mA
Output OFF Leakage Current		I_{OFF}	—	$V_{IH} = 5.5V$	—	—	1.0	μA

I/O PORTS (I/O-1 to I/O-4)

Input Leakage Current		I_{LI}	—	$V_{IH} = 3.0V$, $V_{IL} = 0V$	—	—	± 1.0	μA
Input Voltage	High Level	V_{IH}	—		2.4	~	3.0	V
	Low Level	V_{IL}	—		0	~	0.6	
Output Current	High Level	I_{OH}	—	$V_{OH} = 2.7V$	− 0.4	− 0.8	—	mA
	Low Level	I_{OL}	—	$V_{OL} = 0.3V$	0.4	0.8	—	

(*) Guaranteed at $V_{DD} = 1.8$~$3.6V$ and $Ta = -10$~$60°C$

DO OUTPUT (DO1, DO2)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output OFF Leakage Current		I_{TL}	—	V_{TLH} = 3.0V, V_{TLL} = 0V	—	—	± 1.0	μA
Output Current	High Level	I_{OH}	—	V_{OH} = 2.7V	− 0.4	− 0.8	—	mA
	Low Level	I_{OL}	—	V_{OL} = 0.3V	0.4	0.8	—	

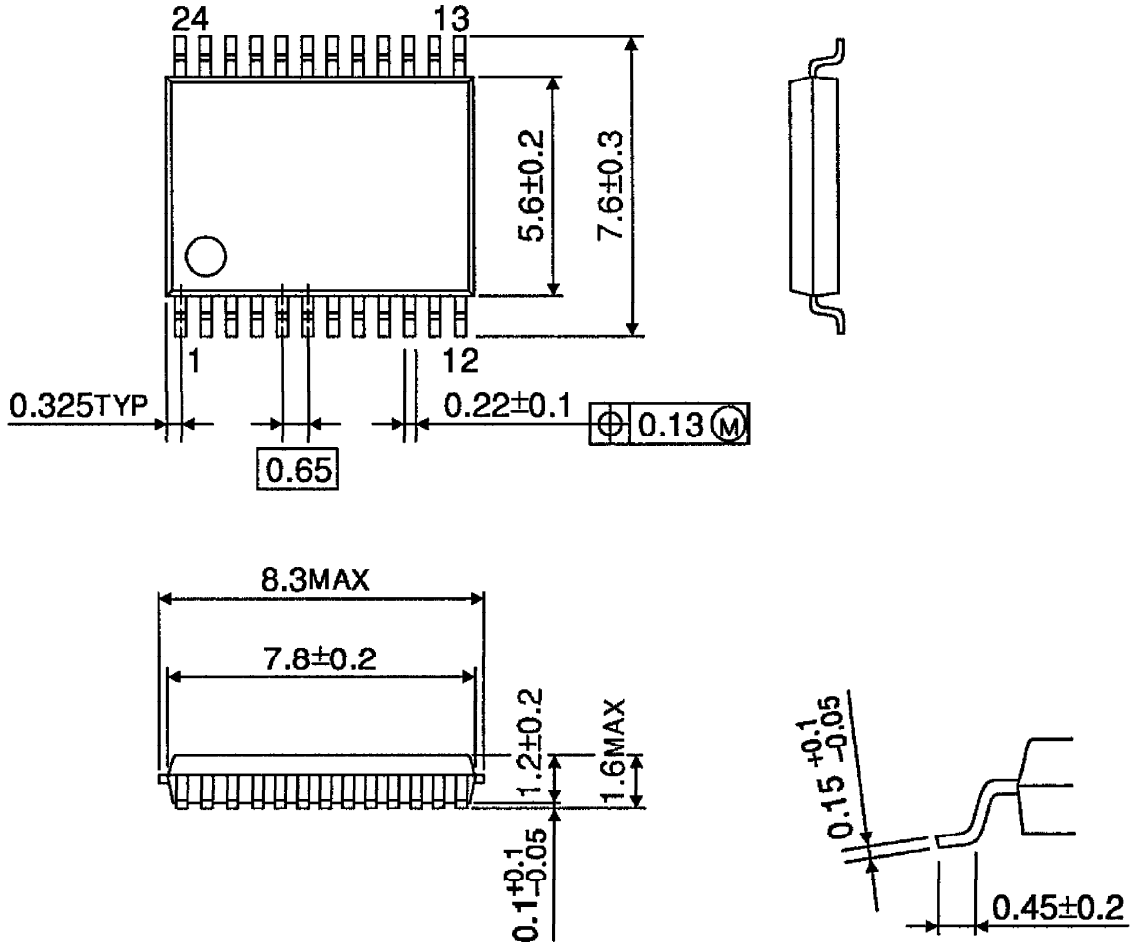
TEST AND $\overline{\text{INH}}$ PINS

Input Pull-Down Resistance		R_I	—	TEST pin	25	50	100	kΩ
Input Voltage	High Level	V_{IH}	—	$\overline{\text{INH}}$ pin	2.4	~	3.0	V
	Low Level	V_{IL}	—	$\overline{\text{INH}}$ pin	0	~	0.6	

OUTLINE DRAWING

SSOP24-P-300A

Unit : mm



Weight : 0.31g (Typ.)