- **Highest-Performance Floating-Point Digital Signal Processor (DSP): TMS320C6713**
  - **Eight 32-Bit Instructions/Cycle**
  - **32/64-Bit Data Word**
  - **225-, 150-MHz Clock Rate**
  - **4.4-, 6.7-ns Instruction Cycle Time**
  - **1800 MIPS/1350 MFLOPS, 1200 MIPS /900 MFLOPS**
  - **Rich Peripheral Set, Optimized for Audio**
- **VelociTI™ Advanced Very Long Instruction Word (VLIW) TMS320C67x™ DSP Core**
  - **Eight Independent Functional Units:**
    - **Two ALUs (Fixed-Point)**
    - **Four ALUs (Floating- and Fixed-Point)**
    - **Two Multipliers (Floating- and Fixed-Point)**
  - **Load-Store Architecture With 32 32-Bit General-Purpose Registers**
  - **Instruction Packing Reduces Code Size**
  - **All Instructions Conditional**
- **Instruction Set Features**
  - **Native Instructions for IEEE 754**
    - **Single- and Double-Precision**
  - **Byte-Addressable (8-, 16-, 32-Bit Data)**
  - **8-Bit Overflow Protection**
  - **Saturation; Bit-Field Extract, Set, Clear; Bit-Counting; Normalization**
- **L1/L2 Memory Architecture**
  - **4K-Byte L1P Program Cache (Direct-Mapped)**
  - **4K-Byte L1D Data Cache (2-Way)**
  - **256K-Byte L2 Memory, With 64K-Byte L2 Unified Cache/Mapped RAM**
  - **192K-Byte Additional L2 Mapped RAM**
- **Device Configuration**
  - **Boot Mode: HPI, 8-, 16-, and 32-Bit ROM Boot**
  - **Endianness: Little Endian, Big Endian**
- **32-Bit External Memory Interface (EMIF)**
  - **Glueless Interface to SRAM, EPROM, Flash, SBSRAM, and SDRAM**
  - **512M-Byte Total Addressable External Memory Space**
- **Enhanced Direct-Memory-Access (EDMA) Controller (16 Independent Channels)**
- **16-Bit Host-Port Interface (HPI)**
- **Two Multichannel Audio Serial Ports (McASPs)**
  - **Two Independent Clock Zones Each (1 TX and 1 RX)**
  - **Eight Serial Data Pins Per Port: Individually Assignable to any of the Clock Zones**
  - **Each Clock Zone Includes:**
    - **Programmable Clock Generator**
    - **Programmable Frame Sync Generator**
    - **TDM Streams From 2-32 Time Slots**
    - **Support for Slot Size: 8, 12, 16, 20, 24, 28, 32 Bits**
    - **Data Formatter for Bit Manipulation**
  - **Wide Variety of I2S and Similar Bit Stream Formats**
  - **Integrated Digital Audio Interface Transmitter (DIT) Supports:**
    - **S/PDIF, IEC60958-1, AES-3 Formats**
    - **Up to 16 transmit pins**
    - **Enhanced Channel Status/User Data RAM**
  - **Extensive Error Checking and Recovery**
- **Two Inter-Integrated Circuit (I^2C) Buses Multi-Master and Slave Interfaces**
- **Two Multichannel Buffered Serial Ports (McBSPs):**
  - **Serial-Peripheral-Interface (SPI)**
  - **High-Speed TDM Interface**
  - **AC97 Interface**
- **Two 32-Bit General-Purpose Timers**
- **One Dedicated General-Purpose Input/Output Module With 16 pins**
- **Flexible Phase-Locked-Loop (PLL) Based Clock Generator Module**
- **IEEE-1149.1 (JTAG†) Boundary-Scan-Compatible**
- **Package Options:**
  - **208-Pin PowerPAD™ Plastic (Low-Profile) Quad Flatpack (PYP)**
  - **256-Pin Ball Grid Array Package (GFN)**
- **0.13-μm/6-Level Metal Process**
  - **CMOS Technology**
- **3.3-V I/Os, 1.2-V Internal**

PRODUCT PREVIEW

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† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

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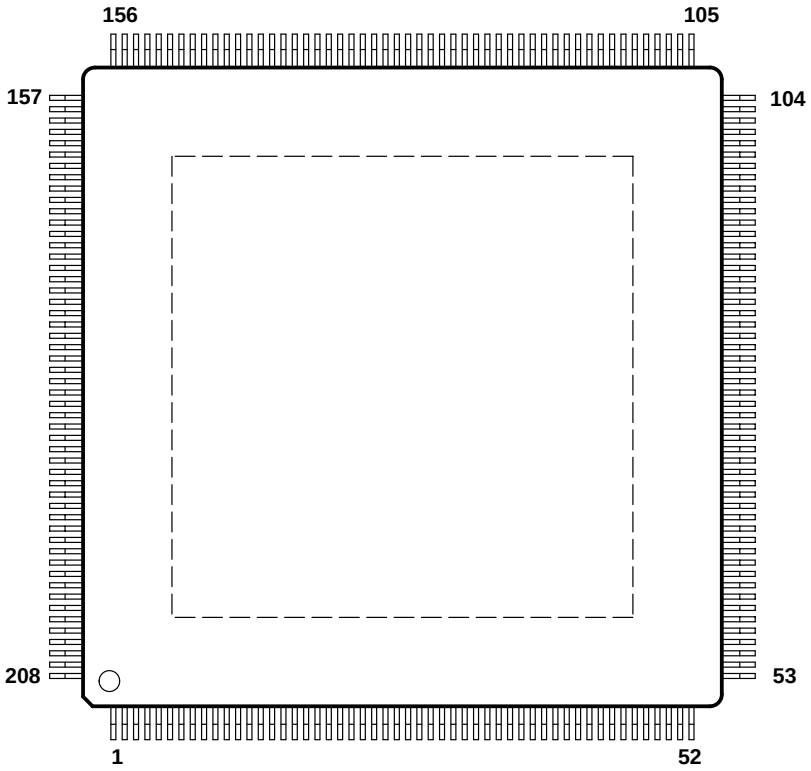
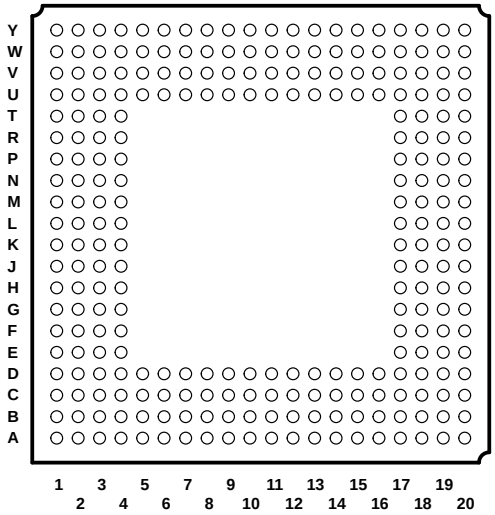
PYP PowerPAD™ QFP package (top view)

PYP 208-PIN PowerPAD™ PLASTIC QUAD FLATPACK (PQFP)
(TOP VIEW)



GFN BGA package (bottom view)

GFN 256-PIN BALL GRID ARRAY (BGA) PACKAGE
(BOTTOM VIEW)



PRODUCT PREVIEW

description

The TMS320C67x™ DSPs (including the TMS320C6713 device) compose the floating–point DSP generation in the TMS320C6000™ DSP platform. The TMS320C6713 (C6713) device is based on the high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making this DSP an excellent choice for multichannel and multifunction applications.

Operating at 225 MHz, the C6713 delivers up to 1350 million floating-point operations per second (MFLOPS), 1800 million instructions per second (MIPS), and with dual fixed-/floating-point multipliers up to 450 million multiply-accumulate operations per second (MMACS).

The C6713 uses a two-level cache-based architecture and has a powerful and diverse set of peripherals. The Level 1 program cache (L1P) is a 4K-Byte direct-mapped cache and the Level 1 data cache (L1D) is a 4K-Byte 2-way set-associative cache. The Level 2 memory/cache (L2) consists of a 256K-Byte memory space that is shared between program and data space. 64K Bytes of the 256K Bytes in L2 memory can be configured as mapped memory, cache, or combinations of the two. The remaining 192K Bytes in L2 serves as mapped SRAM.

The C6713 has a rich peripheral set that includes two Multichannel Audio Serial Ports (McASPs), two Multichannel Buffered Serial Ports (McBSPs), two Inter-Integrated Circuit (I2C) buses, one dedicated General-Purpose Input/Output (GPIO) module, two general-purpose timers, a host-port interface (HPI), and a glueless external memory interface (EMIF) capable of interfacing to SDRAM, SBSRAM, and asynchronous peripherals.

The two McASP interface modules each support one transmit and one receive clock zone. Each of the McASP has eight serial data pins which can be individually allocated to any of the two zones. The serial port supports time-division multiplexing on each pin from 2 to 32 time slots. The C6713 has sufficient bandwidth to support all 16 serial data pins transmitting a 192 kHz stereo signal. Serial data in each zone may be transmitted and received on multiple serial data pins simultaneously and formatted in a multitude of variations on the Philips Inter-IC Sound (I2S) format.

In addition, the McASP transmitter may be programmed to output multiple S/PDIF, IEC60958, AES-3 encoded data channels simultaneously, with a single RAM containing the full implementation of user data and channel status fields.

The McASP also provides extensive error-checking and recovery features, such as the bad clock detection circuit for each high-frequency master clock which verifies that the master clock is within a programmed frequency range.

The two I2C ports on the TMS320C6713 allow the DSP to easily control peripheral devices, boot from a serial EEPROM, and communicate with a host processor.

The TMS320C67x DSP generation is supported by the TI eXpressDSP™ set of industry benchmark development tools, including a highly optimizing C/C++ Compiler, the Code Composer Studio™ Integrated Development Environment (IDE), JTAG-based emulation and real-time debugging, and the DSP/BIOS™ kernel.

device characteristics

Table 1 provides an overview of the C6713 DSP. The table shows significant features of the C6713 device, including the capacity of on-chip RAM, the peripherals, the execution time, and the package type with pin count. For more details on the C67x™ DSP device part numbers and part numbering, see Table 32 and Figure 11.

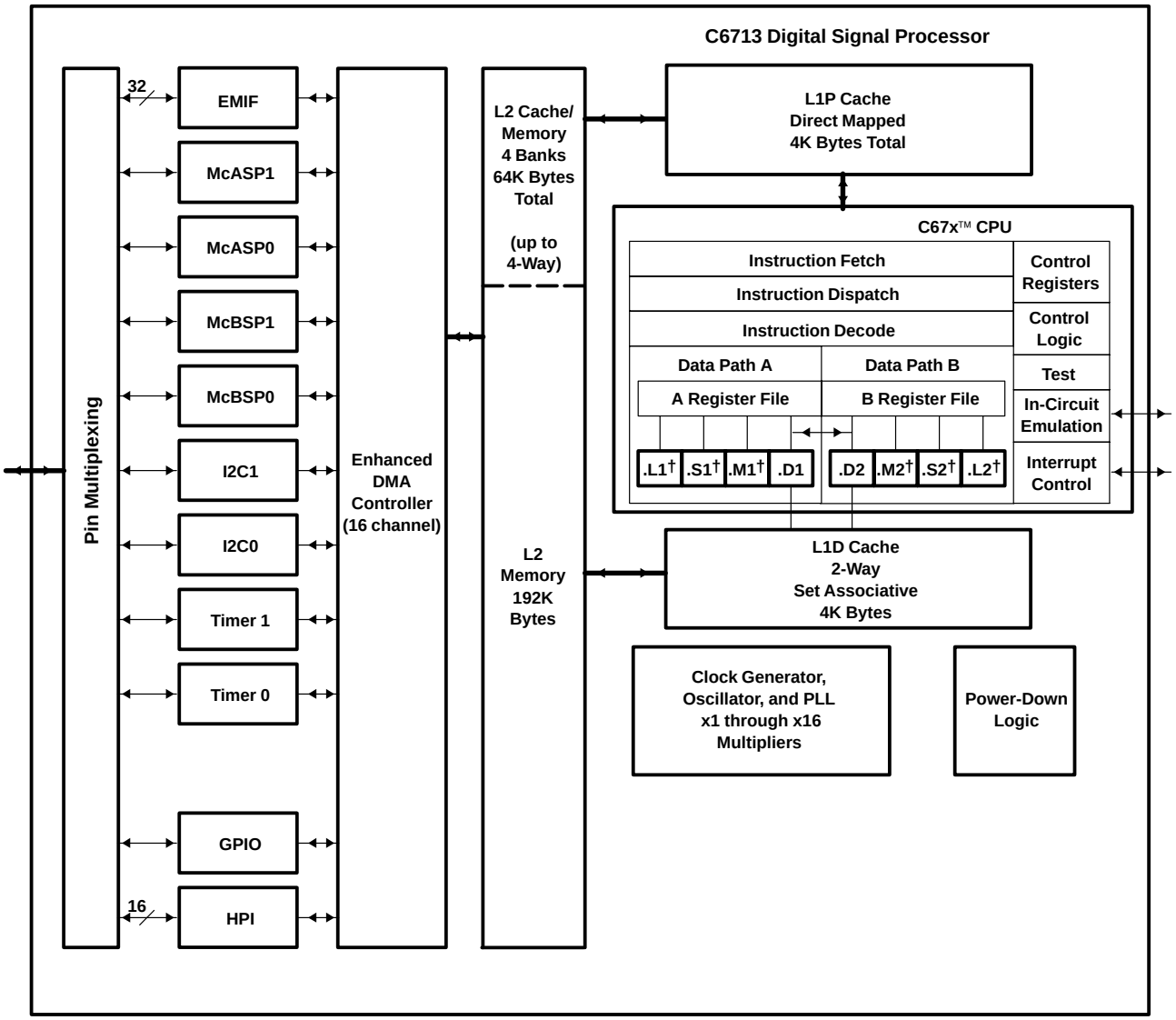
Table 1. Characteristics of the C6713 Processor

HARDWARE FEATURES		C6713 (FLOATING-POINT DSP)	
		GFN	PYP
Peripherals	EMIF	1 (32 bit)	1 (16 bit)
	EDMA (16 Channels)	1	
	HPI (16 bit)	1	
	McASPs	2	
	I2Cs	2	
	McBSPs	2	
	32-Bit Timers	2	
	GPIO Modules	1	
On-Chip Memory	Size (Bytes)	264K	
	Organization	4K-Byte (4KB) L1 Program (L1P) Cache 4KB L1 Data (L1D) Cache 64KB Unified L2 Cache/Mapped RAM 192KB L2 Mapped RAM	
CPU ID+CPU Rev ID	Control Status Register (CSR.[31:16])	0x0203	
Frequency	MHz	225, 150	150
Cycle Time	ns	4.4 ns (C6713GFN-225), 6.7 ns (C6713GFN-150)	6.7 ns (C6713PYP-150)
Voltage	Core (V)	1.2	
	I/O (V)	3.3	
Clock Generator Options	Prescaler Multiplier Postscaler	/1, /2, /3, ..., /32 x1, x2, x3, ..., x16 /1, /2, /3, ..., /32	
Packages	27 x 27 mm	256-Pin BGA (GFN)	–
	28 x 28 mm	–	208-Pin PowerPAD™ PQFP (PYP)
Process Technology	µm	0.13	
Product Status Product Preview (PP) Advance Information (AI) Production Data (PD)		PP	PP

PRODUCT PREVIEW

C67x is a trademark of Texas Instruments.

functional block and CPU (DSP core) diagram



† In addition to fixed-point instructions, these functional units execute floating-point instructions.

EMIF interfaces to:
–SDRAM
–SBSRAM
–SRAM,
–ROM/Flash, and
–I/O devices

McBSPs interface to:
–SPI Control Port
–High-Speed TDM Codecs
–AC97 Codecs
–Serial EEPROM

McASPs interface to:
–I2S Multichannel ADC, DAC, Codec, DIR
–DIT: Multiple Outputs

PRODUCT PREVIEW

CPU (DSP core) description

The TMS320C6713 floating-point digital signal processor is based on the C67x CPU. The CPU fetches VelociTI™ advanced very-long instruction words (VLIW) (256 bits wide) to supply up to eight 32-bit instructions to the eight functional units during every clock cycle. The VelociTI™ VLIW architecture features controls by which all eight units do not have to be supplied with instructions if they are not ready to execute. The first bit of every 32-bit instruction determines if the next instruction belongs to the same execute packet as the previous instruction, or whether it should be executed in the following clock as a part of the next execute packet. Fetch packets are always 256 bits wide; however, the execute packets can vary in size. The variable-length execute packets are a key memory-saving feature, distinguishing the C67x CPU from other VLIW architectures.

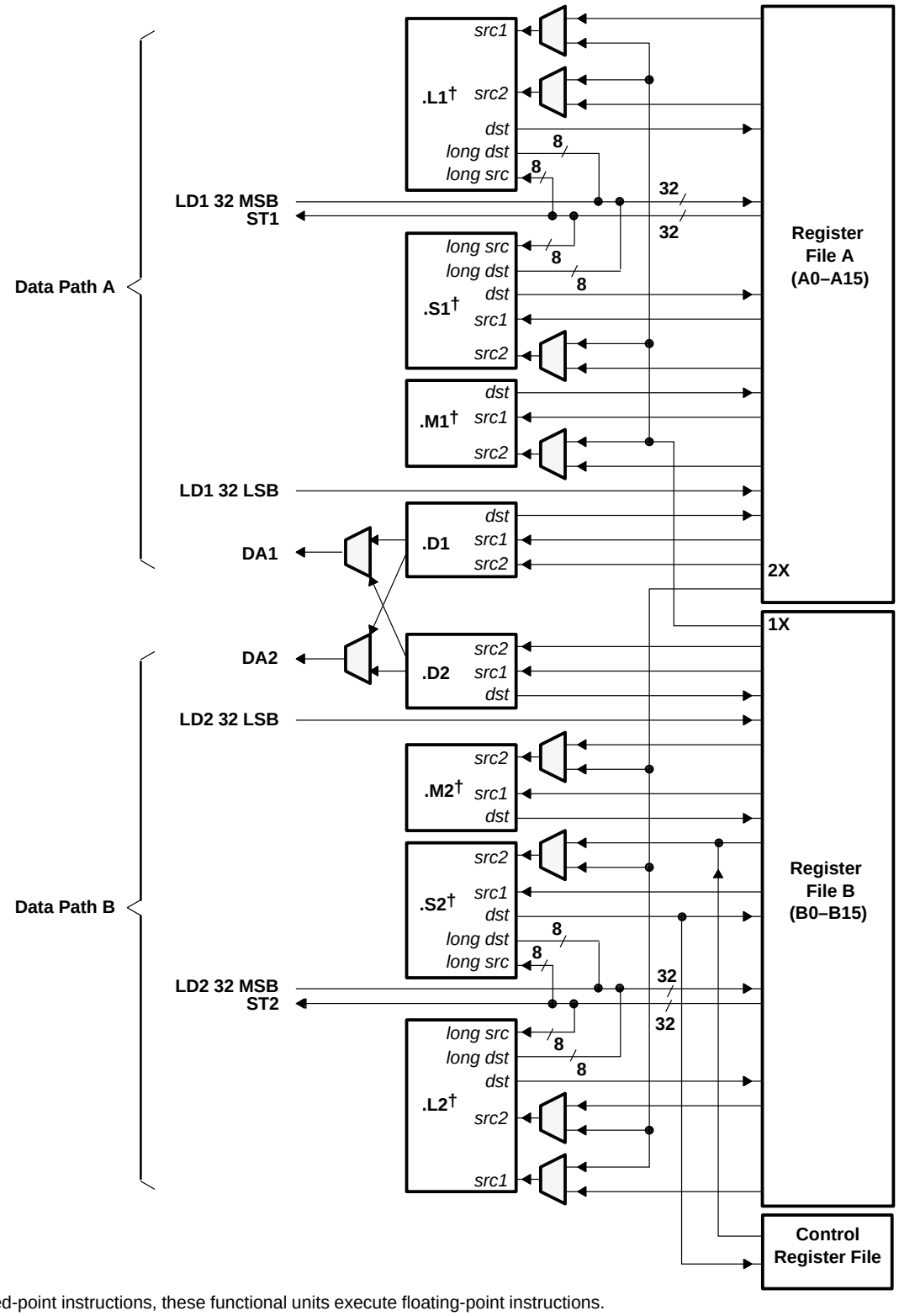
The CPU features two sets of functional units. Each set contains four units and a register file. One set contains functional units .L1, .S1, .M1, and .D1; the other set contains units .D2, .M2, .S2, and .L2. The two register files each contain 16 32-bit registers for a total of 32 general-purpose registers. The two sets of functional units, along with two register files, compose sides A and B of the CPU (see the functional block and CPU diagram and Figure 1). The four functional units on each side of the CPU can freely share the 16 registers belonging to that side. Additionally, each side features a single data bus connected to all the registers on the other side, by which the two sets of functional units can access data from the register files on the opposite side. While register access by functional units on the same side of the CPU as the register file can service all the units in a single clock cycle, register access using the register file across the CPU supports one read and one write per cycle.

The C67x CPU executes all C62x instructions. In addition to C62x fixed-point instructions, the six out of eight functional units (.L1, .S1, .M1, .M2, .S2, and .L2) also execute floating-point instructions. The remaining two functional units (.D1 and .D2) also execute the new LDDW instruction which loads 64 bits per CPU side for a total of 128 bits per cycle.

Another key feature of the C67x CPU is the load/store architecture, where all instructions operate on registers (as opposed to data in memory). Two sets of data-addressing units (.D1 and .D2) are responsible for all data transfers between the register files and the memory. The data address driven by the .D units allows data addresses generated from one register file to be used to load or store data to or from the other register file. The C67x CPU supports a variety of indirect addressing modes using either linear- or circular-addressing modes with 5- or 15-bit offsets. All instructions are conditional, and most can access any one of the 32 registers. Some registers, however, are singled out to support specific addressing or to hold the condition for conditional instructions (if the condition is not automatically “true”). The two .M functional units are dedicated for multiplies. The two .S and .L functional units perform a general set of arithmetic, logical, and branch functions with results available every clock cycle.

The processing flow begins when a 256-bit-wide instruction fetch packet is fetched from a program memory. The 32-bit instructions destined for the individual functional units are “linked” together by “1” bits in the least significant bit (LSB) position of the instructions. The instructions that are “chained” together for simultaneous execution (up to eight in total) compose an execute packet. A “0” in the LSB of an instruction breaks the chain, effectively placing the instructions that follow it in the next execute packet. If an execute packet crosses the fetch-packet boundary (256 bits wide), the assembler places it in the next fetch packet, while the remainder of the current fetch packet is padded with NOP instructions. The number of execute packets within a fetch packet can vary from one to eight. Execute packets are dispatched to their respective functional units at the rate of one per clock cycle and the next 256-bit fetch packet is not fetched until all the execute packets from the current fetch packet have been dispatched. After decoding, the instructions simultaneously drive all active functional units for a maximum execution rate of eight instructions every clock cycle. While most results are stored in 32-bit registers, they can be subsequently moved to memory as bytes or half-words as well. All load and store instructions are byte-, half-word, or word-addressable.

CPU (DSP core) description (continued)



† In addition to fixed-point instructions, these functional units execute floating-point instructions.

Figure 1. TMS320C67x™ CPU (DSP Core) Data Paths

memory map summary

Table 2 shows the memory map address ranges of the C6713 device.

Table 2. TMS320C6713 Memory Map Summary

MEMORY BLOCK DESCRIPTION	BLOCK SIZE (BYTES)	HEX ADDRESS RANGE
Internal RAM (L2)	192K	0000 0000 – 0002 FFFF
Internal RAM/Cache	64K	0003 0000 – 0003 FFFF
Reserved	24M – 256K	0004 0000 – 017F FFFF
External Memory Interface (EMIF) Registers	256K	0180 0000 – 0183 FFFF
L2 Registers	128K	0184 0000 – 0185 FFFF
Reserved	128K	0186 0000 – 0187 FFFF
HPI Registers	256K	0188 0000 – 018B FFFF
McBSP 0 Registers	256K	018C 0000 – 018F FFFF
McBSP 1 Registers	256K	0190 0000 – 0193 FFFF
Timer 0 Registers	256K	0194 0000 – 0197 FFFF
Timer 1 Registers	256K	0198 0000 – 019B FFFF
Interrupt Selector Registers	512	019C 0000 – 019C 01FF
Device Configuration Registers	4	019C 0200 – 019C 0203
Reserved	256K – 516	019C 0204 – 019F FFFF
EDMA RAM and EDMA Registers	256K	01A0 0000 – 01A3 FFFF
Reserved	768K	01A4 0000 – 01AF FFFF
GPIO Registers	16K	01B0 0000 – 01B0 3FFF
Reserved	240K	01B0 4000 – 01B3 FFFF
I2C0 Registers	16K	01B4 0000 – 01B4 3FFF
I2C1 Registers	16K	01B4 4000 – 01B4 7FFF
Reserved	16K	01B4 8000 – 01B4 BFFF
McASP0 Registers	16K	01B4 C000 – 01B4 FFFF
McASP1 Registers	16K	01B5 0000 – 01B5 3FFF
Reserved	160K	01B5 4000 – 01B7 BFFF
PLL Registers	8K	01B7 C000 – 01B7 DFFF
Reserved	4M + 520K	01B7 E000 – 01FF FFFF
QDMA Registers	52	0200 0000 – 0200 0033
Reserved	16M – 52	0200 0034 – 02FF FFFF
Reserved	720M	0300 0000 – 2FFF FFFF
McBSP0 Data	64M	3000 0000 – 33FF FFFF
McBSP1 Data	64M	3400 0000 – 37FF FFFF
Reserved	64M	3800 0000 – 3BFF FFFF
McASP0 Data	1M	3C00 0000 – 3C0F FFFF
McASP1 Data	1M	3C10 0000 – 3C1F FFFF
Reserved	1G + 62M	3C20 0000 – 7FFF FFFF
EMIF CE0†	256M	8000 0000 – 8FFF FFFF
EMIF CE1†	256M	9000 0000 – 9FFF FFFF
EMIF CE2†	256M	A000 0000 – AFFF FFFF
EMIF CE3†	256M	B000 0000 – BFFF FFFF
Reserved	1G	C000 0000 – FFFF FFFF

† The number of EMIF address pins (EA[21:2]) limits the maximum addressable memory (SDRAM) to 128MB per CE space.

L2 memory structure expanded

Figure 2 shows the detail of the L2 memory structure.

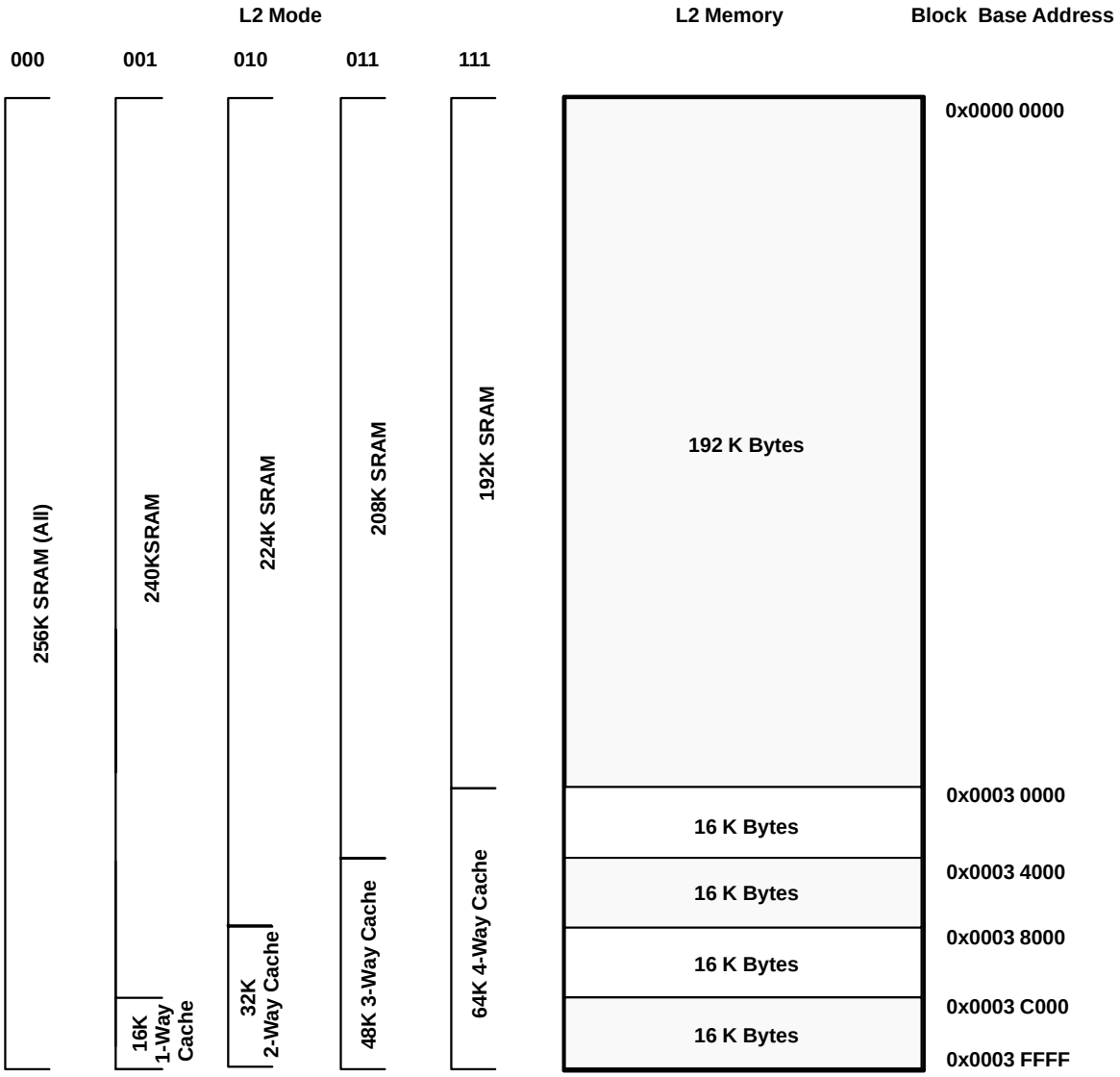


Figure 2. L2 Memory Configuration

peripheral register descriptions

Table 3 through Table 13 identify the peripheral registers for the C6713 device by their register names, acronyms, and hex address or hex address range. For more detailed information on the register contents, bit names, and their descriptions, see the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190).

Table 3. EMIF Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0180 0000	GBLCTL	EMIF global control
0180 0004	CECTL1	EMIF CE1 space control
0180 0008	CECTL0	EMIF CE0 space control
0180 000C	–	Reserved
0180 0010	CECTL2	EMIF CE2 space control
0180 0014	CECTL3	EMIF CE3 space control
0180 0018	SDCTL	EMIF SDRAM control
0180 001C	SDTIM	EMIF SDRAM refresh control
0180 0020	SDEXT	EMIF SDRAM extension
0180 0024 – 0183 FFFF	–	Reserved

Table 4. L2 Cache Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 0000	CCFG	Cache configuration register
0184 4000	L2FBAR	L2 flush base address register
0184 4004	L2FWC	L2 flush word count register
0184 4010	L2CBAR	L2 clean base address register
0184 4014	L2CWC	L2 clean word count register
0184 4020	L1PFBAR	L1P flush base address register
0184 4024	L1PFWC	L1P flush word count register
0184 4030	L1DFBAR	L1D flush base address register
0184 4034	L1DFWC	L1D flush word count register
0184 5000	L2FLUSH	L2 flush register
0184 5004	L2CLEAN	L2 clean register
0184 8200	MAR0	Controls CE0 range 8000 0000 – 80FF FFFF
0184 8204	MAR1	Controls CE0 range 8100 0000 – 81FF FFFF
0184 8208	MAR2	Controls CE0 range 8200 0000 – 82FF FFFF
0184 820C	MAR3	Controls CE0 range 8300 0000 – 83FF FFFF
0184 8240	MAR4	Controls CE1 range 9000 0000 – 90FF FFFF
0184 8244	MAR5	Controls CE1 range 9100 0000 – 91FF FFFF
0184 8248	MAR6	Controls CE1 range 9200 0000 – 92FF FFFF
0184 824C	MAR7	Controls CE1 range 9300 0000 – 93FF FFFF
0184 8280	MAR8	Controls CE2 range A000 0000 – A0FF FFFF
0184 8284	MAR9	Controls CE2 range A100 0000 – A1FF FFFF
0184 8288	MAR10	Controls CE2 range A200 0000 – A2FF FFFF
0184 828C	MAR11	Controls CE2 range A300 0000 – A3FF FFFF
0184 82C0	MAR12	Controls CE3 range B000 0000 – B0FF FFFF
0184 82C4	MAR13	Controls CE3 range B100 0000 – B1FF FFFF
0184 82C8	MAR14	Controls CE3 range B200 0000 – B2FF FFFF
0184 82CC	MAR15	Controls CE3 range B300 0000 – B3FF FFFF
0184 82D0 – 0185 FFFF	–	Reserved

peripheral register descriptions (continued)

Table 5. Interrupt Selector Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
019C 0000	MUXH	Interrupt multiplexer high	Selects which interrupts drive CPU interrupts 10–15 (INT10–INT15)
019C 0004	MUXL	Interrupt multiplexer low	Selects which interrupts drive CPU interrupts 4–9 (INT04–INT09)
019C 0008	EXTPOL	External interrupt polarity	Sets the polarity of the external interrupts (EXT_INT4–EXT_INT7)
019C 000C – 019F FFFF	–	Reserved	

Table 6. EDMA Parameter RAM†

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01A0 0000 – 01A0 0017	–	Parameters for Event 0 (6 words)
01A0 0018 – 01A0 002F	–	Parameters for Event 1 (6 words)
01A0 0030 – 01A0 0047	–	Parameters for Event 2 (6 words)
01A0 0048 – 01A0 005F	–	Parameters for Event 3 (6 words)
01A0 0060 – 01A0 0077	–	Parameters for Event 4 (6 words)
01A0 0078 – 01A0 008F	–	Parameters for Event 5 (6 words)
01A0 0090 – 01A0 00A7	–	Parameters for Event 6 (6 words)
01A0 00A8 – 01A0 00BF	–	Parameters for Event 7 (6 words)
01A0 00C0 – 01A0 00D7	–	Parameters for Event 8 (6 words)
01A0 00D8 – 01A0 00EF	–	Parameters for Event 9 (6 words)
01A0 00F0 – 01A0 00107	–	Parameters for Event 10 (6 words)
01A0 0108 – 01A0 011F	–	Parameters for Event 11 (6 words)
01A0 0120 – 01A0 0137	–	Parameters for Event 12 (6 words)
01A0 0138 – 01A0 014F	–	Parameters for Event 13 (6 words)
01A0 0150 – 01A0 0167	–	Parameters for Event 14 (6 words)
01A0 0168 – 01A0 017F	–	Parameters for Event 15 (6 words)
01A0 0180 – 01A0 0197	–	Reload/link parameters for Event M (6 words)
01A0 0198 – 01A0 01AF	–	Reload/link parameters for Event N (6 words)
...		...
01A0 07E0 – 01A0 07F7	–	Reload/link parameters for Event Z (6 words)
01A0 07F8 – 01A0 07FF	–	Scratch pad area (2 words)

† The C6211/C6211B device has sixty-nine parameter sets [six (6) words each] that can be used to reload/link EDMA transfers.

peripheral register descriptions (continued)

Table 7. EDMA Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01A0 0800 – 01A0 FEFC	–	Reserved
01A0 FF00	ESEL0	EDMA event selector 0
01A0 FF04	ESEL1	EDMA event selector 1
01A0 FF08	–	Reserved
01A0 FF0C	ESEL3	EDMA event selector 3
01A0 FF1F – 01A0 FFDC	–	Reserved
01A0 FFE0	PQSR	Priority queue status register
01A0 FFE4	CIPR	Channel interrupt pending register
01A0 FFE8	CIER	Channel interrupt enable register
01A0 FFEC	CCER	Channel chain enable register
01A0 FFF0	ER	Event register
01A0 FFF4	EER	Event enable register
01A0 FFF8	ECR	Event clear register
01A0 FFFC	ESR	Event set register
01A1 0000 – 01A3 FFFF	–	Reserved

Table 8. Quick DMA (QDMA) and Pseudo Registers†

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0200 0000	QOPT	QDMA options parameter register
0200 0004	QSRC	QDMA source address register
0200 0008	QCNT	QDMA frame count register
0200 000C	QDST	QDMA destination address register
0200 0010	QIDX	QDMA index register
0200 0014 – 0200 001C	–	Reserved
0200 0020	QSOPT	QDMA pseudo options register
0200 0024	QSSRC	QDMA pseudo source address register
0200 0028	QSCNT	QDMA pseudo frame count register
0200 002C	QSDST	QDMA pseudo destination address register
0200 0030	QSIDX	QDMA pseudo index register

† All the QDMA and Pseudo registers are write-accessible only

Table 9. PLL Wrapper Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01B7 C000 – 01B7 C0FF	–	Reserved
01B7 C100	PLLCSR	PLL control/status register
01B7 C104 – 01B7 C10F	–	Reserved
01B7 C110	PLLM	PLL multiplier control register
01B7 C114	PLLDIV0	PLL wrapper divider 0 register
01B7 C118	PLLDIV1	PLL wrapper divider 1 register
01B7 C11C	PLLDIV2	PLL wrapper divider 2 register
01B7 C120	PLLDIV3	PLL wrapper divider 3 register
01B7 C124	OSCDIV1	Oscillator divider 1 register
01B7 C128 – 01B7 DFFF	–	Reserved

peripheral register descriptions (continued)

Table 10. McASP0 and McASP1 Registers

HEX ADDRESS RANGE		ACRONYM	REGISTER NAME
McASP0	McASP1		
01B4 C000	01B5 0000	–	Reserved
01B4 C004	01B5 0004	PWRDEMU	Power down and emulation management register
01B4 C008	01B5 0008	–	Reserved
01B4 C00C	01B5 000C	–	Reserved
01B4 C010	01B5 0010	PFUNC	Pin function register
01B4 C014	01B5 0014	PDIR	Pin direction register
01B4 C018	01B5 0018	PDOUT	Pin data out register
01B4 C01C	01B5 001C	PDIN/PDSET	Pin data in / data set register Read returns: PDIN Writes affect: PDSET
01B4 C020	01B5 0020	PDCLR	Pin data clear register
01B4 C024 – 01B4 C040	01B5 0024 – 01B5 0040	–	Reserved
01B4 C044	01B5 0044	GBLCTL	Global control register
01B4 C048	01B5 0048	AMUTE	Mute control register
01B4 C04C	01B5 004C	DLBCTL	Digital Loop-back control register
01B4 C050	01B5 0050	DITCTL	DIT mode control register
01B4 C054 – 01B4 C05C	01B5 0054 – 01B5 005C	–	Reserved
01B4 C060	01B5 0060	RGBLCTL	Alias of GBLCTL containing only Receiver Reset bits, allows transmit to be reset independently from receive.
01B4 C064	01B5 0064	RMASK	Receiver format unit bit mask register
01B4 C068	01B5 0068	RFMT	Receive bit stream format register
01B4 C06C	01B5 006C	AFSRCTL	Receive frame sync control register
01B4 C070	01B5 0070	ACLKRCTL	Receive clock control register
01B4 C074	01B5 0074	AHCLKRCTL	High-frequency receive clock control register
01B4 C078	01B5 0078	RTDM	Receive TDM slot 0–31 register
01B4 C07C	01B5 007C	RINTCTL	Receiver interrupt control register
01B4 C080	01B5 0080	RSTAT	Status register – Receiver
01B4 C084	01B5 0084	RSLOT	Current receive TDM slot register
01B4 C088	01B5 0088	RCLKCHK	Receiver clock check control register
01B4 C08C – 01B4 C09C	01B5 008C – 01B5 009C	–	Reserved
01B4 C0A0	01B5 00A0	XGBLCT	Alias of GBLCTL containing only Transmitter Reset bits, allows transmit to be reset independently from receive.
01B4 C0A4	01B5 00A4	XMASK	Transmit format unit bit mask register
01B4 C0A8	01B5 00A8	XFMT	Transmit bit stream format register
01B4 C0AC	01B5 00AC	AFSXCTL	Transmit frame sync control register
01B4 C0B0	01B5 00B0	ACLKXCTL	Transmit clock control register
01B4 C0B4	01B5 00B4	AHCLKXCTL	High-frequency Transmit clock control register
01B4 C0B8	01B5 00B8	XTDM	Transmit TDM slot 0–31 register
01B4 C0BC	01B5 00BC	XINTCTL	Transmit interrupt control register
01B4 C0C0	01B5 00C0	XSTAT	Status register – Transmitter
01B4 C0C4	01B5 00C4	XSLOT	Current transmit TDM slot

peripheral register descriptions (continued)

Table 10. McASP0 and McASP1 Registers (Continued)

HEX ADDRESS RANGE		ACRONYM	REGISTER NAME
McASP0	McASP1		
01B4 C0C8	01B5 00C8	XCLKCHK	Transmit clock check control register
01B4 C0CC – 01B4 C0FC	01B5 00CC – 01B5 00FC	–	Reserved
01B4 C100	01B5 0100	DITCSRA0	Left (even TDM slot) channel status register file
01B4 C104	01B5 0104	DITCSRA1	Left (even TDM slot) channel status register file
01B4 C108	01B5 0108	DITCSRA2	Left (even TDM slot) channel status register file
01B4 C10C	01B5 010C	DITCSRA3	Left (even TDM slot) channel status register file
01B4 C110	01B5 0110	DITCSRA4	Left (even TDM slot) channel status register file
01B4 C114	01B5 0114	DITCSRA5	Left (even TDM slot) channel status register file
01B4 C118	01B5 0118	DITCSRB0	Right (odd TDM slot) channel status register file
01B4 C11C	01B5 011C	DITCSRB1	Right (odd TDM slot) channel status register file
01B4 C120	01B5 0120	DITCSRB2	Right (odd TDM slot) channel status register file
01B4 C124	01B5 0124	DITCSRB3	Right (odd TDM slot) channel status register file
01B4 C128	01B5 0128	DITCSRB4	Right (odd TDM slot) channel status register file
01B4 C12C	01B5 012C	DITCSRB5	Right (odd TDM slot) channel status register file
01B4 C130	01B5 0130	DITUDRA0	Left (even TDM slot) user data register file
01B4 C134	01B5 0134	DITUDRA1	Left (even TDM slot) user data register file
01B4 C138	01B5 0138	DITUDRA2	Left (even TDM slot) user data register file
01B4 C13C	01B5 013C	DITUDRA3	Left (even TDM slot) user data register file
01B4 C140	01B5 0140	DITUDRA4	Left (even TDM slot) user data register file
01B4 C144	01B5 0144	DITUDRA5	Left (even TDM slot) user data register file
01B4 C148	01B5 0148	DITUDRB0	Right (odd TDM slot) user data register file
01B4 C14C	01B5 014C	DITUDRB1	Right (odd TDM slot) user data register file
01B4 C150	01B5 0150	DITUDRB2	Right (odd TDM slot) user data register file
01B4 C154	01B5 0154	DITUDRB3	Right (odd TDM slot) user data register file
01B4 C158	01B5 0158	DITUDRB4	Right (odd TDM slot) user data register file
01B4 C15C	01B5 015C	DITUDRB5	Right (odd TDM slot) user data register file
01B4 C160 – 01B4 C17C	01B5 0160 – 01B5 017C	–	Reserved
01B4 C180	01B5 0180	SRCTL0	Serializer 0 control register
01B4 C184	01B5 0184	SRCTL1	Serializer 1 control register
01B4 C188	01B5 0188	SRCTL2	Serializer 2 control register
01B4 C18C	01B5 018C	SRCTL3	Serializer 3 control register
01B4 C190	01B5 0190	SRCTL4	Serializer 4 control register
01B4 C194	01B5 0194	SRCTL5	Serializer 5 control register
01B4 C198	01B5 0198	SRCTL6	Serializer 6 control register
01B4 C19C	01B5 019C	SRCTL7	Serializer 7 control register
01B4 C1A0 – 01B4 C1FC	01B5 C1A0 – 01B5 01FC	–	Reserved
01B4 C200	01B5 0200	XBUF0	Transmit Buffer for Serializer 0
01B4 C204	01B5 0204	XBUF1	Transmit Buffer for Serializer 1
01B4 C208	01B5 0208	XBUF2	Transmit Buffer for Serializer 2
01B4 C20C	01B5 020C	XBUF3	Transmit Buffer for Serializer 3
01B4 C210	01B50C210	XBUF4	Transmit Buffer for Serializer 4

peripheral register descriptions (continued)

Table 10. McASP0 and McASP1 Registers (Continued)

HEX ADDRESS RANGE		ACRONYM	REGISTER NAME
McASP0	McASP1		
01B4 C214	01B5 0214	XBUF5	Transmit Buffer for Serializer 5
01B4 C218	01B5 0218	XBUF6	Transmit Buffer for Serializer 6
01B4 C21C	01B5 021C	XBUF7	Transmit Buffer for Serializer 7
01B4 C220 – 01B4 C27C	01B5 C220 – 01B5 027C	–	Reserved
01B4 C280	01B5 0280	RBUF0	Receive Buffer for Serializer 0
01B4 C284	01B5 0284	RBUF1	Receive Buffer for Serializer 1
01B4 C288	01B5 0288	RBUF2	Receive Buffer for Serializer 2
01B4 C28C	01B5 028C	RBUF3	Receive Buffer for Serializer 3
01B4 C290	01B5 0290	RBUF4	Receive Buffer for Serializer 4
01B4 C294	01B5 0294	RBUF5	Receive Buffer for Serializer 5
01B4 C298	01B5 0298	RBUF6	Receive Buffer for Serializer 6
01B4 C29C	01B5 029C	RBUF7	Receive Buffer for Serializer 7
01B4 C2A0 – 01B4 FFFF	01B5 02A0 – 01B5 3FFF	–	Reserved

Table 11. I2C0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01B4 0000	I2COAR0	I2C0 own address register
01B4 0004	I2CIER0	I2C0 interrupt enable register
01B4 0008	I2CSTR0	I2C0 interrupt status register
01B4 000C	I2CCLKL0	I2C0 clock low-time divider register
01B4 0010	I2CCLKH0	I2C0 clock high-time divider register
01B4 0014	I2CCNT0	I2C0 data count register
01B4 0018	I2CDRR0	I2C0 data receive register
01B4 001C	I2CSAR0	I2C0 slave address register
01B4 0020	I2CDXR0	I2C0 data transmit register
01B4 0024	I2CMDR0	I2C0 mode register
01B4 0028	I2CISRC0	I2C0 interrupt source register
01B4 002C	–	Reserved
01B4 0030	I2CPSC0	I2C0 prescaler register
01B4 0034 – 01B4 3FFF	–	Reserved

peripheral register descriptions (continued)

Table 12. I2C1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01B4 4000	I2COAR1	I2C1 own address register
01B4 4004	I2CIER1	I2C1 interrupt enable register
01B4 4008	I2CSTR1	I2C1 interrupt status register
01B4 400C	I2CCLKL1	I2C1 clock low-time divider register
01B4 4010	I2CCLKH1	I2C1 clock high-time divider register
01B4 4014	I2CCNT1	I2C1 data count register
01B4 4018	I2CDRR1	I2C1 data receive register
01B4 401C	I2CSAR1	I2C1 slave address register
01B4 4020	I2CDXR1	I2C1 data transmit register
01B4 4024	I2CMDR1	I2C1 mode register
01B4 4028	I2CISRC1	I2C1 interrupt source register
01B4 402C	–	Reserved
01B4 4030	I2CPSC1	I2C1 prescaler register
01B4 4034 – 01B4 7FFF	–	Reserved

Table 13. HPI Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
–	HPID	HPI data register	Host read/write access only
–	HPIA	HPI address register	Host read/write access only
0188 0000	HPIC	HPI control register	Both Host/CPU read/write access
0188 0001 – 018B FFFF	–	Reserved	

Table 14. McBSP 0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
018C 0000	DRR0	McBSP0 data receive register via Peripheral Bus	The CPU and DMA/EDMA controller can only read this register; they cannot write to it.
0x3000 0000 – 0x33FF FFFF	DRR0	McBSP0 data receive register via EDMA Bus	
018C 0004	DXR0	McBSP0 data transmit register via Peripheral Bus	
0x3000 0000 – 0x33FF FFFF	DXR0	McBSP0 data transmit register via EDMA Bus	
018C 0008	SPCR0	McBSP0 serial port control register	
018C 000C	RCR0	McBSP0 receive control register	
018C 0010	XCR0	McBSP0 transmit control register	
018C 0014	SRGR0	McBSP0 sample rate generator register	
018C 0018	MCR0	McBSP0 multichannel control register	
018C 001C	RCER0	McBSP0 receive channel enable register	
018C 0020	XCER0	McBSP0 transmit channel enable register	
018C 0024	PCR0	McBSP0 pin control register	
018C 0028 – 018F FFFF	–	Reserved	

peripheral register descriptions (continued)

Table 15. McBSP 1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0190 0000	DRR1	Data receive register via Peripheral Bus	The CPU and DMA/EDMA controller can only read this register; they cannot write to it.
0x3400 0000 – 0x37FF FFFF	DRR1	McBSP1 data receive register via EDMA Bus	
0190 0004	DXR1	McBSP1 data transmit register via Peripheral Bus	
0x3400 0000 – 0x37FF FFFF	DXR1	McBSP1 data transmit register via EDMA Bus	
0190 0008	SPCR1	McBSP1 serial port control register	
0190 000C	RCR1	McBSP1 receive control register	
0190 0010	XCR1	McBSP1 transmit control register	
0190 0014	SRGR1	McBSP1 sample rate generator register	
0190 0018	MCR1	McBSP1 multichannel control register	
0190 001C	RCER1	McBSP1 receive channel enable register	
0190 0020	XCER1	McBSP1 transmit channel enable register	
0190 0024	PCR1	McBSP1 pin control register	
0190 0028 – 0193 FFFF	–	Reserved	

Table 16. Timer 0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0194 0000	CTL0	Timer 0 control register	Determines the operating mode of the timer, monitors the timer status, and controls the function of the TOUT pin.
0194 0004	PRD0	Timer 0 period register	Contains the number of timer input clock cycles to count. This number controls the TSTAT signal frequency.
0194 0008	CNT0	Timer 0 counter register	Contains the current value of the incrementing counter.
0194 000C – 0197 FFFF	–	Reserved	

Table 17. Timer 1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0198 0000	CTL1	Timer 1 control register	Determines the operating mode of the timer, monitors the timer status, and controls the function of the TOUT pin.
0198 0004	PRD1	Timer 1 period register	Contains the number of timer input clock cycles to count. This number controls the TSTAT signal frequency.
0198 0008	CNT1	Timer 1 counter register	Contains the current value of the incrementing counter.
0198 000C – 019B FFFF	–	Reserved	

peripheral register descriptions (continued)

Table 18. GPIO Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01B0 0000	GPEN	GPIO enable register
01B0 0004	GPDIR	GPIO direction register
01B0 0008	GPVAL	GPIO value register
01B0 000C	–	Reserved
01B0 0010	GPDH	GPIO delta high register
01B0 0014	GPHM	GPIO high mask register
01B0 0018	GPDL	GPIO delta low register
01B0 001C	GPLM	GPIO low mask register
01B0 0020	GPGC	GPIO global control register
01B0 0024	GPPOL	GPIO interrupt polarity register
01B0 0028 – 01B0 3FFF	–	Reserved

PWRD bits in CPU CSR register description

Table 19 identifies the PWRD field (bits 15–10) in the CPU CSR register. These bits control the device power-down modes. For more detailed information on the PWRD bit field of the CPU CSR register, see the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190).

Table 19. PWRD field bits in the CPU CSR Register

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
–	CSR	Control status register	The PWRD field (bits 15–10 in the CPU CSR) controls the device power-down modes. Accessible by writing a value to the CSR register.

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interrupts and interrupt selector

The C67x DSP core supports 16 prioritized interrupts, which are listed in Table 20. The highest priority interrupt is INT_00 (dedicated to RESET) while the lowest priority is INT_15. The first four interrupts are non-maskable and fixed. The remaining interrupts (4–15) are maskable and default to the interrupt source listed in Table 20. However, their interrupt source may be reprogrammed to any one of the sources listed in Table 21 (Interrupt Selector). Table 21 lists the selector value corresponding to each of the alternate interrupt sources. The selector choice for interrupts 4–15 is made by programming the corresponding fields (listed in Table 20) in the MUXH (address 0x019C0000) and MUXL (address 0x019C0004) registers.

Table 20. DSP Interrupts

DSP INTERRUPT NUMBER	INTERRUPT SELECTOR CONTROL REGISTER	DEFAULT SELECTOR VALUE (BINARY)	DEFAULT INTERRUPT EVENT
INT_00	–	–	RESET
INT_01	–	–	NMI
INT_02	–	–	Reserved
INT_03	–	–	Reserved
INT_04	MUXL[4:0]	00100	EXTINT4
INT_05	MUXL[9:5]	00101	EXTINT5
INT_06	MUXL[14:10]	00110	EXTINT6
INT_07	MUXL[20:16]	00111	EXTINT7
INT_08	MUXL[25:21]	01000	EDMAINT
INT_09	MUXL[30:26]	01001	EMUDTDMA
INT_10	MUXH[4:0]	00011	SDINT
INT_11	MUXH[9:5]	01010	EMURTDXRX
INT_12	MUXH[14:10]	01011	EMURTDXTX
INT_13	MUXH[20:16]	00000	DSPINT
INT_14	MUXH[25:21]	00001	TINT0
INT_15	MUXH[30:26]	00010	TINT1

Table 21. Interrupt Selector

INTERRUPT SELECTOR VALUE (BINARY)	INTERRUPT EVENT	MODULE
00000	DSPINT	HPI
00001	TINT0	Timer 0
00010	TINT1	Timer 1
00011	SDINT	EMIF
00100	EXTINT4	GPIO
00101	EXTINT5	GPIO
00110	EXTINT6	GPIO
00111	EXTINT7	GPIO
01000	EDMAINT	EDMA
01001	EMUDTDMA	Emulation
01010	EMURTDXRX	Emulation
01011	EMURTDXTX	Emulation
01100	XINT0	McBSP0
01101	RINT0	McBSP0
01110	XINT1	McBSP1
01111	RINT1	McBSP1
10000	GPINT0	GPIO
10001	Reserved	–
10010	Reserved	–
10011	Reserved	–
10100	Reserved	–
10101	Reserved	–
10110	I2CINT0	I2C0
10111	I2CINT1	I2C1
11000	Reserved	–
11001	Reserved	–
11010	Reserved	–
11011	Reserved	–
11100	AXINT0	McASP0
11101	ARINT0	McASP0
11110	AXINT1	McASP1
11111	ARINT1	McASP1

EDMA module and EDMA selector

The C67x EDMA supports up to 16 EDMA channels. Four of the sixteen channels (channels 8–11) are reserved for EDMA chaining, leaving 12 EDMA channels available to service peripheral devices.

The EDMA selector registers that control the EDMA channels servicing peripheral devices are located at addresses 0x01A0FF00 (ESEL0), 0x01A0FF04 (ESEL1), and 0x01A0FF0C (ESEL3). These EDMA selector registers control the mapping of the EDMA events to the EDMA channels. Each EDMA event has an assigned EDMA selector code (see Table 23). By loading each EVTSELx register field with an EDMA selector code, users can map any desired EDMA event to any specified EDMA channel. Table 22 lists the default EDMA selector value for each EDMA channel.

See Table 24 and Table 25 for the EDMA Event Selector registers and their assoicated bit descriptions.

EDMA module and EDMA selector (continued)

Table 22. EDMA Channels

EDMA CHANNEL	EDMA SELECTOR CONTROL REGISTER	DEFAULT SELECTOR VALUE (BINARY)	DEFAULT EDMA EVENT
0	ESEL0[5:0]	000000	DSPINT
1	ESEL0[13:8]	000001	TINT0
2	ESEL0[21:16]	000010	TINT1
3	ESEL0[29:24]	000011	SDINT
4	ESEL1[5:0]	000100	EXTINT4
5	ESEL1[13:8]	000101	EXTINT5
6	ESEL1[21:16]	000110	EXTINT6
7	ESEL1[29:24]	000111	EXTINT7
8	n/a	n/a	TCC8 (Chaining)
9	n/a	n/a	TCC9 (Chaining)
10	n/a	n/a	TCC10 (Chaining)
11	n/a	n/a	TCC11 (Chaining)
12	ESEL3[5:0]	001000	XEVT0
13	ESEL3[13:8]	001001	REVT0
14	ESEL3[21:16]	001010	XEVT1
15	ESEL3[29:24]	001011	REVT1

Table 23. EDMA Selector

EDMA SELECTOR CODE (BINARY)	EDMA EVENT	MODULE
000000	DSPINT	HPI
000001	TINT0	TIMER0
000010	TINT1	TIMER1
000011	SDINT	EMIF
000100	EXTINT4	GPIO
000101	EXTINT5	GPIO
000110	EXTINT6	GPIO
000111	EXTINT7	GPIO
001000	GPINT0	GPIO
001001	GPINT1	GPIO
001010	GPINT2	GPIO
001011	GPINT3	GPIO
001100	XEVT0	McBSP0
001101	REVT0	McBSP0
001110	XEVT1	McBSP1
001111	REVT1	McBSP1
010000–011111	Reserved	
100000	AXEVTE0	McASP0
100001	AXEVTO0	McASP0
100010	AXEVT0	McASP0
100011	AREVTE0	McASP0
100100	AREVTO0	McASP0
100101	AREVT0	McASP0
100110	AXEVTE1	McASP1
100111	AXEVTO1	McASP1
101000	AXEVT1	McASP1
101001	AREVTE1	McASP1
101010	AREVTO1	McASP1
101011	AREVT1	McASP1
101100	I2CREVT0	I2C0
101101	I2CXEVT0	I2C0
101110	I2CREVT1	I2C1
101111	I2CXEVT1	I2C1
110000	GPINT8	GPIO
110001	GPINT9	GPIO
110010	GPINT10	GPIO
110011	GPINT11	GPIO
110100	GPINT12	GPIO
110101	GPINT13	GPIO
110110	GPINT14	GPIO
110111	GPINT15	GPIO
111000–111111	Reserved	

EDMA module and EDMA selector (continued)

Table 24. EDMA Event Selector Registers (ESEL0, ESEL1, and ESEL3)

ESEL0 Register (0x01A0 FF00)

31–30	29–28	27–24	23–22	21–20	19–16
Reserved	EVTSEL3		Reserved	EVTSEL2	
R–0	R/W–00 0011b		R–0	R/W–00 0010b	

15–14	13–12	11–8	7–6	5–4	3–0
Reserved	EVTSEL1		Reserved	EVTSEL0	
R–0	R/W–00 0001b		R–0	R/W–00 0000b	

Legend: R = Read only, R/W = Read/Write; -n = value after reset

ESEL1 Register (0x01A0 FF04)

31–30	29–28	27–24	23–22	21–20	19–16
Reserved	EVTSEL7		Reserved	EVTSEL6	
R–0	R/W–00 0111b		R–0	R/W–00 0110b	

15–14	13–12	11–8	7–6	5–4	3–0
Reserved	EVTSEL5		Reserved	EVTSEL4	
R–0	R/W–00 0101b		R–0	R/W–00 0100b	

Legend: R = Read only, R/W = Read/Write; -n = value after reset

ESEL3 Register (0x01A0 FF0C)

31–30	29–28	27–24	23–22	21–20	19–16
Reserved	EVTSEL15		Reserved	EVTSEL14	
R–0	R/W–00 1011b		R–0	R/W–00 1010b	

15–14	13–12	11–8	7–6	5–4	3–0
Reserved	EVTSEL13		Reserved	EVTSEL12	
R–0	R/W–00 1001b		R–0	R/W–00 1000b	

Legend: R = Read only, R/W = Read/Write; -n = value after reset

Table 25. EDMA Event Selection Registers (ESEL0, ESEL1, and ESEL3) Description

BIT #	NAME	DESCRIPTION
31:30 23:22 15:14 7:6	Reserved	Reserved. Read-only, writes have no effect.
29:24 21:16 13:8 5:0	EVTSELx	EDMA event selection bits for channel x. Allows mapping of the EDMA events to the EDMA channels. The EVTSEL0 through EVTSEL15 bits correspond to the channels 0 to 15, respectively. These EVTSELx fileds are user–selectable. By configuring the EVTSELx fields to the EDMA selector value of the desired EDMA sync event number (see Table 23), users can map any EDMA event to the EDMA channel. For example, if EVTSEL15 is programmed to 00 0001b (the EDMA selector code for TINT0), then channel 15 is triggered by Timer0 TINT0 events.

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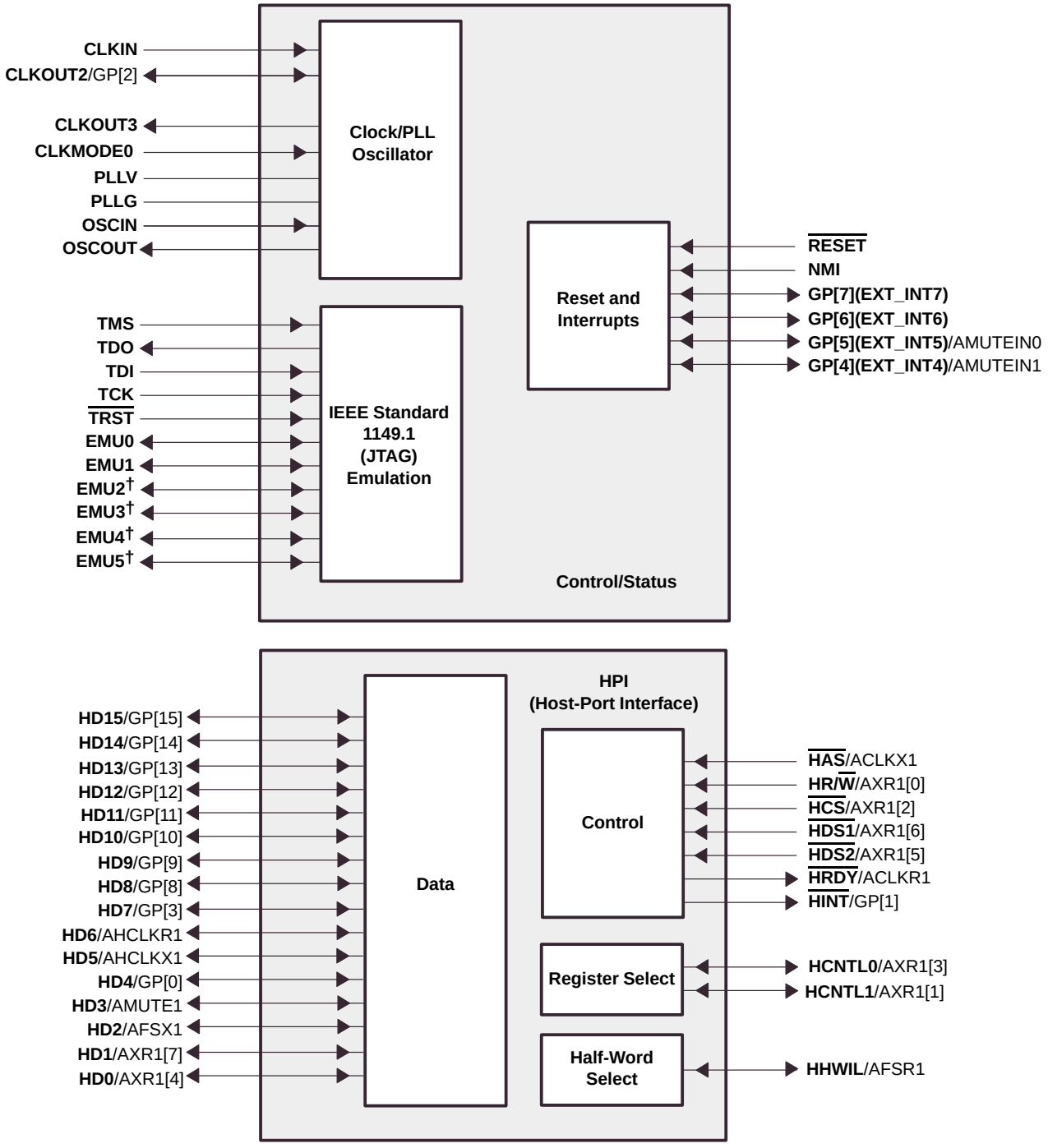
signal groups description

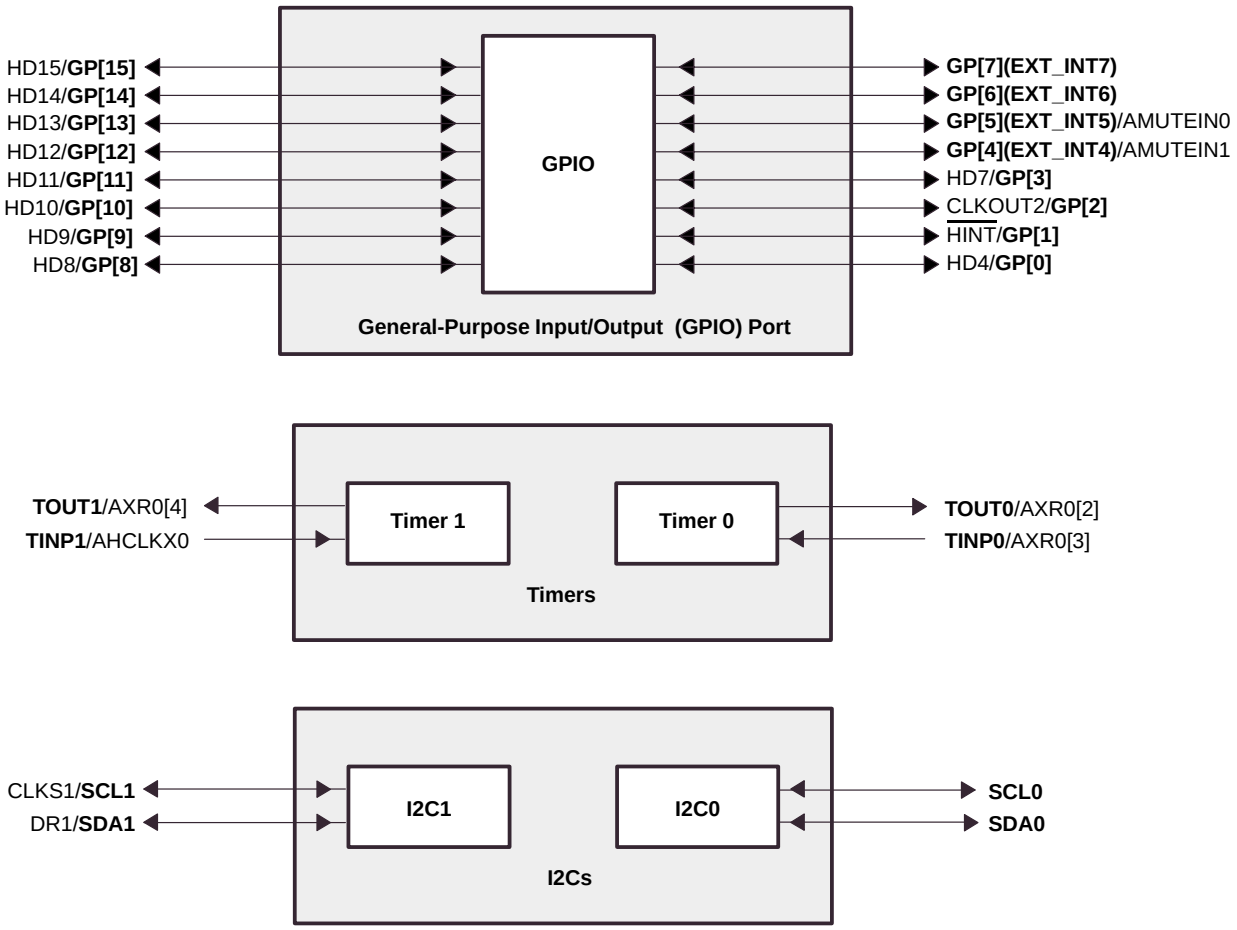


†These external pins are applicable to the GFN package only.

NOTE A: On multiplexed pins, bolded text denotes the active function of the pin for that particular peripheral module.

Figure 3. CPU (DSP Core) and Peripheral Signals

signal groups description (continued)



NOTE A: On multiplexed pins, bolded text denotes the active function of the pin for that particular peripheral module.

Figure 4. Peripheral Signals

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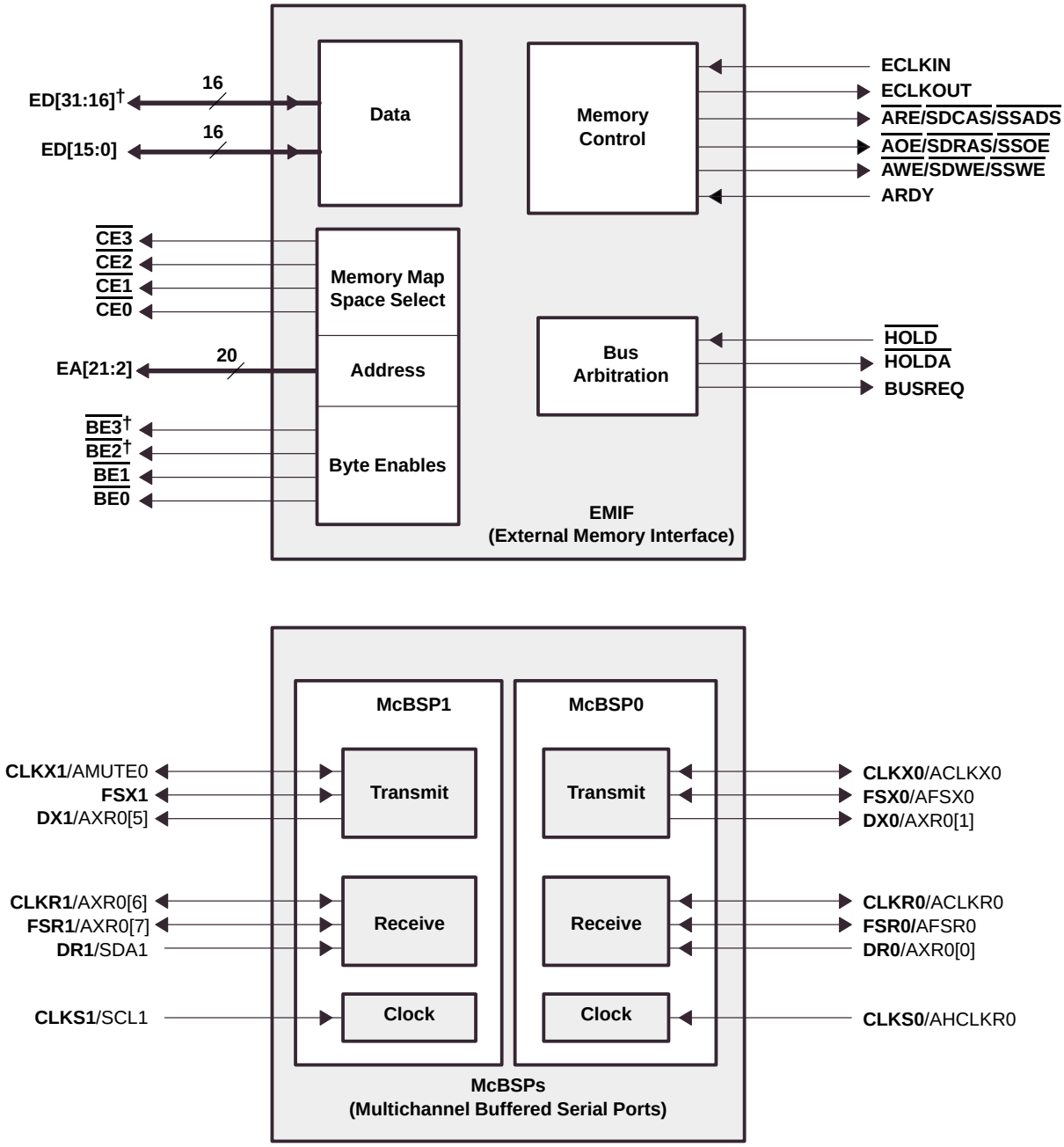
signal groups description (continued)

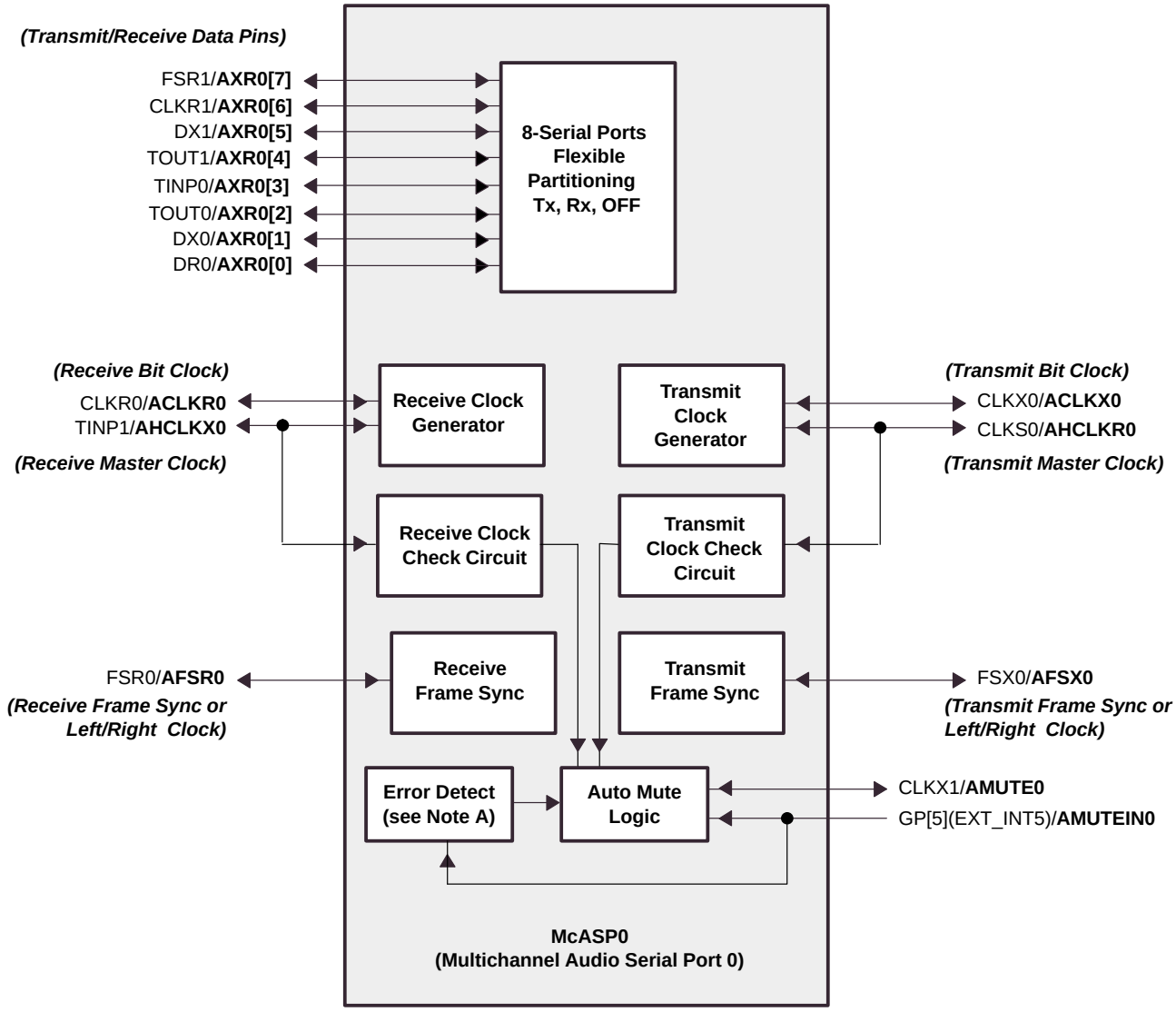


†These external pins are applicable to the GFN package only.

NOTE A: On multiplexed pins, bolded text denotes the active function of the pin for that particular peripheral module.

Figure 4. Peripheral Signals (Continued)

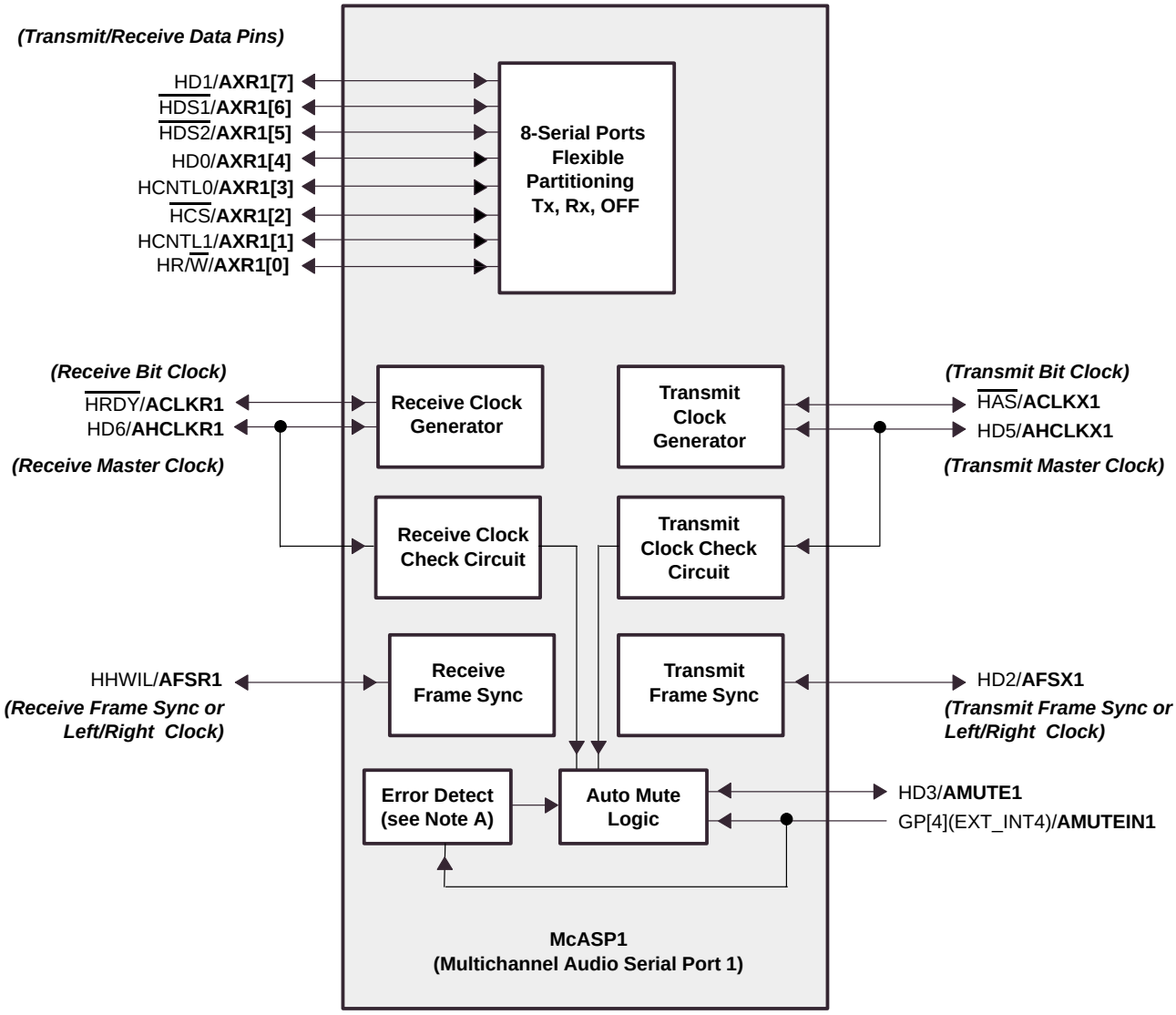
signal groups description (continued)



NOTES: A. The McASPs' Error Detect function detects underruns, overruns, early/late frame syncs, DMA errors, and external mute input.
B. On multiplexed pins, bolded text denotes the active function of the pin for that particular peripheral module.
C. Bolded and italicized text within parentheses denotes the function of the pins in an audio system.

Figure 4. Peripheral Signals (Continued)

signal groups description (continued)



NOTES: A. The McASPs' Error Detect function detects underruns, overruns, early/late frame syncs, DMA errors, and external mute input.
B. On multiplexed pins, bolded text denotes the active function of the pin for that particular peripheral module.
C. Bolded and italicized text within parentheses denotes the function of the pins in an audio system.

Figure 4. Peripheral Signals (Continued)

DEVICE CONFIGURATIONS

On the C6713 device, bootmode and certain device configurations/peripheral selections are determined at device reset, while other device configurations/peripheral selections are software-configurable via the device configurations register (DEVCFG) [address location 0x019C0200] after device reset.

device configurations at device reset

Table 26 describes the C6713 device configuration pins, which are set up via external pullup/pulldown resistors through the HPI data pins (HD[4:3], HD8, and HD12) and CLKMODE0 pin. For more details on these device configuration pins, see the Terminal Functions table and the Debugging Considerations section.

Table 26. Device Configurations Pins at Device Reset (HD[4:3], HD8, HD12, and CLKMODE0)†

CONFIGURATION PIN	PYP	GFN	FUNCTIONAL DESCRIPTION
HD8		B17	Device Endian mode (LEND) 0 – System operates in Big Endian mode 1 – System operates in Little Endian mode (default)
HD[4:3] (BOOTMODE)		A15, C19, C20	Bootmode Configuration Pins (BOOTMODE) 00 – $\overline{CE1}$ width 32-bit, HPI boot 01 – $\overline{CE1}$ width 8-bit, Asynchronous external ROM boot with default timings (default mode) 10 – $\overline{CE1}$ width 16-bit, Asynchronous external ROM boot 11 – $\overline{CE1}$ width 32-bit, Asynchronous external ROM boot
HD12		C15	Pulldown. **For proper device operation, this pin must be externally pulled down with a 1-kΩ resistor.**
CLKMODE0		C4	Clock generator input clock source select 0 – Oscillator pads (OSCIN, OSCOUT directly from the crystal oscillator) 1 – CLKIN square wave [default] **This pin *must* be pulled to the correct level even after reset.**

† Other HD pins (HD [15, 13, 11:9, 7:5, 2:0] have pullups/pulldowns (IPUs/IPDs). For proper device operation, ***do not*** oppose these pins with external IPUs/IPDs at reset.

PRODUCT PREVIEW

DEVICE CONFIGURATIONS (CONTINUED)

peripheral selection at device reset

Some C6713 peripherals share the same pins but are mutually exclusive (i.e., HPI, general-purpose input/output 0 pins GP[15:8, 3, 1, 0], McASP0, and I2C0).

- HPI versus McASP1, I2C0, and GP peripherals

  The HPI_EN (HD14 pin) is latched at reset. This pin selects whether the HPI peripheral or McASP1, I2C0 peripherals, and GP[15:8, 3, 1, 0] pins are functionally enabled (see Table 27).

Table 27. HPI_EN (HD14 Pin) Peripheral Selection (HPI or McASP1, I2C0, and Select GP Pins)

PERIPHERAL SELECTION	PERIPHERALS SELECTED		DESCRIPTION
HPI_EN (HD14 Pin)	HPI	McASP1, I2C0, and GP [15:8,3,1,0]	
0		√	HPI_EN = 0 HPI is disabled; McASP1 and I2C0 peripherals and GP [15:8, 3, 1,0] pins are enabled. All multiplexed HPI/McASP1 and HPI/GP pins function as McASP1 and GP pins, respectively. To use the GP pins, the appropriate bits in the GPEN and GPDIR registers need to be configured. The IPUs on the I2C0 pins are disabled, allowing for I2C0 use. When the I2C0 peripheral is not used, to avoid floating inputs, these I2C0 pins must be externally pulled up with 1-kΩ resistor.
1	√		HPI_EN = 1 HPI is enabled; McASP1 and I2C0 peripherals and GP [15:8, 3, 1,0] pins are disabled [default]. All multiplexed HPI/McASP1 and HPI/GP pins function as HPI pins. In addition, since the I2C0 peripheral is disabled, the IPUs on the I2C0 pins are enabled to avoid floating inputs.

DEVICE CONFIGURATIONS (CONTINUED)

peripheral selection/device configurations via the DEVCFG control register

The device configuration register (DEVCFG) allows the user to control the peripheral selection of the McBSP0, McBSP1, McASP0, and I2C1 peripherals. The DEVCFG register also offers the user control of the EMIF input clock source and the timer output functions of the TOUT1/AXR0[4] and TOUT0/AXR0[2] multiplexed pins. For more detailed information on the DEVCFG register control bits, see Table 28 and Table 29.

Table 28. Device Configuration Register (DEVCFG) [Address location: 0x019C0200]

31							16
Reserved†							
RW-0							
15		5	4	3	2	1	0
Reserved†			EKSRC	TOUT1SEL	TOUT0SEL	McASP0EN	I2C1EN
RW-0			R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R/W = Read/Write; -n = value after reset

† ***Do not*** write non-zero values to these bit locations.

Table 29. Device Configuration (DEVCFG) Register Selection Bit Descriptions

BIT #	NAME	DESCRIPTION
31:5	Reserved	Reserved. ***Do not*** write non-zero values to these bit locations.
4	EKSRC	EMIF input clock source bit. Determines which clock signal is used as the EMIF input clock. 0 = SYSCLK3 (from the clock generator) is the EMIF input clock source (default) 1 = ECLKIN external pin is the EMIF input clock source
3	TOUT1SEL	Timer 1 output (TOUT1) pin function select bit. Selects the pin function of the TOUT1/AXR0[4] external pin independent of the rest of the peripheral selection bits in the DEVCFG register. 0 = The pin functions as a Timer 1 output (TOUT1) pin (default) 1 = The pin functions as the McASP0 AXR0[4] pin.
2	TOUT0SEL	Timer 0 output (TOUT0) pin function select bit. Selects the pin function of the TOUT0/AXR0[2] external pin independent of the rest of the peripheral selection bits in the DEVCFG register. 0 = The pin functions as a Timer 0 output (TOUT0) pin (default) 1 = The pin functions as the McASP0 AXR0[2] pin.
1	MCASP0EN	Multichannel Audio Serial Port 0 (McASP0) enable bit. Selects whether McASP0 or the McBSP0 peripheral is enabled. 0 = McASP0 is disabled (functional for DIT mode only), McBSP0 is enabled (default). 1 = McASP0 is enabled, McBSP0 is disabled.
0	I2C1EN	Inter-integrated circuit 1 (I2C1) enable bit. Selects whether I2C1 or the McBSP1 peripheral is enabled. 0 = I2C1 is disabled, McBSP1 is enabled (default) The internal IPU/IPDs on the CLKS1/SCL1 and DR1/SDA1 pins are enabled for McBSP1's use. 1 = I2C1 is enabled, McBSP1 is disabled The internal IPU/IPDs on the CLKS1/SCL1 and DR1/SDA1 pins are disabled for I2C1's use

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DEVICE CONFIGURATIONS (CONTINUED)

multiplexed pins

Multiplexed pins are pins that are shared by more than one peripheral and are internally multiplexed. Most of these pins are configured by software via the device configuration register (DEVCFG), and the others (specifically, the HPI pins) are configured by an external pullup/pulldown resistor on the HD14 pin (HPI_EN) at reset. The muxed pins that are configured by software are intended to be programmed once during software initialization. The muxed pins that are configured by external pullup/pulldown resistors are mutually exclusive; only one peripheral has primary control of the function of these pins after reset. Table 30 summarizes the peripheral pins affected by the HPI_EN (HD14 pin) and DEVCFG register. Table 31 identifies the multiplexed pins on the C6713 device; shows the default (primary) function and the default settings after reset; and describes the pins, registers, etc. necessary to configure the specific multiplexed functions.

DEVICE CONFIGURATIONS (CONTINUED)

Table 30. Peripheral Pin Selection Matrix†

SELECTION BITS		PERIPHERAL PINS AVAILABILITY										
BIT NAME	BIT VALUE	McASP0‡	McASP1	I2C0	I2C1	McBSP0	McBSP1	TIMER0	TIMER1	HPI	GPIO PINS	EMIF
HPI_EN (boot config pin)	0		AHCLKX1 AHCLKR1 ACLKX1 ACLKR1 AFSX1 AFSR1 AMUTE1 AXR1[0] to AXR1[7]	All						None	GP[0:1], GP[3], GP[8:15] Plus: GP2 ctrl'd by GP2EN	
	1		None	None						All	**NO** GP[0:1], GP[3], GP[8:15]	
McASP0EN (DEVCFG bit)	0	None				All						
	1	ACLKK0 ACLKR0 AFSX0 AFSR0 AHCLKR0 AXR0[0] AXR0[1]				None						
IIC1EN (DEVCFG bit)	0	**NO** AMUTE0 AXR0[5] AXR0[6] AXR0[7]			None		All					
	1	AMUTE0 AXR0[5] AXR0[6] AXR0[7]			All		None					
TOUT0SEL (DEVCFG bit)	0	**NO** AXR0[2]						TOUT0				
	1	AXR0[2]						**NO** TOUT0				
TOUT1SEL (DEVCFG bit)	0	**NO** AXR0[4]							TOUT1			
	1	AXR0[4]							**NO** TOUT1			

† Gray blocks indicate that the peripheral is not affected by the selection bit.
‡ The McASP0 pins AXR0[3] and AHCLKX0 are shared with the timer input pins TINP0 and TINP1, respectively. See Table 31 for more detailed information.

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DEVICE CONFIGURATIONS (CONTINUED)

Table 31. C6713 Device Multiplexed/Shared Pins

MULTIPLEXED PINS NAME	PYP	GFN	DEFAULT FUNCTION	DEFAULT SETTING	DESCRIPTION
CLKOUT2/GP[2]		Y12	CLKOUT2	GP2EN = 0 (GPEN reigster bit) GP[2] function disabled, CLKOUT2 enabled	When the CLKOUT2 pin is enabled , the CLK2EN bit in the EMIF global control register (GBLCTL) controls the CLKOUT2 pin. CLK2EN = 0: CLKOUT2 held high CLK2EN = 1: CLKOUT2 enabled to clock To use these as GPIO pins, the GPxEN bits in the GPIO Enable Register and the GPxDIR bits in the GPIO Direction Register must be properly configured. GPxEN = 1: GPx pin enabled GPxDIR = 0: GPx pin is an input GPxDIR = 1: GPx pin is an output To use AMUTEIN0/1 pin function, the GP[5]/GP[4] pins must be configured as an input, and set to 1 the INSTAT bit in the associated McASP AMUTE register.
GP[5](EXT_INT5)/AMUTEIN0		C1	GP[5](EXT_INT5)	No Function GP5EN = 0 (disabled) GP4EN = 0 (disabled) GPxDIR = 0 (input)	
GP[4](EXT_INT4)/AMUTEIN1		C2	GP[4](EXT_INT4)		
CLKS0/AHCLKR0		K3	McBSP0 pin function	MCASP0EN = 0 (DEVCFG register bit) McASP0 pins disabled, McBSP0 pins enabled	To enable the McASP0 peripheral, the McASP0EN bit in the DEVCFG register must be set to 1 (disabling the McBSP0 peripheral pins).
DR0/AXR0[0]		J1			
DX0/AXR0[1]		H2			
FSR0/AFSR0		J3			
FSX0/AFSX0		H1			
CLKR0/ACLKR0		H3			
CLKX0/ACLKX0		G3			
CLKS1/SCL1		E1	McBSP1 pin function	I2C1EN = 0 (DEVCFG register bit) I2C1 disabled, McBSP0 pins enabled	To enable the I2C1 peripheral, the I2C1EN bit in the DEVCFG register must be set to 1, disabling the McBSP1 peripheral pins.
DR1/SDA1		M2			
DX1/AXR0[5]		L2	McBSP1 pin function	I2C1EN = 0 (DEVCFG register bit) I2C1 disabled, McBSP1 pins enabled	To enable the McASP0 peripheral pins the I2C1EN bit in the DEVCFG register must be set to 1.
FSR1/AXR0[7]		M3			
CLKR1/AXR0[6]		M1			
CLKX1/AMUTE0		L3			

DEVICE CONFIGURATIONS (CONTINUED)

Table 31. C6713 Device Multiplexed/Shared Pins

MULTIPLEXED PINS NAME	PYP	GFN	DEFAULT FUNCTION	DEFAULT SETTING	DESCRIPTION
$\overline{\text{HINT}}$/GP[1]		J20	HPI pin function	HPI_EN (HD14 pin) = 1 (HPI enabled) McASP1, I2C0, and eleven GP pins are disabled.	To enable the McASP1 and I2C0 peripherals and the eleven GP pins, an external pulldown resistor (1 kΩ) must be provided on the HD14 pin setting HPI_EN = 0 at reset. To use these as GPIO pins, the GPxEN bits in the GPIO Enable Register and the GPxDIR bits in the GPIO Direction Register must be properly configured. GPxEN = 1: GPx pin enabled GPxDIR = 0: GPx pin is an input GPxDIR = 1: GPx pin is an output
HD15/GP[15]		B14			
HD14/GP[14]		C14			
HD13/GP[13]		A15			
HD12/GP[12]		C15			
HD11/GP[11]		A16			
HD10/GP[10]		B16			
HD9/GP[9]		C16			
HD8/GP[8]		B17			
HD7/GP[3]		A18			
HD4/GP[0]		C19			
HD1/AXR1[7]		D20			
HD0/AXR1[4]		E20			
HCNTL1/AXR1[1]		G19			
HCNTL0/AXR1[3]		G18			
HR/$\overline{\text{W}}$/AXR1[0]		G20			
$\overline{\text{HDS1}}$/AXR1[6]		E9			
$\overline{\text{HDS2}}$/AXR1[5]		F18			
$\overline{\text{HCS}}$/AXR1[2]		F20			
HD6/AHCLKR1		H19			
HD5/AHCLKX1		B18			
HD3/AMUTE1		C20			
HD2/AFSX1		D18			
HHWIL/AFSR1		H20			
$\overline{\text{HRDY}}$/ACLKR1		H19			
$\overline{\text{HAS}}$/ACLKX1		E18			
TINP0/AXR0[3]		G2	Both TINP0 and AXR0[3] input function	AXR3 bit in the McASP0 PDIR register = 0 (input)	By default, this pin functions as TINP0 and AXR0[3] input. Setting the AXR3 bit in the McASP0 PDIR register to a 1 enables AXR0[3] as an output and disables the TINP0 pin function.
TINP1/AHCLKX0		F2	Both TINP1 and AHCLKX0 input function	AHCLKX bit in the McASP0 PDIR register = 0 (input)	By default, this pin functions as TINP1 and AHCLKX0 input. Setting the AHCLKX bit in the McASP0 PDIR register to a 1 enables AHCLKX0 as an output and disables the TINP1 pin function.

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DEVICE CONFIGURATIONS (CONTINUED)

Table 31. C6713 Device Multiplexed/Shared Pins

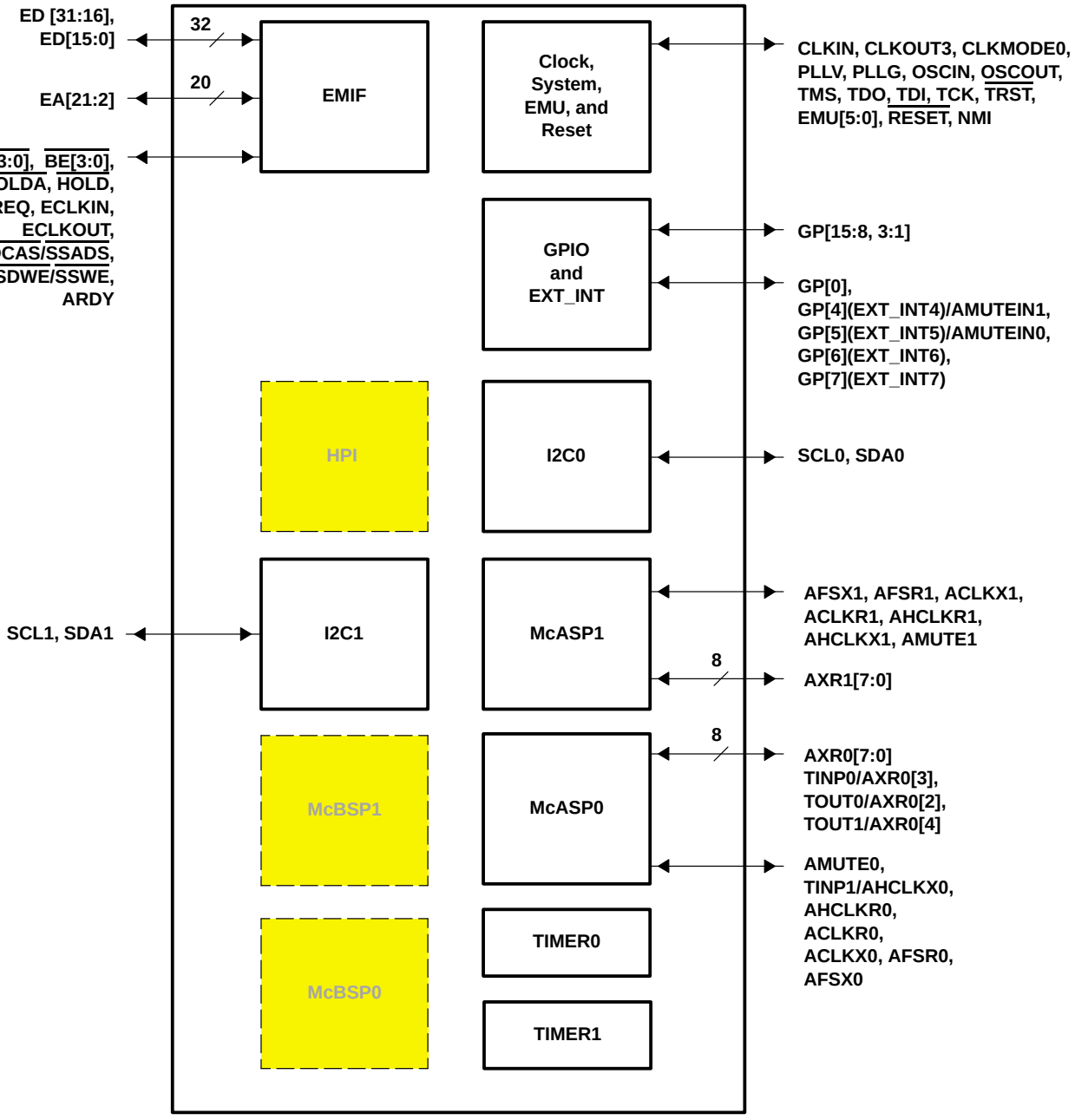
MULTIPLEXED PINS NAME	PYP	GFN	DEFAULT FUNCTION	DEFAULT SETTING	DESCRIPTION
TOUT0/AXR0[2]		G1	Timer 0 output function	TOUT0SEL = 0 (DEVCFG register bit) TOUT0 pin enabled and McASP0 AXR0[2] disabled	To enable the McASP0 AXR0[2] pin, the following must be properly configured: TOUT0SEL = 1 (TOUT0 disabled, AXR0[2] enabled. If the AXR2 bit in the McASP0 PDIR register = 0, then AXR0[2] is an input pin. If the AXR2 bit in the McASP0 PDIR register = 1, then AXR0[2] is an output pin.
TOUT1/AXR0[4]		F1	Timer 1 output function	TOUT1SEL = 0 (DEVCFG register bit) TOUT1 pin enabled and McASP0 AXR0[4] disabled	To enable the McASP0 AXR0[4] pin, the following must be properly configured: TOUT1SEL = 1 (TOUT1 disabled, AXR0[4] enabled. If the AXR4 bit in the McASP0 PDIR register = 0, then AXR0[4] is an input pin. If the AXR4 bit in the McASP0 PDIR register = 1, then AXR0[4] is an output pin.

configuration examples

Figure 5 through Figure 10 illustrate examples of peripheral selections that are configurable on this device.

DEVICE CONFIGURATIONS (CONTINUED)

configuration examples (continued)



Shading denotes a peripheral module not available for this configuration.

DEVCFG Register Value: 0x0000 000F
McASP0EN = 1
I2C1EN = 1
TOUT0SEL = 1
TOUT1SEL = 1
EKSRC = 0

HPI_EN(HD14) = 0
GP2EN BIT = 1 (GPEN Register)

Figure 5. Configuration Example A (2 I2C + 2 McASP)

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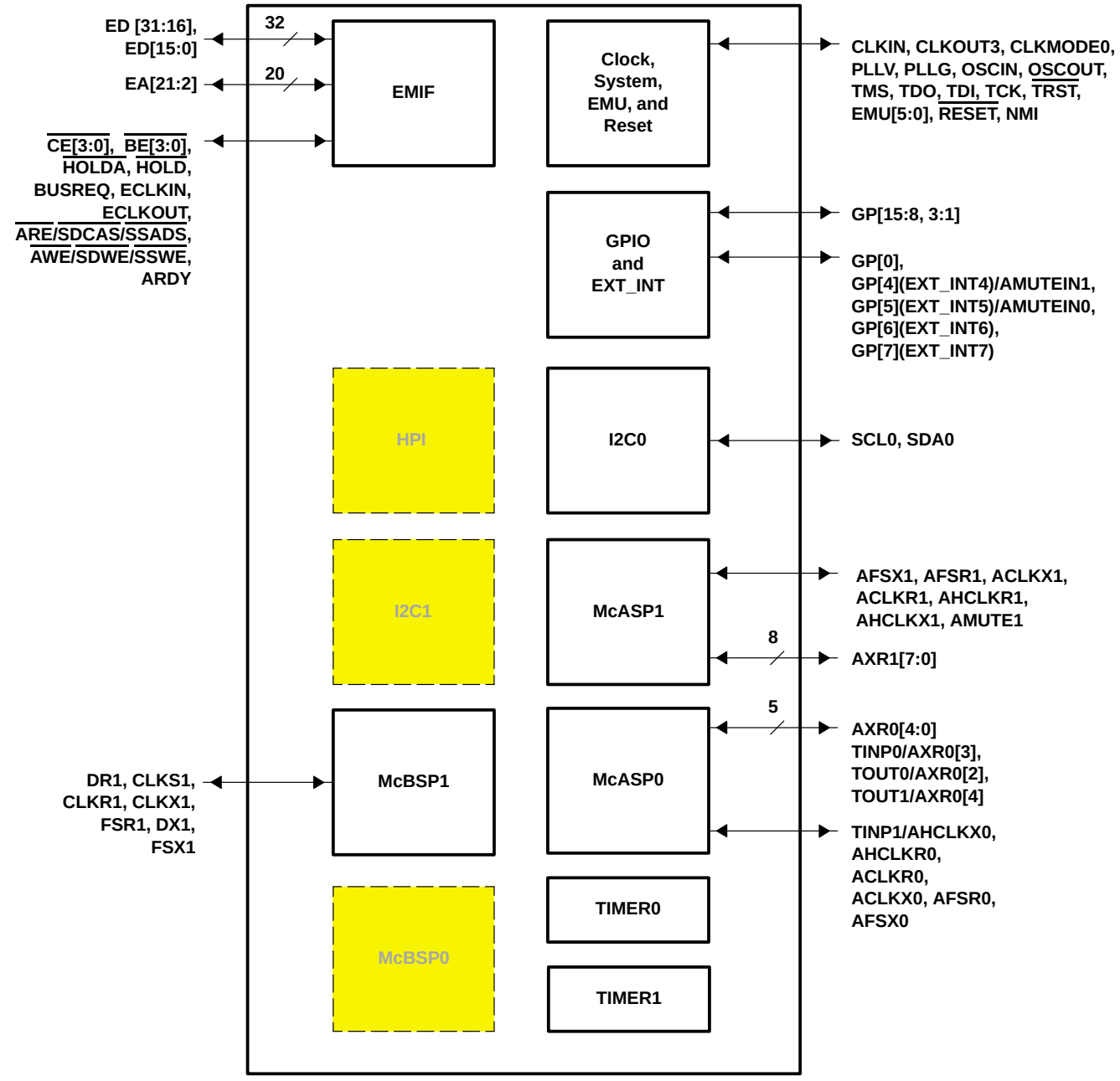
configuration examples (continued)



Shading denotes a peripheral module not available for this configuration.

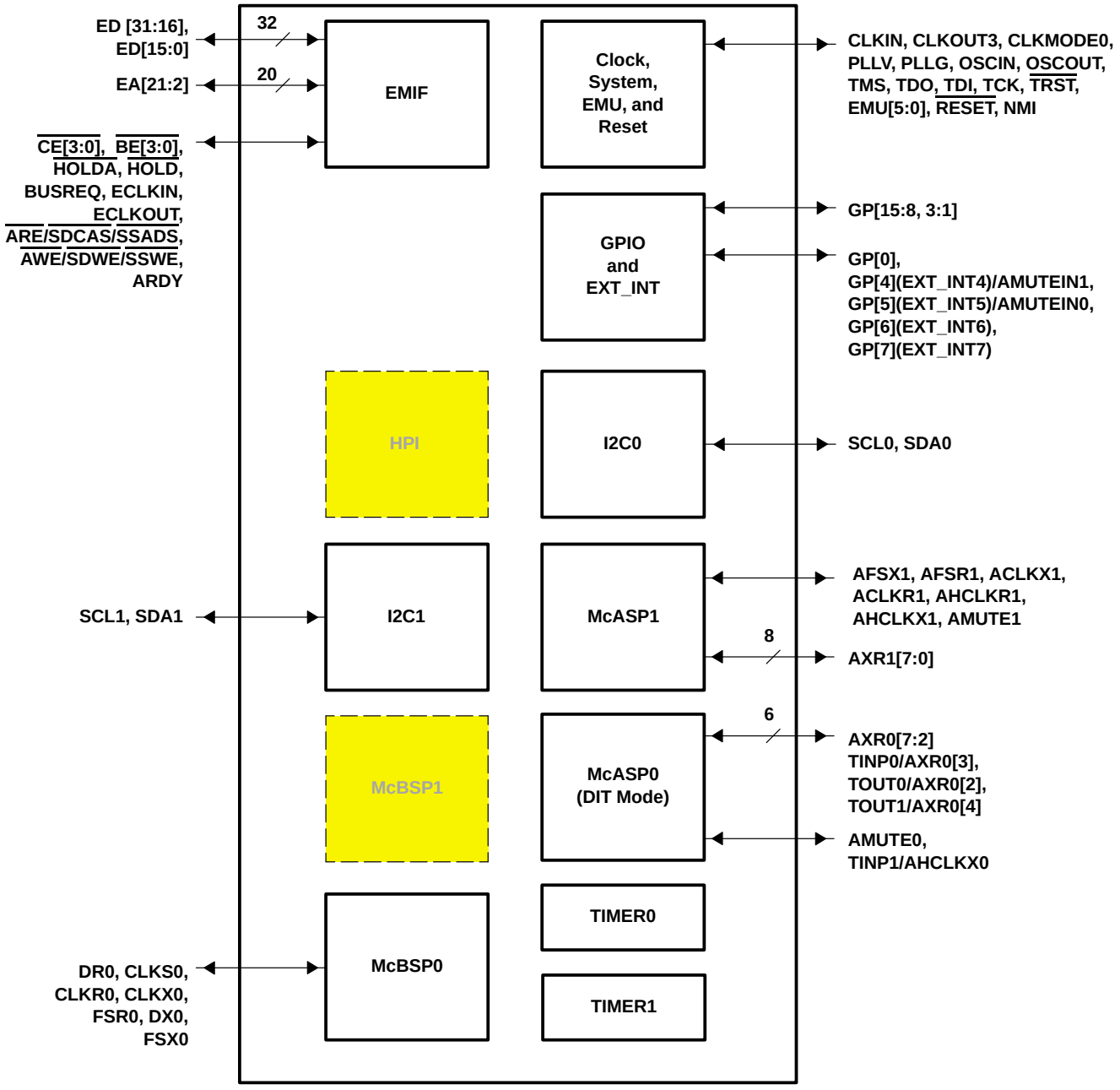
DEVCFG Register Value: 0x0000 000E
McASP0EN = 1
I2C1EN = 0
TOUT0SEL = 1
TOUT1SEL = 1
EKSRC = 0

HPI_EN(HD14) = 0
GP2EN BIT = 1 (GPEN Register)

Figure 6. Configuration Example B (1 I2C + 1 McBSP + 2 McASP)

DEVICE CONFIGURATIONS (CONTINUED)

configuration examples (continued)



DEVCFG Register Value: 0x0000 000D
McASP0EN = 0
I2C1EN = 1
TOUT0SEL = 1
TOUT1SEL = 1
EKSRC = 0

HPI_EN(HD14) = 0
GP2EN BIT = 1 (GPEN Register)

Figure 7. Configuration Example C [2 I2C + 1 McBSP + 1 McASP + 1 McASP (DIT)]

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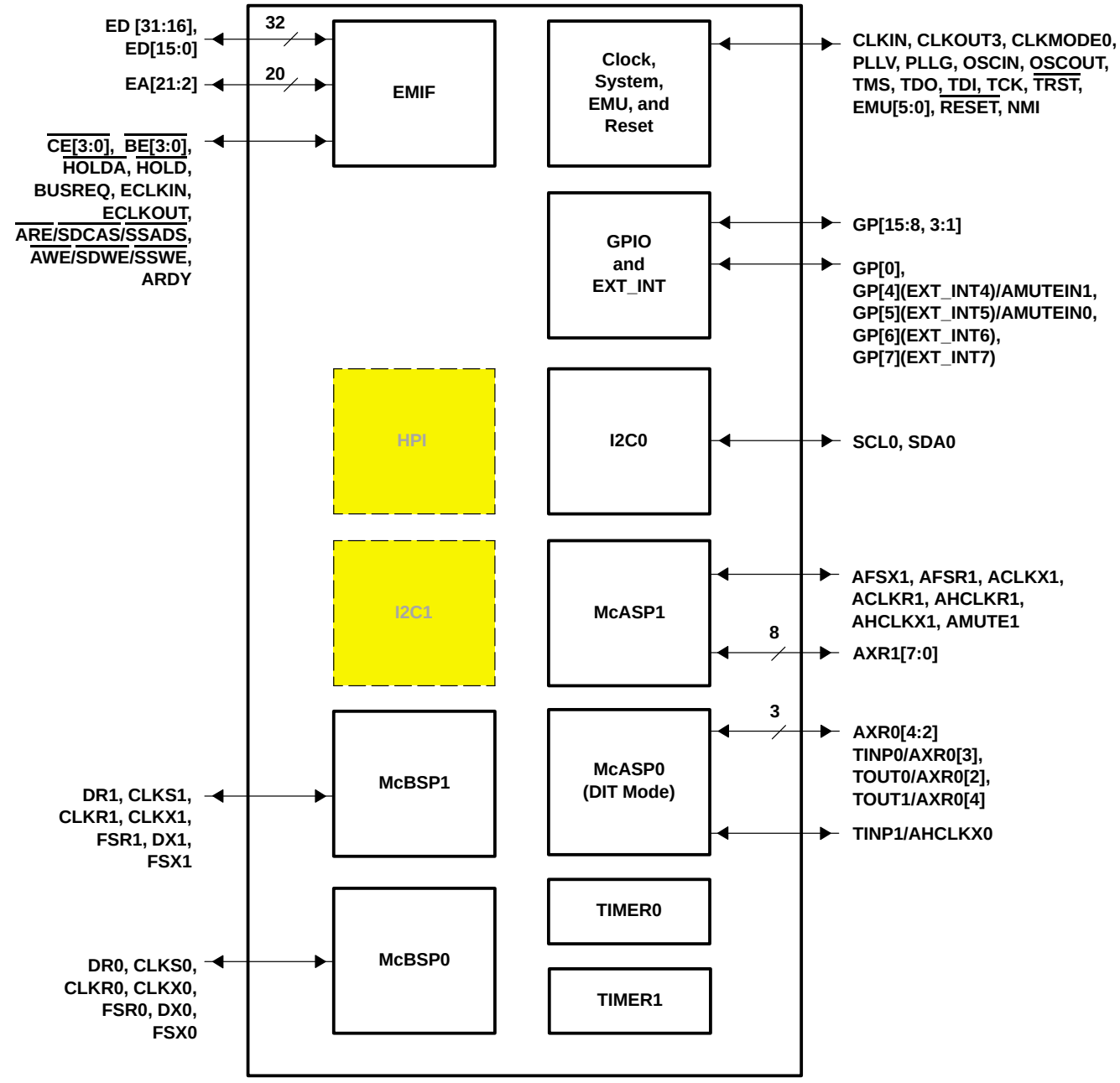
DEVICE CONFIGURATIONS (CONTINUED)

configuration examples (continued)



Shading denotes a peripheral module not available for this configuration.

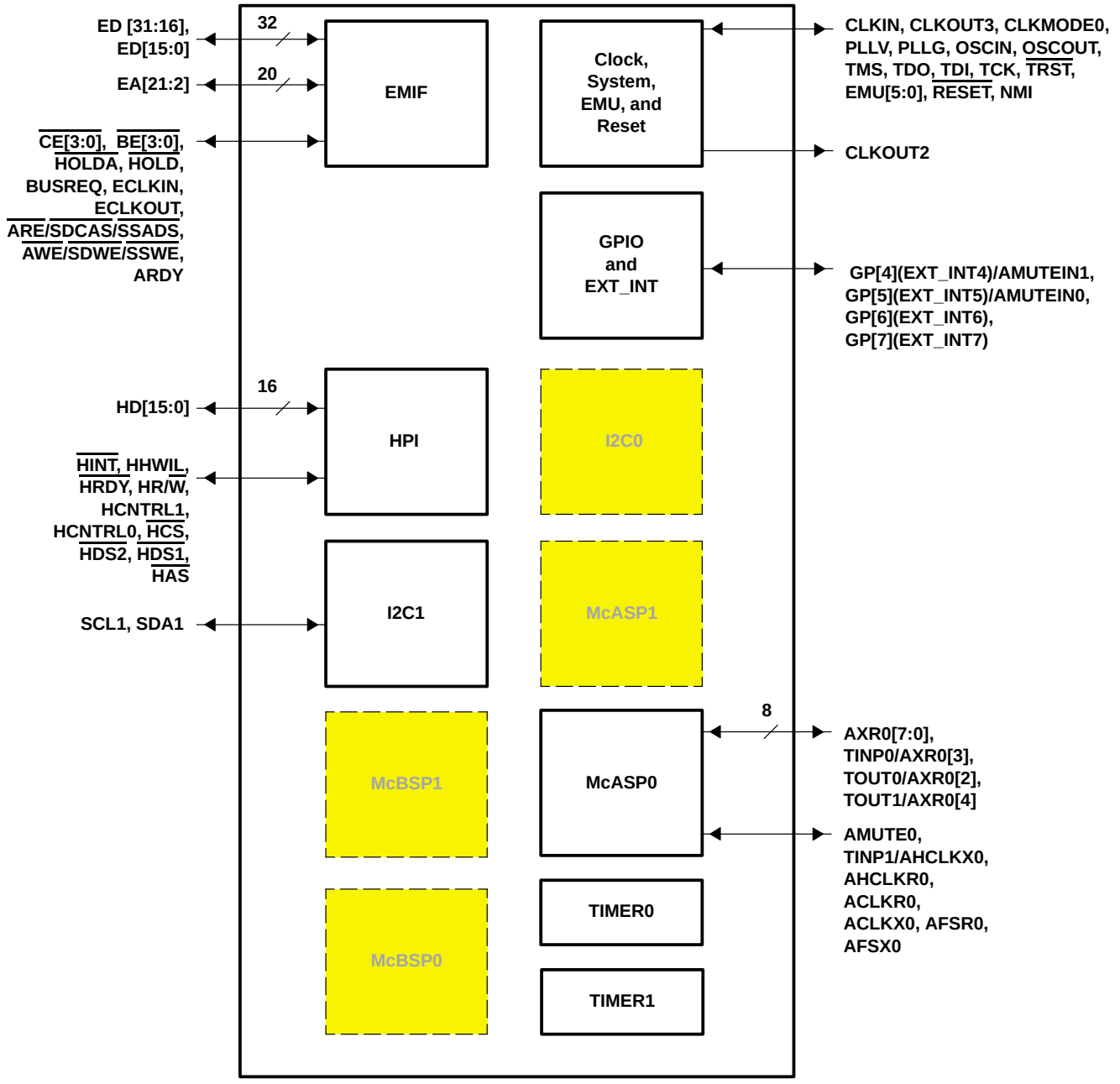
DEVCFG Register Value: 0x0000 000C
McASP0EN = 0
I2C1EN = 0
TOUT0SEL = 1
TOUT1SEL = 1
EKSRC = 0

HPI_EN(HD14) = 0
GP2EN BIT = 1 (GPEN Register)

Figure 8. Configuration Example D [1 I2C + 2 McBSP + 1 McASP + 1 McASP (DIT)]

DEVICE CONFIGURATIONS (CONTINUED)

configuration examples (continued)



Shading denotes a peripheral module not available for this configuration.

DEVCFG Register Value: 0x0000 000F
McASP0EN = 1
I2C1EN = 1
TOUT0SEL = 1
TOUT1SEL = 1
EKSRC = 0

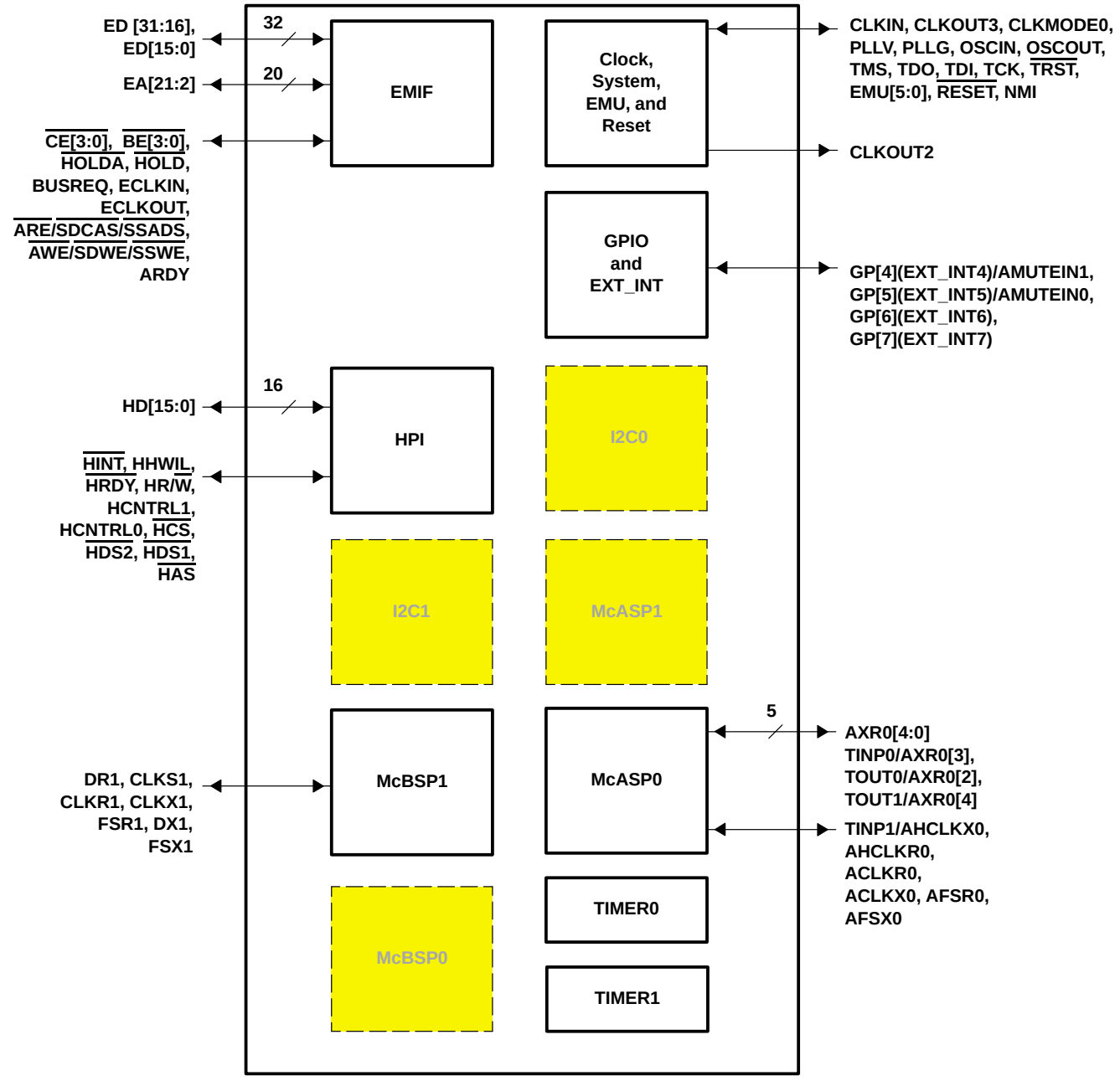
HPI_EN(HD14) = 1
GP2EN BIT = 0 (GPEN Register)

Figure 9. Configuration Example E (1 I2C + HPI + 1 McASP)

PRODUCT PREVIEW

DEVICE CONFIGURATIONS (CONTINUED)

configuration examples (continued)



Shading denotes a peripheral module not available for this configuration.

DEVCFG Register Value: **0x0000 000E**
McASP0EN = 1
I2C1EN = 1
TOUT0SEL = 1
TOUT1SEL = 1
EKSRC = 0

HPI_EN(HD14) = 1
GP2EN BIT = 0 (GPEN Register)

Figure 10. Configuration Example F (1 McBSP + HPI + 1 McASP)

DEVICE CONFIGURATIONS (CONTINUED)

debugging considerations

It is recommended that external connections be provided to peripheral selection/device configuration pins, including HD[14:12, 8, 4, 3], and CLKMODE0. Although internal pullup resistors exist on these pins, providing external connectivity adds convenience to the user in debugging and flexibility in switching operating modes.

Internal pullup/pulldown resistors also exist on the non-configuration pins on the HPI data bus (HD[15, 13, 11:9, 7:5, 2:0]). For proper device operation, ***do not*** oppose the internal pullup/pulldown resistors on these non-configuration pins with external pullup/pulldown resistors. If an external controller provides signals to these non-configuration pins, these signals must be driven to the default state of the pins at reset, or not be driven at all.

For the internal pullup/pulldown resistors for all device pins, see the terminal functions table.

TERMINAL FUNCTIONS

The terminal functions table identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type (I, O/Z, or I/O/Z), whether the pin has any internal pullup/pulldown resistors and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed/shared pins, and debugging considerations, see the Device Configurations section of this data sheet.

Terminal Functions

SIGNAL NAME	PIN NO. PYP	PIN NO. GFN	TYPE†	IPD/ IPU‡	DESCRIPTION
CLOCK/PLL CONFIGURATION					
CLKIN		A3	I	IPD	Clock Input
CLKOUT2/GP[2]		Y12	O/Z	IPD	Clock output at half of device speed (**O/Z**) [default] (SYSCLK2 internal signal from the clock generator) or this pin can be programmed as GP[2] pin (I/O/Z)
CLKOUT3		D10	I	IPD	Programmable clock output (OSC Divider internal signal from clock generator)
CLKMODE0		C4	I	IPU	Clock generator input clock source select 0 – Oscillator pads (OSCIN, OSCOUT directly from the crystal oscillator) 1 – CLKIN square wave [default]
PLLV		A4	A§		Analog power (1.2 V) for PLL
PLLG		C6	A§		Analog ground for PLL
OSCIN		D12	I	—	Crystal oscillator Input (XI)
OSCOUT		C12	O	—	Crystal oscillator output (XO)
JTAG EMULATION					
TMS		B7	I	IPU	JTAG test-port mode select
TDO		A8	O/Z	IPU	JTAG test-port data out
TDI		A7	I	IPU	JTAG test-port data in
TCK		A6	I	IPU	JTAG test-port clock
$\overline{\text{TRST}}$		B6	I	IPD	JTAG test-port reset
EMU5	—	B12	I/O/Z	IPU	Emulation pin 5. Reserved for future use, leave unconnected.
EMU4	—	C11	I/O/Z	IPU	Emulation pin 4. Reserved for future use, leave unconnected.
EMU3	—	B10	I/O/Z	IPU	Emulation pin 3. Reserved for future use, leave unconnected.
EMU2	—	D3	I/O/Z	IPU	Emulation pin 2. Reserved for future use, leave unconnected.
EMU1		B9	I/O/Z	IPU	Emulation pin 1¶
EMU0		D9	I/O/Z	IPU	Emulation pin 0¶
RESETS AND INTERRUPTS					
$\overline{\text{RESET}}$		A13	I	IPU	Device reset
NMI		C13	I	IPD	Nonmaskable interrupt • Edge-driven (rising edge)
GP[7](EXT_INT7)		E3	I/O/Z	IPU	General-purpose input/output pins (**I/O/Z**) which also function as external interrupts [default] • Edge-driven • Polarity independently selected via the External Interrupt Polarity Register bits (EXTPOL.[3:0]) GP[4] and GP[5] pins also function as AMUTEIN1 McASP1 mute input and AMUTEIN0 McASP0 mute input, respectively, if enabled by the INSTAT bit in the McASP AMUTE register.
GP[6](EXT_INT6)		D2			
GP[5](EXT_INT5)/ AMUTEIN0		C1			
GP[4](EXT_INT4)/ AMUTEIN1		C2			

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

§ A = Analog signal (PLL Filter)

¶ The EMU0 and EMU1 pins are internally pulled up with 30-kΩ resistors; therefore, for emulation and normal operation, no external pullup/pulldown resistors are necessary. However, for boundary scan operation, pull down the EMU1 and EMU0 pins with a dedicated 1-kΩ resistor.

PRODUCT PREVIEW

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. PYP	PIN NO. GFN	TYPE†	IPD/ IPU‡	DESCRIPTION
HOST-PORT INTERFACE (HPI)					
$\overline{\text{HINT}}$/GP[1]		J20	O/Z	IPU	Host interrupt (from DSP to host) (**O**) [default] or this pin can be programmed as a GP[1] pin (I/O/Z).
HCNTL1/AXR1[1]		G19	I	IPU	Host control – selects between control, address, or data registers (**I**) [default] or McASP1 data pin 1 (I/O/Z).
HCNTL0/AXR1[3]		G18	I	IPU	Host control – selects between control, address, or data registers (**I**) [default] or McASP1 data pin 3 (I/O/Z).
HHWIL/AFSR1		H20	I	IPU	Host half-word select – first or second half-word (not necessarily high or low order) (**I**) [default] or McASP1 receive frame sync or left/right clock (LRCLK) (I/O/Z).
HR/$\overline{\text{W}}$/AXR1[0]		G20	I	IPU	Host read or write select (**I**) [default] or McASP1 data pin 0 (I/O/Z).
HD15/GP[15]		B14	I/O/Z	IPU	Host-port data pins (**I/O/Z**) [default] or general-purpose input/output pins (I/O/Z) • Used for transfer of data, address, and control • Also controls initialization of DSP modes at reset via pullup/pulldown resistors – Device Endian mode (HD8) 0 – Big Endian 1 – Little Endian – Boot mode (HD[4:3]) 00 – $\overline{\text{CE1}}$ width 32-bit, HPI boot 01 – $\overline{\text{CE1}}$ width 8-bit, Asynchronous external ROM boot with default timings (default mode) 10 – $\overline{\text{CE1}}$ width 16-bit, Asynchronous external ROM boot 11 – $\overline{\text{CE1}}$ width 32-bit, Asynchronous external ROM boot – HPI_EN (HD14) 0 – HPI disabled, McASP1 and I2C0 enabled 1 – HPI enabled, McASP1 and I2C0 disabled (default) **For proper device operation, the HD12 pin must be externally pulled down with a 1-kΩ resistor.** Other HD pins (HD [15, 13, 11:9, 7:5, 2:0] have pullups/pulldowns (IPUs/IPDs). For proper device operation, ***do not*** oppose these pins with external IPUs/IPDs at reset. For more details, see the Device Configurations section of this data sheet.
HD14/GP[14]		C14		IPU	
HD13/GP[13]		A15		IPU	
HD12/GP[12]		C15		IPU	
HD11/GP[11]		A16		IPU	
HD10/GP[10]		B16		IPU	
HD9/GP[9]		C16		IPU	
HD8/GP[8]		B17		IPU	
HD7/GP[3]		A18		IPU	
HD6/AHCLKR1		C17		IPU	Host-port data pin 6 (**I/O/Z**) [default] or McASP1 receive high-frequency master clock (I/O/Z).
HD5/AHCLKX1		B18		IPU	Host-port data pin 5 (**I/O/Z**) [default] or McASP1 transmit high-frequency master clock (I/O/Z).
HD4/GP[0]		C19		IPD	Host-port data pin 4 (**I/O/Z**) [default] or this pin can be programmed as a GP 0 pin (I/O/Z).
HD3/AMUTE1		C20		IPU	Host-port data pin 3 (**I/O/Z**) [default] or McASP1 mute output (I/O/Z).
HD2/AFSX1		D18		IPU	Host-port data pin 2 (**I/O/Z**) [default] or McASP1 transmit frame sync or left/right clock (LRCLK) (I/O/Z).
HD1/AXR1[7]		D20		IPU	Host-port data pin 1 (**I/O/Z**) [default] or McASP1 data pin 7 (I/O/Z).
HD0/AXR1[4]		E20		IPU	Host-port data pin 0 (**I/O/Z**) [default] or McASP1 data pin 4 (I/O/Z).

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. PYP	PIN NO. GFN	TYPE†	IPD/ IPU‡	DESCRIPTION
HOST-PORT INTERFACE (HPI) (CONTINUED)					
$\overline{\text{HAS}}$/ACLKX1		E18	I	IPU	Host address strobe (**I**) [default] or McASP1 transmit bit clock (I/O/Z).
$\overline{\text{HCS}}$/AXR1[2]		F20	I	IPU	Host chip select (**I**) [default] or McASP1 data pin 2 (I/O/Z).
$\overline{\text{HDS1}}$/AXR1[6]		E19	I	IPU	Host data strobe 1 (**I**) [default] or McASP1 data pin 6 (I/O/Z).
$\overline{\text{HDS2}}$/AXR1[5]		F18	I	IPU	Host data strobe 2 (**I**) [default] or McASP1 data pin 5 (I/O/Z) .
$\overline{\text{HRDY}}$/ACLKR1		H19	O/Z	IPD	Host ready (from DSP to host) (**O**) [default] or McASP1 receive bit clock (I/O/Z).
EMIF – COMMON SIGNALS TO ALL TYPES OF MEMORY					
$\overline{\text{CE3}}$		V6	O/Z	IPU	Memory space enables • Enabled by bits 28 through 31 of the word address • Only one asserted during any external data access
$\overline{\text{CE2}}$		W6	O/Z	IPU	
$\overline{\text{CE1}}$		W18	O/Z	IPU	
$\overline{\text{CE0}}$		V17	O/Z	IPU	
$\overline{\text{BE3}}$	—	V5	O/Z	IPU	Byte-enable control • Decoded from the two lowest bits of the internal address • Byte-write enables for most types of memory • Can be directly connected to SDRAM read and write mask signal (SDQM)
$\overline{\text{BE2}}$	—	Y4	O/Z	IPU	
$\overline{\text{BE1}}$		U19	O/Z	IPU	
$\overline{\text{BE0}}$		V20	O/Z	IPU	
EMIF – BUS ARBITRATION					
$\overline{\text{HOLDA}}$		J18	O/Z	IPU	Hold-request-acknowledge to the host
$\overline{\text{HOLD}}$		J17	I	IPU	Hold request from the host
BUSREQ		J19	O/Z	IPU	Bus request output
EMIF – ASYNCHRONOUS/SYNCHROUS MEMORY CONTROL					
ECLKIN		Y11	I	IPD	External EMIF input clock source
ECLKOUT		Y10	O/Z	IPD	EMIF output clock depends on the EKSRC bit (DEVCFG.[16]). • EKSRC = 0 EMIF output clock source is the internal SYSCLK3 signal from the clock generator (default). • EKSRC = 1 ECLKOUT is based on the the external EMIF input clock source pin (ECLKIN).
$\overline{\text{ARE}}$/$\overline{\text{SDCAS}}$/ $\overline{\text{SSADS}}$		V11	O/Z	IPU	Asynchronous memory read enable/SDRAM column-address strobe/SBSRAM address strobe
$\overline{\text{AOE}}$/$\overline{\text{SDRAS}}$/ $\overline{\text{SSOE}}$		W10	O/Z	IPU	Asynchronous memory output enable/SDRAM row-address strobe/SBSRAM output enable
$\overline{\text{AWE}}$/$\overline{\text{SDWE}}$/ $\overline{\text{SSWE}}$		V12	O/Z	IPU	Asynchronous memory write enable/SDRAM write enable/SBSRAM write enable
ARDY		Y5	I	IPU	Asynchronous memory ready input
EMIF – ADDRESS					
EA21		U18	O/Z	IPU	External address (word address)
EA20		Y18			
EA19		W17			
EA18		Y16			
EA17		V16			
EA16		Y15			

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‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

PRODUCT PREVIEW

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. PYP	PIN NO. GFN	TYPE†	IPD/ IPU‡	DESCRIPTION
EMIF – ADDRESS (CONTINUED)					
EA15		W15	O/Z	IPU	External address (word address)
EA14		Y14			
EA13		W14			
EA12		V14			
EA11		W13			
EA10		V10			
EA9		Y9			
EA8		V9			
EA7		Y8			
EA6		W8			
EA5		V8			
EA4		W7			
EA3		V7			
EA2		Y6			
EMIF – DATA					
ED31		N3	I/O/Z	IPU	External data pins (ED[31:16] pins applicable to GFN package only)
ED30		P3			
ED29		P2			
ED28		P1			
ED27		R2			
ED26		R3			
ED25		T2			
ED24		T1			
ED23		U3			
ED22		U1			
ED21		U2			
ED20		V1			
ED19		V2			
ED18		Y3			
ED17		W4			
ED16		V4			
ED15		T19			
ED14		T20			
ED13		T18			
ED12		R20			
ED11		R19			
ED10		P20			
ED9		P18			
ED8		N20			

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground
‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. PYP	PIN NO. GFN	TYPE†	IPD/ IPU‡	DESCRIPTION
EMIF – DATA (CONTINUED)					
ED7		N19	I/O/Z	IPU	External data pins (ED[31:16] pins applicable to GFN package only)
ED6		N18			
ED5		M20			
ED4		M19			
ED3		L19			
ED2		L18			
ED1		K19			
ED0		K18			
MULTICHANNEL AUDIO SERIAL PORT 1 (McASP1)					
GP[4](EXT_INT4)/ AMUTEIN1		C2	I/O/Z	IPU	General-purpose input/output pin 4 and external interrupt 4 (**I/O/Z**) [default] or McASP1 mute input (I/O/Z).
HD3/AMUTE1		C20	I/O/Z	IPU	Host-port data pin 3 (**I/O/Z**) [default] or McASP1 mute output (I/O/Z).
$\overline{\text{HRDY}}$/ACLKR1		H19	I/O/Z	IPU	Host ready (from DSP to host) (**O**) [default] or McASP1 receive bit clock (I/O/Z).
HD6/AHCLKR1		C17	I/O/Z	IPU	Host-port data pin 6 (**I/O/Z**) [default] or McASP1 receive high-frequency master clock (I/O/Z).
$\overline{\text{HAS}}$/ACLKX1		E18	I/O/Z	IPU	Host address strobe (**I**) [default] or McASP 1 transmit bit clock (I/O/Z).
HD5/AHCLKX1		B18	I/O/Z	IPU	Host-port data pin 5 (**I/O/Z**) [default] or McASP1 transmit high-frequency master clock (I/O/Z).
HHWIL/AFSR1		H20	I/O/Z	IPU	Host half-word select – first or second half-word (not necessarily high or low order) (**I**) [default] or McASP1 receive frame sync or left/right clock (LRCLK) (I/O/Z).
HD2/AFSX1		D18	I/O/Z	IPU	Host-port data pin 2 (**I/O/Z**) [default] or McASP1 transmit frame sync or left/right clock (LRCLK) (I/O/Z).
HD1/AXR1[7]		D20	I/O/Z	IPU	Host-port data pin 1 (**I/O/Z**) [default] or McASP1 data pin 7 (I/O/Z).
$\overline{\text{HDS1}}$/AXR1[6]		E19	I/O/Z	IPU	Host data strobe 1 (**I**) [default] or McASP1 data pin 6 (I/O/Z).
$\overline{\text{HDS2}}$/AXR1[5]		F18	I/O/Z	IPU	Host data strobe 2 (**I**) [default] or McASP1 data pin 5 (I/O/Z).
HD0/AXR1[4]		E20	I/O/Z	IPU	Host-port data pin 0 (**I/O/Z**) [default] or McASP1 data pin 4 (I/O/Z).
HCNTL0/AXR1[3]		G18	I/O/Z	IPU	Host control – selects between control, address, or data registers (**I**) [default] or McASP1 data pin 3 (I/O/Z).
$\overline{\text{HCS}}$/AXR1[2]		F20	I/O/Z	IPU	Host chip select (**I**) [default] or McASP1 data pin 2 (I/O/Z).
HCNTL1/AXR1[1]		G19	I/O/Z	IPU	Host control – selects between control, address, or data registers (**I**) [default] or McASP1 data pin 1 (I/O/Z).
HR/$\overline{\text{W}}$/AXR1[0]		G20	I/O/Z	IPU	Host read or write select (**I**) [default] or McASP1 data pin 0 (I/O/Z).

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

PRODUCT PREVIEW

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. PYP	PIN NO. GFN	TYPE†	IPD/ IPU‡	DESCRIPTION
MULTICHANNEL AUDIO SERIAL PORT 0 (McASP0)					
GP[5](EXT_INT5)/ AMUTEIN0		C1	I/O/Z	IPU	General-purpose input/output pin 5 and external interrupt 5 (**I/O/Z**) [default] or McASP0 mute input (I/O/Z).
CLKX1/AMUTE0		L3	I/O/Z	IPD	McBSP1 transmit clock (**I/O/Z**) [default] or McASP0 mute output (I/O/Z).
CLKR0/ACLKR0		H3	I/O/Z	IPD	McBSP0 receive clock (**I/O/Z**) [default] or McASP0 receive bit clock (I/O/Z).
TINP1/AHCLKX0		F2	I/O/Z	IPD	Timer 1 input (**I**) [default] or McBSP0 transmit high-frequency master clock (I/O/Z).
CLKX0/ACLKX0		G3	I/O/Z	IPD	McBSP0 transmit clock (**I/O/Z**) [default] or McASP0 transmit bit clock (I/O/Z).
CLKS0/AHCLKR0		K3	I/O/Z	IPD	McBSP0 external clock source (as opposed to internal) (**I**) [default] or McASP0 receive high-frequency master clock (I/O/Z).
FSR0/AFSR0		J3	I/O/Z	IPD	McBSP0 receive frame sync (**I/O/Z**) [default] or McASP0 receive frame sync or left/right clock (LRCLK) (I/O/Z).
FSX0/AFSX0		H1	I/O/Z	IPD	McBSP0 transmit frame sync (**I/O/Z**) [default] or McASP0 transmit frame sync or left/right clock (LRCLK) (I/O/Z).
FSR1/AXR0[7]		M3	I/O/Z	IPD	McBSP1 receive frame sync (**I/O/Z**) [default] or McASP0 data pin 7 (I/O/Z).
CLKR1/AXR0[6]		M1	I/O/Z	IPD	McBSP1 receive clock (**I/O/Z**) [default] or McASP0 data pin 6 (I/O/Z).
DX1/AXR0[5]		L2	I/O/Z	IPU	McBSP1 rransmit data (**O/Z**) [default] or McASP0 data pin 5 (I/O/Z).
TOUT1/AXR0[4]		F1	I/O/Z	IPD	Timer 1 output (**O**) [default] or McASP0 data pin 4 (I/O/Z).
TINP0/AXR0[3]		G2	I/O/Z	IPD	Timer 0 input (**I**) [default] or McASP0 data pin 3 (I/O/Z).
TOUT0/AXR0[2]		G1	I/O/Z	IPD	Timer 0 output (**O**) [default] or McASP0 data pin 2 (I/O/Z).
DX0/AXR0[1]		H2	I/O/Z	IPU	McBSP0 transmit data (**O/Z**) [default] or McASP0 data pin 1 (I/O/Z).
DR0/AXR0[0]		J1	I/O/Z	IPU	McBSP0 receive data (**I**) [default] or McASP0 data pin 0 (I/O/Z).
TIMER 1					
TOUT1/AXR0[4]		F1	O	IPD	Timer 1 output (**O**) [default] or McASP0 data pin 4 (I/O/Z).
TINP1/AHCLKX0		F2	I	IPD	Timer 1 input (**I**) [default] or McBSP0 transmit high-frequency master clock (I/O/Z).
TIMER0					
TOUT0/AXR0[2]		G1	O	IPD	Timer 0 output (**O**) [default] or McASP0 data pin 2 (I/O/Z).
TINP0/AXR0[3]		G2	I	IPD	Timer 0 input (**I**) [default] or McASP0 data pin 3 (I/O/Z).

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. PYP	PIN NO. GFN	TYPE†	IPD/ IPU‡	DESCRIPTION
MULTICHANNEL BUFFERED SERIAL PORT 1 (McBSP1)					
CLKS1/SCL1		E1	I	IPD	McBSP1 external clock source (as opposed to internal) (**I**) [default] or I2C1 clock (I/O/Z).
CLKR1/AXR0[6]		M1	I/O/Z	IPD	McBSP1 receive clock (**I/O/Z**) [default] or McASP0 TX/RX data pin 6 (I/O/Z).
CLKX1/AMUTE0		L3	I/O/Z	IPD	McBSP1 transmit clock (**I/O/Z**) [default] or McASP0 mute output (I/O/Z).
DR1/SDA1		M2	I	IPU	McBSP1 receive data (**I**) [default] or I2C1 data (I/O/Z).
DX1/AXR0[5]		L2	O/Z	IPU	McBSP1 transmit data (**O/Z**) [default] or McASP0 TX/RX data pin 5 (I/O/Z).
FSR1/AXR0[7]		M3	I/O/Z	IPD	McBSP1 receive frame sync (**I/O/Z**) [default] or McASP0 TX/RX data pin 7 (I/O/Z).
FSX1		L1	I/O/Z	IPD	McBSP1 transmit frame sync
MULTICHANNEL BUFFERED SERIAL PORT 0 (McBSP0)					
CLKS0/AHCLKR0		K3	I	IPD	McBSP0 external clock source (as opposed to internal) (**I**) [default] or McASP0 receive high-frequency master clock (I/O/Z).
CLKR0/ACLKR0		H3	I/O/Z	IPD	McBSP0 receive clock (**I/O/Z**) [default] or McASP0 receive bit clock (I/O/Z).
CLKX0/ACLKX0		G3	I/O/Z	IPD	McBSP0 transmit clock (**I/O/Z**) [default] or McASP0 transmit bit clock (I/O/Z).
DR0/AXR0[0]		J1	I	IPU	McBSP0 receive data (**I**) [default] or McASP0 TX/RX data pin 0 (I/O/Z).
DX0/AXR0[1]		H2	O/Z	IPU	McBSP0 transmit data (**O/Z**) [default] or McASP0 TX/RX data pin 1 (I/O/Z).
FSR0/AFSR0		J3	I/O/Z	IPD	McBSP0 receive frame sync (**I/O/Z**) [default] or McASP0 receive frame sync or left/right clock (LRCLK) (I/O/Z).
FSX0/AFSX0		H1	I/O/Z	IPD	McBSP0 transmit frame sync (**I/O/Z**) [default] or McASP0 transmit frame sync or left/right clock (LRCLK) (I/O/Z).
INTER-INTEGRATED CIRCUIT 1 (I2C1)					
CLKS1/SCL1		E1	I/O/Z	IPD	McBSP1 external clock source (as opposed to internal) (**I**) [default] or I2C1 clock (I/O/Z).
DR1/SDA1		M2	I/O/Z	IPU	McBSP1 receive data (**I**) [default] or I2C1 data (I/O/Z).
INTER-INTEGRATED CIRCUIT 0 (I2C0)					
SCL0		N1	I/O/Z	IPU	I2C0 clock.
SDA0		N2	I/O/Z	IPU	I2C0 data.

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‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

PRODUCT PREVIEW

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. PYP	PIN NO. GFN	TYPE†	IPD/ IPU‡	DESCRIPTION
GENERAL-PURPOSE INPUT/OUTPUT (GPIO)					
HD15/GP[15]		B14	I/O/Z	IPU	Host-port data pins (**I/O/Z**) [default] or general-purpose input/output pins (I/O/Z) • Used for transfer of data, address, and control • Also controls initialization of DSP modes at reset via pullup/pulldown resistors – Device Endian mode (HD8) 0 – Big Endian 1 – Little Endian – Boot mode (HD[4:3]) 00 – $\overline{CE1}$ width 32-bit, HPI boot 01 – $\overline{CE1}$ width 8-bit, Asynchronous external ROM boot with default timings (default mode) 10 – $\overline{CE1}$ width 16-bit, Asynchronous external ROM boot 11 – $\overline{CE1}$ width 32-bit, Asynchronous external ROM boot – HPI_EN (HD14) 0 – HPI disabled, McASP1 and I2C0 enabled 1 – HPI enabled, McASP1 and I2C0 disabled (default) **For proper device operation, the HD12 pin must be externally pulled down with a 1-kΩ resistor.** Other HD pins (HD [15, 13, 11:9, 7:5, 2:0] have pullups/pulldowns (IPUs/IPDs). For proper device operation, ***do not*** oppose these pins with external IPUs/IPDs at reset. For more details, see the Device Configurations section of this data sheet.
HD14/GP[14]		C14		IPU	
HD13/GP[13]		A15		IPU	
HD12/GP[12]		C15		IPU	
HD11/GP[11]		A16		IPU	
HD10/GP[10]		B16		IPU	
HD9/GP[9]		C16		IPU	
HD8/GP[8]		B17		IPU	
GP[7](EXT_INT7)		E3	I/O/Z	IPU	General-purpose input/output pins (**I/O/Z**) which also function as external interrupts [default] • Edge-driven • Polarity independently selected via the External Interrupt Polarity Register bits (EXTPOL.[3:0]) GP[4] and GP[5] pins also function as AMUTEIN1 McASP1 mute input and AMUTEIN0 McASP0 mute input, respectively, if enabled by the INSTAT bit in the McASP AMUTE register.
GP[6](EXT_INT6)		D2			
GP[5](EXT_INT5)/ AMUTEIN0		C1			
GP[4](EXT_INT4)/ AMUTEIN1		C2			
HD7/GP[3]		A18	I/O/Z	IPU	Host-port data pin 7 (**I/O/Z**) [default] or general-purpose input/output 0 pin 3 (I/O/Z)
CLKOUT2/GP[2]		Y12	I/O/Z	IPD	Clock output at half of device speed (**O/Z**) [default] or this pin can be programmed as GP[2] pin.
$\overline{HINT}$/GP[1]		J20	O	IPU	Host interrupt (from DSP to host) (**O**) [default] or this pin can be programmed as a GP[1] pin (I/O/Z).
HD4/GP[0]		C19	I/O/Z	IPD	Host-port data pin 4 (**I/O/Z**) [default] or this pin can be programmed as a GP[0] pin (I/O/Z).
RESERVED FOR TEST					
RSV0		A5	O/Z	IPU	Reserved. (Leave unconnected, **do not** connect to power or ground)
RSV1		B5	A§		Reserved. (Leave unconnected, **do not** connect to power or ground)
RSV2		D7	O/Z	IPD	Reserved. (Leave unconnected, **do not** connect to power or ground)

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground
‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)
§ A = Analog signal

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. PYP	PIN NO. GFN	TYPE†	DESCRIPTION
SUPPLY VOLTAGE PINS				
DV_{DD}		A17	S	3.3-V supply voltage
		B3		
		B8		
		B13		
		C5		
		C10		
		D1		
		D16		
		D19		
		F3		
		H18		
		J2		
		M18		
		R1		
		R18		
		T3		
		U5		
		U7		
		U12		
		U16		
		V13		
		V15		
		V19		
		W3		
		W9		
		W12		
		Y7		
		Y17		
CV_{DD}		A9	S	1.2-V supply voltage
		A10		
		A12		
		B2		
		B19		
		C3		
		C7		
		C18		
		D5		
		D6		
		D11		
		D14		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. PYP	PIN NO. GFN	TYPE†	DESCRIPTION
SUPPLY VOLTAGE PINS (CONTINUED)				
CV_{DD}		D15	S	1.2-V supply voltage
		F4		
		F17		
		K1		
		K4		
		K17		
		L4		
		L17		
		L20		
		R4		
		R17		
		U6		
		U10		
		U11		
		U14		
		U15		
		V3		
		V18		
		W2		
		W19		
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		—		
		—		
		—		
		—		
		—		
		—		
		—		
GROUND PINS				
V_{SS}		A1	GND	Ground pins
		A2		
		A11		
		A14		
		A19		
		A20		
		B1		
		B4		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Terminal Functions (Continued)

SIGNAL NAME	PIN NO. PYP	PIN NO. GFN	TYPE†	DESCRIPTION
GROUND PINS (CONTINUED)				
V_{SS}		B11	GND	Ground pins
		B15		
		B20		
		C8		
		C9		
		D4		
		D8		
		D13		
		D17		
		E2		
		E4		
		E17		
		F19		
		G4		
		G17		
		H4		
		H17		
		J4		
		K2		
		K20		
		M4		
		M17		
		N4		
		N17		
		P4		
		P17		
		P19		
		T4		
		T17		
		U4		
		U8		
		U9		
		U13		
		U17		
		U20		
		W1		
		W5		
		W11		
		W16		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

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Terminal Functions (Continued)

SIGNAL NAME	PIN NO. PYP	PIN NO. GFN	TYPE†	DESCRIPTION
GROUND PINS (CONTINUED)				
V_{SS}		W20	GND	Ground pins
		Y1		
		Y2		
		Y13		
		Y19		
		Y20		
		—		
		—		
		—		
		—		
		—		
		—		
		—		
		—		
		—		
		—		
		—		
		—		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

development support

TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of C6000™ DSP-based applications:

Software Development Tools:
Code Composer Studio™ Integrated Development Environment (IDE): including Editor
C/C++/Assembly Code Generation, and Debug plus additional development tools
Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools:
Extended Development System (XDS™) Emulator (supports C6000™ DSP multiprocessor system debug)
EVM (Evaluation Module)

The *TMS320 DSP Development Support Reference Guide* (SPRU011) contains information about development-support products for all TMS320™ DSP family member devices, including documentation. See this document for further information on TMS320™ DSP documentation or any TMS320™ DSP support products from Texas Instruments. An additional document, the *TMS320 Third-Party Support Reference Guide* (SPRU052), contains information about TMS320™ DSP-related products from other companies in the industry. To receive TMS320™ DSP literature, contact the Literature Response Center at 800/477-8924.

For a complete listing of development-support tools for the TMS320C6000™ DSP platform, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL) and select “Find Development Tools”. For device-specific tools, under “Semiconductor Products”, select “Digital Signal Processors”, choose a product family, and select the particular DSP device. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

device and development-support tool nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP commercial family member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

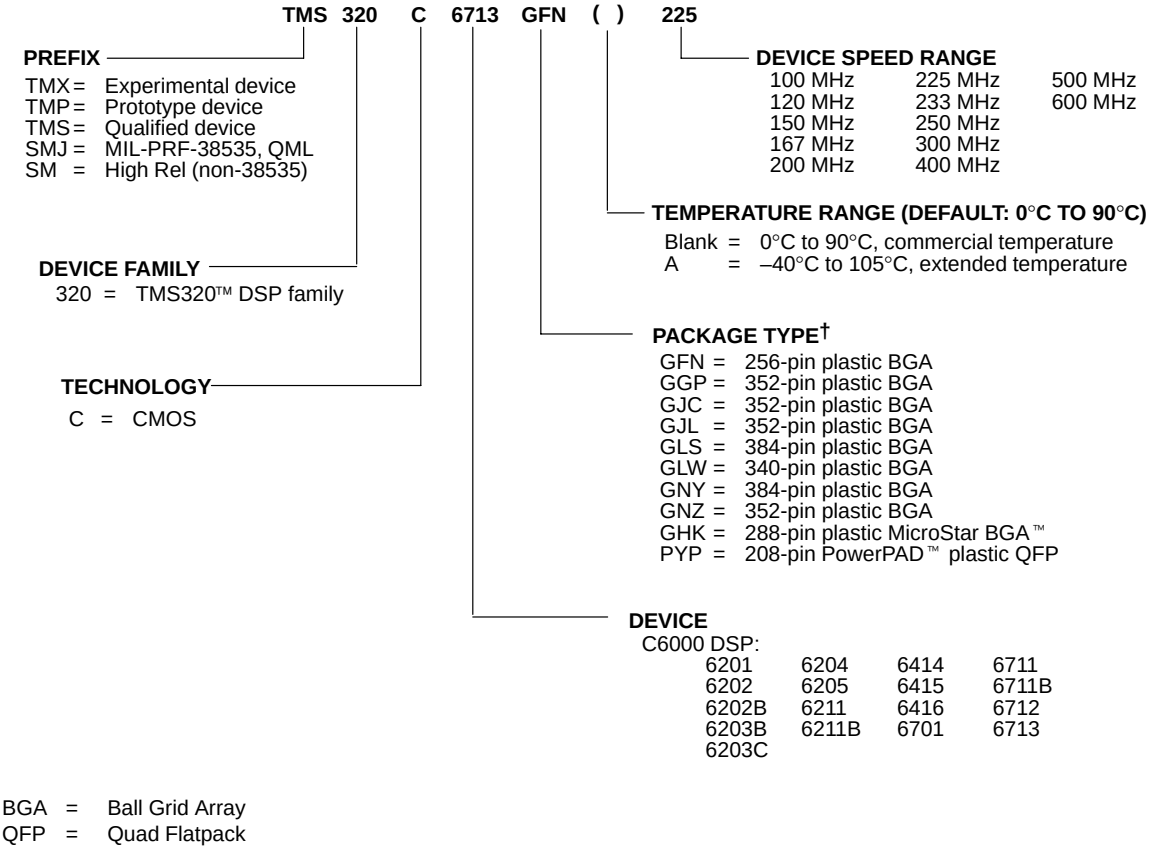
TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, GFN), the temperature range (for example, blank is the default commercial temperature range), and the device speed range in megahertz (for example, -225 is 225 MHz).

Figure 11 provides a legend for reading the complete device name for any TMS320C6000™ DSP family member.

device and development-support tool nomenclature (continued)

Table 32. TMS320C6713 Device Part Numbers (P/Ns) and Ordering Information

DEVICE ORDERABLE P/N	DEVICE SPEED	CORE and I/O VOLTAGE		OPERATING CASE TEMPERATURE RANGE
		CV_{DD} (CORE)	DV_{DD} (I/O)	
C6713				
TMS320C6713GFN225	225 MHz/1350 MFLOPS	1.2 V	3.3 V	0°C to 90°C
TMS320C6713GFN150	150 MHz/900 MFLOPS	1.2 V	3.3 V	0°C to 90°C
TMS320C6713PYP150	150 MHz/900 MFLOPS	1.2 V	3.3 V	0°C to 90°C



† BGA = Ball Grid Array
QFP = Quad Flatpack

Figure 11. TMS320C6000™ DSP Device Nomenclature (Including the TMS320C6713 Device)

PRODUCT PREVIEW

MicroStar BGA and PowerPAD are trademarks of Texas Instruments.

documentation support

Extensive documentation supports all TMS320™ DSP family generations of devices from product announcement through applications development. The types of documentation available include: data sheets, such as this document, with design specifications; complete user's reference guides for all devices and tools; technical briefs; development-support tools; on-line help; and hardware and software applications. The following is a brief, descriptive list of support documentation specific to the C6000™ DSP devices:

The *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189) describes the C6000™ CPU (DSP core) architecture, instruction set, pipeline, and associated interrupts.

The *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190) describes the functionality of the peripherals available on the C6000™ DSP platform of devices, such as the external memory interface (EMIF), host-port interface (HPI), multichannel buffered serial ports (McBSPs), direct-memory-access (DMA), enhanced direct-memory-access (EDMA) controller, expansion bus (XB), clocking and phase-locked loop (PLL); and power-down modes. This guide also includes information on internal data and program memories.

The *PowerPAD Thermally Enhanced Package Technical brief* (literature number SLMA002) focuses on the specifics of integrating a PowerPAD package into the printed circuit board design to make optimum use of the thermal efficiencies designed into the PowerPAD package.

The *TMS320C6000 Technical Brief* (literature number SPRU197) gives an introduction to the C62x™/C67x™ devices, associated development tools, and third-party support.

The tools support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE). For a complete listing of C6000™ DSP latest documentation, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL).

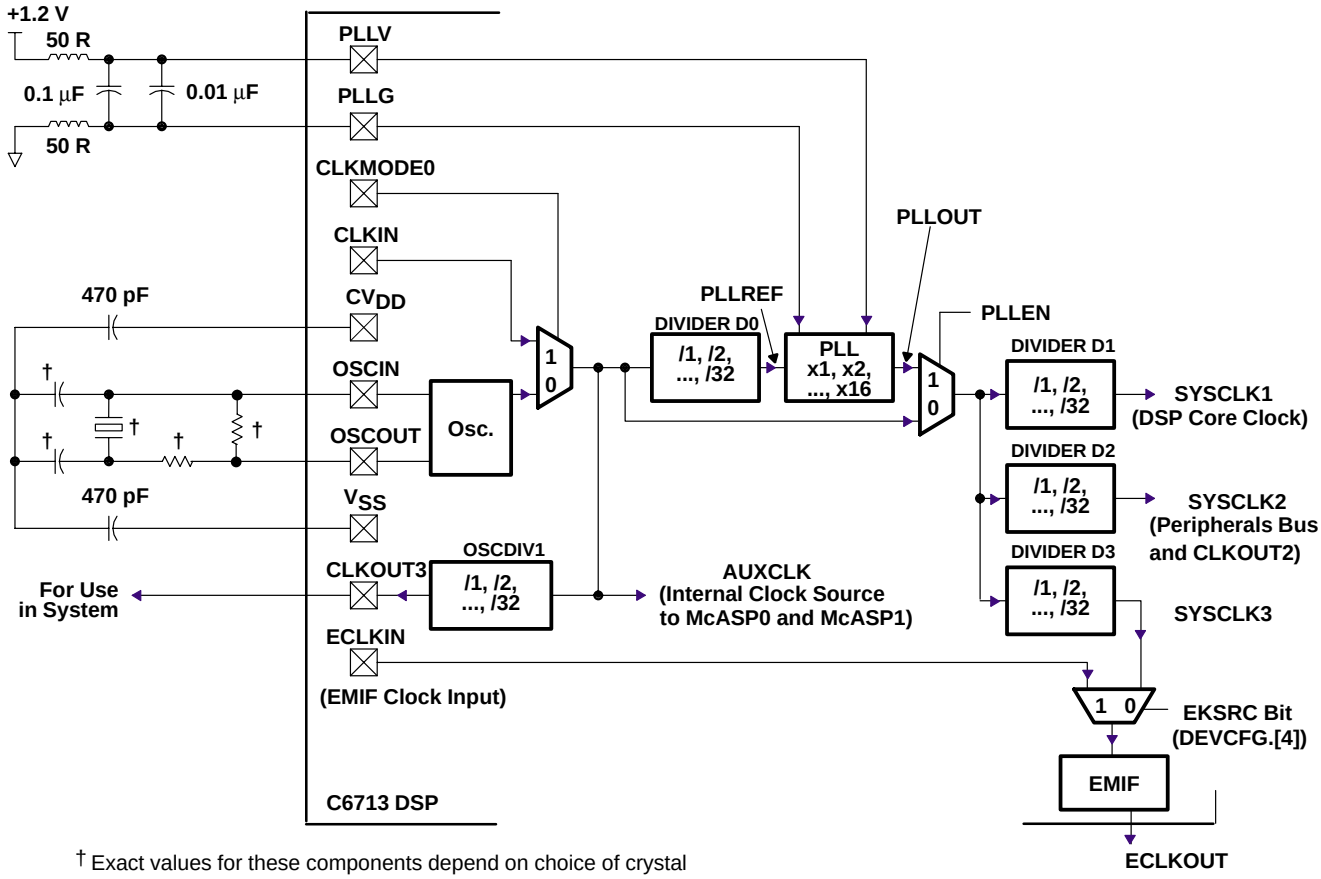
See the Worldwide Web URL for the application report *How To Begin Development Today with the TMS320C6713 Floating-Point DSP* (literature number SPRA809), which describes in more detail the similarities/differences between the C6713 and C6711 C6000™ DSP devices.

C62x is a trademark of Texas Instruments.

clock generator, oscillator, and PLL

The TMS320C6713 includes a flexible clock generator module consisting of a PLL and oscillator, with several dividers so that different clocks may be generated for different parts of the system (i.e., DSP core, Internal Peripheral Control, External Memory Interface – EMIF, and Audio Peripheral Serial Clocks).

Figure 12 illustrates the PLL and clock generator logic.



† Exact values for these components depend on choice of crystal

Figure 12. PLL and Clock Generator Logic

The clock may be sourced either from an externally generated 3.3-V clock input on the CLKIN pin, or from the on-chip oscillator if an external crystal circuit is attached to the device. The oscillator supports fundamental mode crystals up to 30 MHz.

This reference clock (AUXCLK) is also directly available to the McASP modules for use as an internal serial port clock; and may be divided down by a programmable divider (/1, /2, /3, ..., /32) and output on the CLKOUT3 pin for other use in the system.

The input clock source may then either be divided down (by /1, /2, ..., /32) and then multiplied up by a factor of x1, x2, x3, and so on, up to x16.

Either the input clock or the PLL output (if PLLEN is selected) then serves as the high-frequency reference clock for the rest of the DSP system. The DSP core clock, the peripheral bus control clock, and the EMIF clock may be divided down from this high-frequency clock (each with a unique divider) . For example, with a 30 MHz input if the PLL output is configured for 450 MHz, the DSP core may be operated at 225 MHz (/2) while the EMIF may be configured to operate at a rate of 75 MHz (/6).

clock generator, oscillator, and PLL (continued)

The EMIF itself may be clocked from a totally unrelated (asynchronous) reference clock input on the ECLKIN pin if a specific EMIF frequency is needed, or from the on-chip clock generation logic.

The settings for the PLL multiplier and each of the dividers in the clock generation block may be reconfigured via software at run time. If either the input to the PLL is changed or if the PLL multiplier is changed, then software must enter bypass first and stay in bypass until the PLL has had enough time to lock (see electrical specifications).

The clock generator has dedicated power supply pins, and it is recommended that these pins be filtered with a pair of 50R ferrite beads in series with each supply line, bypassed with a pair of capacitors (0.1 μF and 0.01 μF) as close to the device pins (PLLV, PLLG) as possible (as shown in Figure 12).

Similarly, for the lowest jitter on the oscillator circuit, it is recommended that a pair of 470-pF capacitors be connected between an isolated (not directly connected to the board supply) CV_{DD} and V_{SS} pin on either side of the oscillator. This helps to cancel out switching noise from other circuits on the DSP device.

Note that there is a specific minimum and maximum input clock for the block labeled PLL in Figure 12, as well as for the DSP core, peripheral control, and EMIF. In addition, there is a maximum output frequency for the PLL. The clock generator must not be configured to exceed any of these constraints (certain combinations of external clock input, internal dividers, and PLL multiply ratios might not be supported).

SYSCLK2 is the internal clock source for peripheral bus control. SYSCLK2 (Divider D2) ***must*** be programmed to be half of the SYSCLK1 rate. For example, if D1 is configured to divide-by-2 mode (/2), then D2 ***must*** be programmed to divide-by-4 mode (/4). SYSCLK2 is also tied directly to CLKOUT2 pin (see Figure 12).

For detailed information on the clock generator (PLL and oscillator registers) and their associated software bit descriptions, see Table 33 through Table 36.

clock generator, oscillator, and PLL (continued)

PLLCSR Register (0x01B7 C100)

31	28	27	24	23	20	19	16
Reserved							
R–0							

15	12	11	8	7	6	5	4	3	2	1	0
Reserved				STABLE	Reserved			PLLRST	–	PLLPWRDN	PLLEN
R–0				RW–0	R–0			RW–1	R–0	R/W–0b	RW–0

Legend: R = Read only, R/W = Read/Write; -n = value after reset

Table 33. PLL Control/Status Register (PLLCSR)

BIT #	NAME	DESCRIPTION
31:7	Reserved	Reserved. Read-only, writes have no effect.
6	STABLE	Oscillator Input Stable. This bit indicates if the OSCIN/CLKIN input has stabilized. 0 – OSCIN/CLKIN input not yet stable. Oscillator counter is not finished counting (default). 1 – OSCIN/CLKIN input stable.
5:4	Reserved	Reserved. Read-only, writes have no effect.
3	PLLRST	Asserts RESET to PLL 0 – PLL Reset Released. 1 – PLL Reset Asserted (default).
2	Reserved	Reserved. Read-only, writes have no effect.
1	PLLPWRDN	Select PLL Power Down 0 – PLL Operational (default). 1 – PLL Placed in Power-Down State.
0	PLLEN	PLL Mode Enable 0 – Bypass Mode (default). PLL disabled. Divider D0 and PLL are bypassed. SYSCLK1/SYSCLK2/SYSCLK3 are divided down directly from input reference clock. 1 – PLL Enabled. Divider D0 and PLL are not bypassed. SYSCLK1/SYSCLK2/SYSCLK3 are divided down from PLL output.

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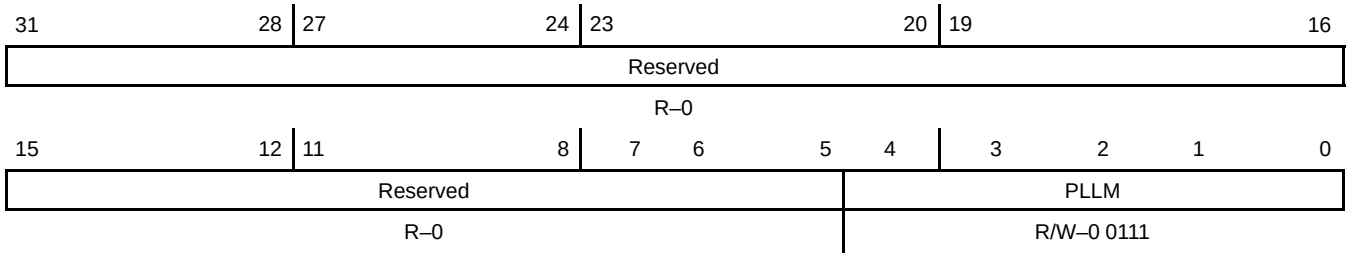
clock generator, oscillator, and PLL (continued)

PLLM Register (0x01B7 C110)



Legend: R = Read only, R/W = Read/Write; -n = value after reset

Table 34. PLL Multiplier Control Register (PLLM)

BIT #	NAME	DESCRIPTION
31:5	Reserved	Reserved. Read-only, writes have no effect.
4:0	PLLM	PLL multiply mode [default is x8 (0 0111)]. 00000 = x1 01000 = x9 00001 = x2 01001 = x10 00010 = x3 01010 = x11 00011 = x4 01011 = x12 00100 = x5 01100 = x13 00101 = x6 01101 = x14 00110 = x7 01110 = x15 00111 = x8 01111 = x16 PLLM select values 10000 through 11111 are *not* supported.

clock generator, oscillator, and PLL (continued)

PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3 Registers (0x01B7 C114, 0x01B7 C118, 0x01B7 C11C, and 0x01B7 C120, respectively)

31 – 28	27 – 24	23 – 20	19 – 16
Reserved			
R–0			

15	14 – 12	11 – 8	7 – 5	4	3 – 2	1 – 0
DxEN	Reserved			PLLDIVx		
R/W–1	R–0			R/W–x xxxx†		

Legend: R = Read only, R/W = Read/Write; -n = value after reset

† Default values for the PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3 bits are /1 (0 0000), /1 (0 0000), /2 (0 0001), and /2 (0 0001), respectively.

Table 35. PLL Wrapper Divider x Registers (Prescaler D0 and Dividers D1, D2, and D3)‡

BIT #	NAME	DESCRIPTION
31:16	Reserved	Reserved. Read-only, writes have no effect.
15	DxEN	Divider Dx Enable (where x denotes 0 through 3). 0 – Divider x Disabled. No clock output. 1 – Divider x Enabled (default).
14:5	Reserved	Reserved. Read-only, writes have no effect.
4:0	PLLDIVx	PLL Divider Ratio [Default values for the PLLDIV0, PLLDIV1, PLLDIV2, and PLLDIV3 bits are /1, /1, /2, and /2, respectively]. 00000 = /1 10000 = /17 00001 = /2 10001 = /18 00010 = /3 10010 = /19 00011 = /4 10011 = /20 00100 = /5 10100 = /21 00101 = /6 10101 = /22 00110 = /7 10110 = /23 00111 = /8 10111 = /24 01000 = /9 11000 = /25 01001 = /10 11001 = /26 01010 = /11 11010 = /27 01011 = /12 11011 = /28 01100 = /13 11100 = /29 01101 = /14 11101 = /30 01110 = /15 11110 = /31 01111 = /16 11111 = /32

‡ Note that SYSCLK2 *must* run at half the rate of SYSCLK1. Therefore, the divider ratio of D2 must be two times slower than D1. For example, if D1 is set to /2, then D2 *must* be set to /4.

clock generator, oscillator, and PLL (continued)

OSCDIV1 Register (0x01B7 C124)

31 – 28	27 – 24	23 – 20	19 – 16
Reserved			
R–0			

15	14 – 12	11 – 8	7 – 5	4	3 – 2	1 – 0
OD1EN	Reserved				OSCDIV1	
R/W–1	R–0				R/W–0 0111	

Legend: R = Read only, R/W = Read/Write; -n = value after reset

The OSCDIV1 register controls the oscillator divider 1 for CLKOUT3. The CLKOUT3 signal does *not* go through the PLL path.

Table 36. Oscillator Divider 1 Register (OSCDIV1)

BIT #	NAME	DESCRIPTION
31:16	Reserved	Reserved. Read-only, writes have no effect.
15	OD1EN	Oscillator Divider 1 Enable. 0 – Oscillator Divider 1 Disabled. 1 – Oscillator Divider 1 Enabled (default).
14:5	Reserved	Reserved. Read-only, writes have no effect.
4:0	OSCDIV1	Oscillator Divider 1 Ratio [default is /8 (0 0111)]. 00000 = /1 10000 = /17 00001 = /2 10001 = /18 00010 = /3 10010 = /19 00011 = /4 10011 = /20 00100 = /5 10100 = /21 00101 = /6 10101 = /22 00110 = /7 10110 = /23 00111 = /8 10111 = /24 01000 = /9 11000 = /25 01001 = /10 11001 = /26 01010 = /11 11010 = /27 01011 = /12 11011 = /28 01100 = /13 11100 = /29 01101 = /14 11101 = /30 01110 = /15 11110 = /31 01111 = /16 11111 = /32

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage range, CV_{DD} (see Note 1) . . . . . –0.3 V to 1.35 V
Supply voltage range, DV_{DD} (see Note 1) . . . . . –0.3 V to 4 V
Input voltage range . . . . . –0.3 V to DV_{DD} + 0.5 V
Output voltage range . . . . . –0.3 V to DV_{DD} + 0.5 V
Operating case temperature ranges, T_C . . . . . 0°C to 90°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions‡

			MIN	NOM	MAX	UNIT
CV_{DD}	Supply voltage, Core referenced to V_{SS}		1.14	1.2	1.26	V
DV_{DD}	Supply voltage, I/O referenced to V_{SS}		3.13	3.3	3.47	V
$V_{(C-D)}$	Maximum supply voltage difference $CV_{DD} - DV_{DD}$				1.32	V
$V_{(D-C)}$	Maximum supply voltage difference $DV_{DD} - CV_{DD}$				2.75	V
V_{IH}	High-level input voltage		0.7*DV_{DD}			V
V_{IL}	Low-level input voltage				0.3*DV_{DD}	V
I_{OH}	High-level output current	All signals except TDO, EMU[5:0], ECLKOUT, CLKOUT2, CLKOUT3, SCL1, SDA1, SCL0, and SDA0			–8	mA
		TDO, EMU[5:0], ECLKOUT, CLKOUT2, and CLKOUT3			–16	mA
I_{OL}	Low-level output current	All signals except TDO, EMU[5:0], ECLKOUT, CLKOUT2, CLKOUT3, SCL1, SDA1, SCL0, and SDA0			8	mA
		TDO, EMU[5:0], ECLKOUT, CLKOUT2, and CLKOUT3			16	mA
		SCL1, SDA1, SCL0, and SDA0			6	mA
T_C	Operating case temperature		0		90	°C

‡ The core supply should be powered up at the same time as, or prior to (and powered down after), the I/O supply. Systems should be designed to ensure that neither supply is powered up for an extended period of time if the other supply is below the proper operating voltage.

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electrical characteristics over recommended ranges of supply voltage and operating case temperature† (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All signals except TDO, EMU[5:0], ECLKOUT, CLKOUT2, CLKOUT3, SCL1, SDA1, SCL0, and SDA0	DV_{DD} = MIN, I_{OH} = MAX	0.8*DV_{DD}			V
		TDO, EMU[5:0], ECLKOUT, CLKOUT2, and CLKOUT3		2.4			V
V_{OL}	Low-level output voltage	All signals except TDO, EMU[5:0], ECLKOUT, CLKOUT2, CLKOUT3, SCL1, SDA1, SCL0, and SDA0	DV_{DD} = MIN, I_{OL} = MAX			0.22*DV_{DD}	V
		TDO, EMU[5:0], ECLKOUT, CLKOUT2, and CLKOUT3				0.4	V
		SCL1, SDA1, SCL0, and SDA0	DV_{DD} = MIN, I_{OL} = 3 mA			0.4	V
			DV_{DD} = MIN, I_{OL} = 6 mA			0.6	V
I_I	Input current		V_I = V_{SS} to DV_{DD}			±150	uA
I_{OZ}	Off-state output current		V_O = DV_{DD} or 0 V			±10	uA
I_{DD2V}	Supply current, CPU + CPU memory access‡		C6713, CV_{DD} = NOM, CPU clock = 225 MHz		TBD		mA
I_{DD2V}	Supply current, peripherals‡		C6713, CV_{DD} = NOM, CPU clock = 225 MHz		TBD		mA
I_{DD3V}	Supply current, I/O pins‡		C6713, DV_{DD} = NOM, CPU clock = 225 MHz		TBD		mA
C_i	Input capacitance					TBD	pF
C_o	Output capacitance					TBD	pF

† For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in the recommended operating conditions table.
‡ Measured with average activity (50% high/50% low power). For more details on CPU, peripheral, and I/O activity, refer to the *TMS320C6000 Power Consumption Summary* application report (literature number SPRA486).

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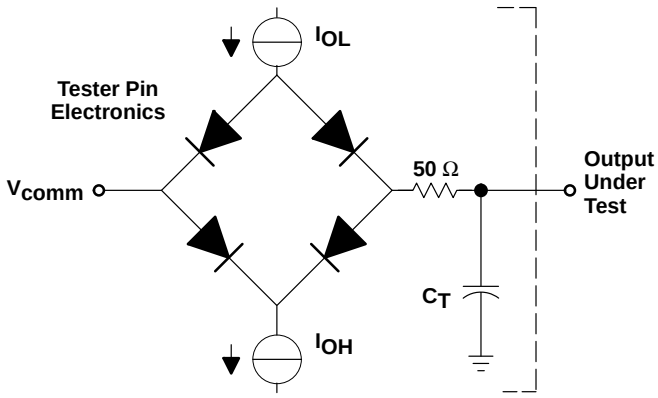
PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA
I_{OH} = 2 mA
V_{comm} = 0.8 V
C_T = 10–15-pF typical load-circuit capacitance

Figure 13. Test Load Circuit for AC Timing Measurements

signal transition levels

All input and output timing parameters are referenced to 1.5 V for both “0” and “1” logic levels.

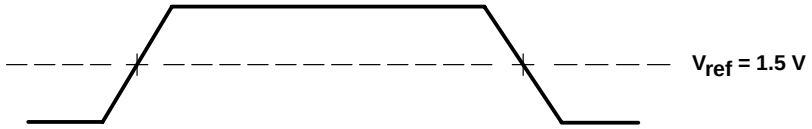


Figure 14. Input and Output Voltage Reference Levels for ac Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, and V_{OL} MAX and V_{OH} MIN for output clocks.

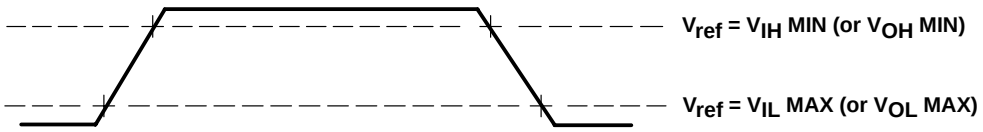


Figure 15. Rise and Fall Transition Time Voltage Reference Levels

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PARAMETER MEASUREMENT INFORMATION (CONTINUED)

timing parameters and board routing analysis

The timing parameter values specified in this data sheet do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. If needed, external logic hardware such as buffers may be used to compensate any timing differences.

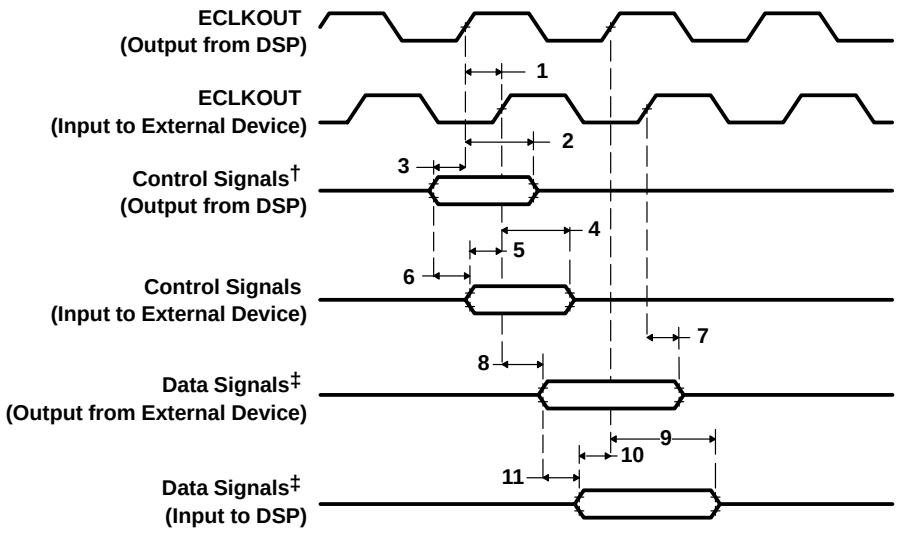
For inputs, timing is most impacted by the round-trip propagation delay from the DSP to the external device and from the external device to the DSP. This round-trip delay tends to negatively impact the input setup time margin, but also tends to improve the input hold time margins (see Table 37 and Figure 16).

Figure 16 represents a general transfer between the DSP and an external device. The figure also represents board route delays and how they are perceived by the DSP and the external device.

PARAMETER MEASUREMENT INFORMATION (CONTINUED)

Table 37. IBIS Timing Parameters Example (see Figure 16)

NO.	DESCRIPTION
1	Clock route delay
2	Minimum DSP hold time
3	Minimum DSP setup time
4	External device hold time requirement
5	External device setup time requirement
6	Control signal route delay
7	External device hold time
8	External device access time
9	DSP hold time requirement
10	DSP setup time requirement
11	Data route delay



† Control signals include data for Writes.
‡ Data signals are generated during Reads from an external device.

Figure 16. IBIS Input/Output Timings

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INPUT AND OUTPUT CLOCKS

timing requirements for CLKIN†‡ (see Figure 17)

NO.			–150 –225		UNIT
			MIN	MAX	
1	$t_{c(CLKIN)}$	Cycle time, CLKIN			ns
2	$t_{w(CLKINH)}$	Pulse duration, CLKIN high			ns
3	$t_{w(CLKINL)}$	Pulse duration, CLKIN low			ns
4	$t_{t(CLKIN)}$	Transition time, CLKIN			ns

† The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
‡ C = CLKIN cycle time in ns. For example, when CLKIN frequency is 40 MHz, use C = 25 ns.

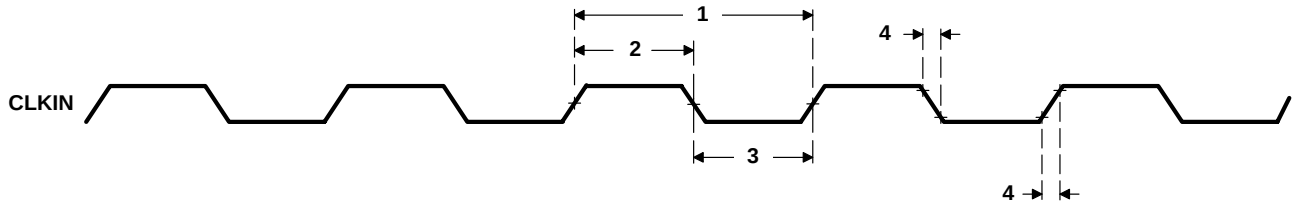

Figure 17. CLKIN Timings

switching characteristics over recommended operating conditions for CLKOUT2†‡ (see Figure 18)

NO.	PARAMETER		–150 –225		UNIT
			MIN	MAX	
1	$t_{c(CKO2)}$	Cycle time, CLKOUT2			ns
2	$t_{w(CKO2H)}$	Pulse duration, CLKOUT2 high			ns
3	$t_{w(CKO2L)}$	Pulse duration, CLKOUT2 low			ns
4	$t_{t(CKO2)}$	Transition time, CLKOUT2			ns

† The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
‡ P = 1/CPU clock frequency in ns

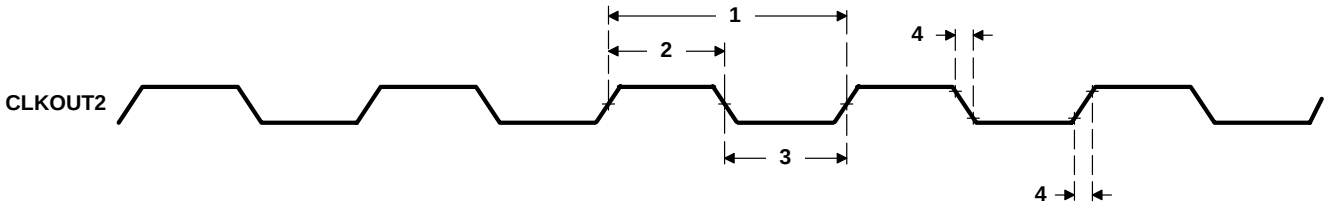

Figure 18. CLKOUT2 Timings

INPUT AND OUTPUT CLOCKS (CONTINUED)

switching characteristics over recommended operating conditions for CLKOUT3†‡ (see Figure 19)

NO.	PARAMETER		–150 –225		UNIT
			MIN	MAX	
1	$t_{c(CKO3)}$	Cycle time, CLKOUT3			ns
2	$t_{w(CKO3H)}$	Pulse duration, CLKOUT3 high			ns
3	$t_{w(CKO3L)}$	Pulse duration, CLKOUT3 low			ns
4	$t_{t(CKO3)}$	Transition time, CLKOUT3			ns

† The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
‡ P = 1/CPU clock frequency in ns

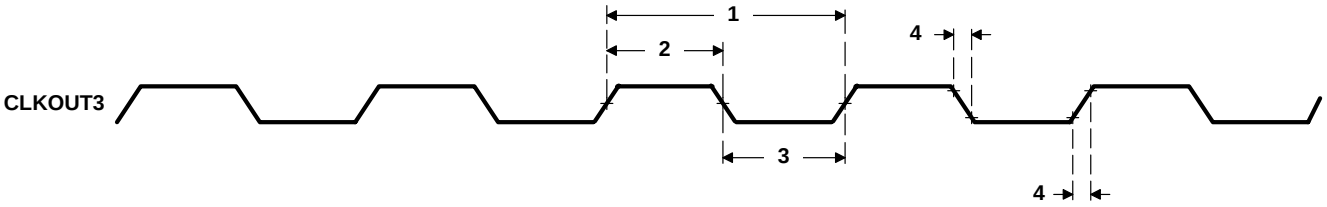

Figure 19. CLKOUT3 Timings

timing requirements for ECLKIN† (see Figure 20)

NO.			–150 –225		UNIT
			MIN	MAX	
1	$t_{c(EKI)}$	Cycle time, ECLKIN			ns
2	$t_{w(EKIH)}$	Pulse duration, ECLKIN high			ns
3	$t_{w(EKIL)}$	Pulse duration, ECLKIN low			ns
4	$t_{t(EKI)}$	Transition time, ECLKIN			ns

† The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.

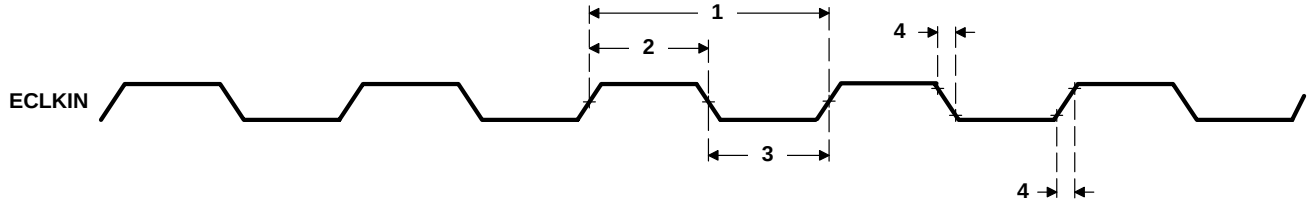

Figure 20. ECLKIN Timings

PRODUCT PREVIEW

INPUT AND OUTPUT CLOCKS (CONTINUED)

switching characteristics over recommended operating conditions for ECLKOUT‡§¶ (see Figure 21)

NO.	PARAMETER		–150 –225		UNIT
			MIN	MAX	
1	$t_{c(EKO)}$	Cycle time, ECLKOUT			
2	$t_{w(EKOH)}$	Pulse duration, ECLKOUT high			
3	$t_{w(EKOL)}$	Pulse duration, ECLKOUT low			
4	$t_{t(EKO)}$	Transition time, ECLKOUT			
5	$t_{d(EKIH-EKOH)}$	Delay time, ECLKIN high to ECLKOUT high			
6	$t_{d(EKIL-EKOL)}$	Delay time, ECLKIN low to ECLKOUT low			

‡ The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
§ E = ECLKIN period in ns
¶ EH is the high period of ECLKIN in ns and EL is the low period of ECLKIN in ns.

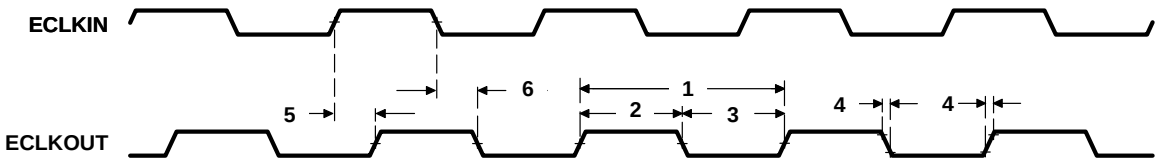

Figure 21. ECLKOUT Timings

PRODUCT PREVIEW

ASYNCHRONOUS MEMORY TIMING

timing requirements for asynchronous memory cycles†‡§ (see Figure 22–Figure 23)

NO.			–150 –225		UNIT
			MIN	MAX	
3	$t_{su(EDV-AREH)}$	Setup time, EDx valid before $\overline{ARE}$ high			
4	$t_{h(AREH-EDV)}$	Hold time, EDx valid after $\overline{ARE}$ high			
6	$t_{su(ARDY-EKOH)}$	Setup time, ARDY valid before ECLKOUT high			
7	$t_{h(EKOH-ARDY)}$	Hold time, ARDY valid after ECLKOUT high			

† To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. The ARDY signal is recognized in the cycle for which the setup and hold time is met. To use ARDY as an asynchronous input, the pulse width of the ARDY signal should be wide enough (e.g., pulse width = 2E) to ensure setup and hold time is met.

‡ RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.

§ E = ECLKOUT period in ns

switching characteristics over recommended operating conditions for asynchronous memory cycles‡§¶ (see Figure 22–Figure 23)

NO.	PARAMETER		–150 –225		UNIT
			MIN	MAX	
1	$t_{osu(SELV-AREL)}$	Output setup time, select signals valid to $\overline{ARE}$ low			
2	$t_{oh(AREH-SELIV)}$	Output hold time, $\overline{ARE}$ high to select signals invalid			
5	$t_{d(EKOH-AREV)}$	Delay time, ECLKOUT high to $\overline{ARE}$ vaild			
8	$t_{osu(SELV-AWEL)}$	Output setup time, select signals valid to $\overline{AWE}$ low			
9	$t_{oh(AWEH-SELIV)}$	Output hold time, $\overline{AWE}$ high to select signals invalid			
10	$t_{d(EKOH-AWEV)}$	Delay time, ECLKOUT high to $\overline{AWE}$ vaild			

‡ RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.

§ E = ECLKOUT period in ns

¶ Select signals include: $\overline{CEx}$, $\overline{BE[3:0]}$, EA[21:2], $\overline{AOE}$; and for writes, include ED[31:0].

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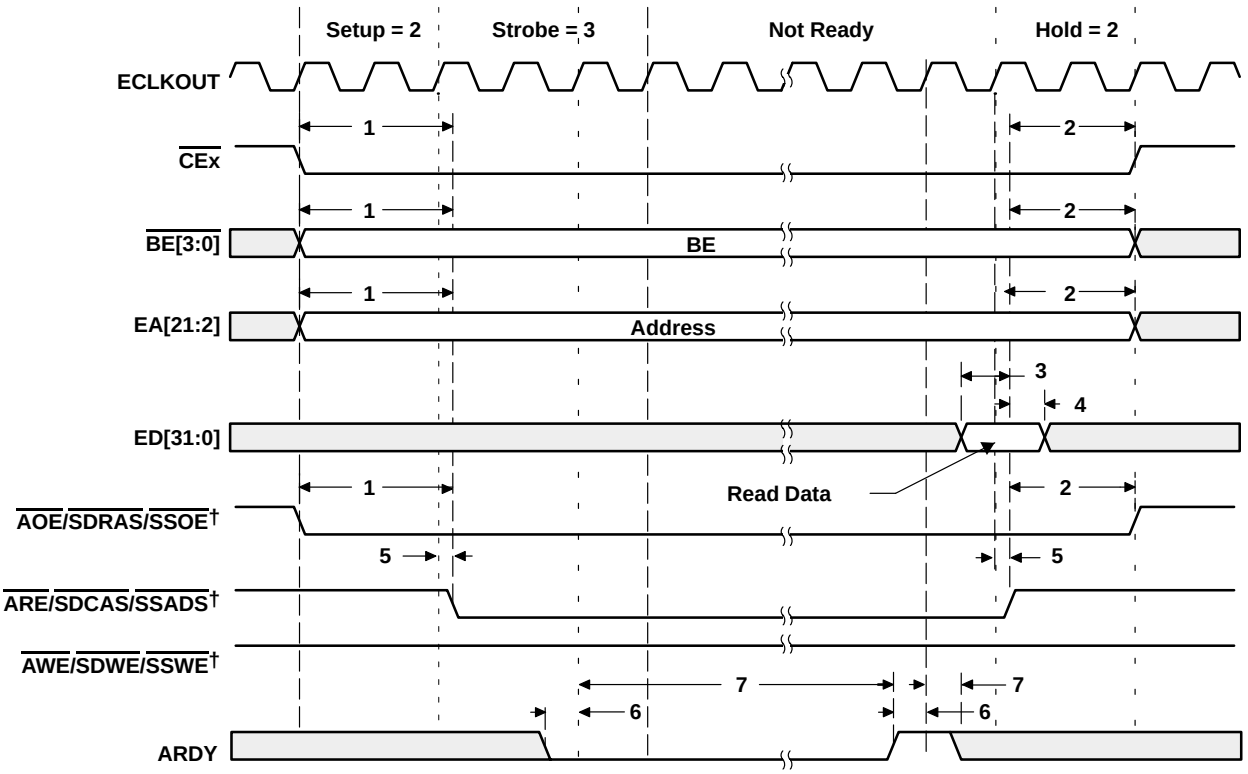
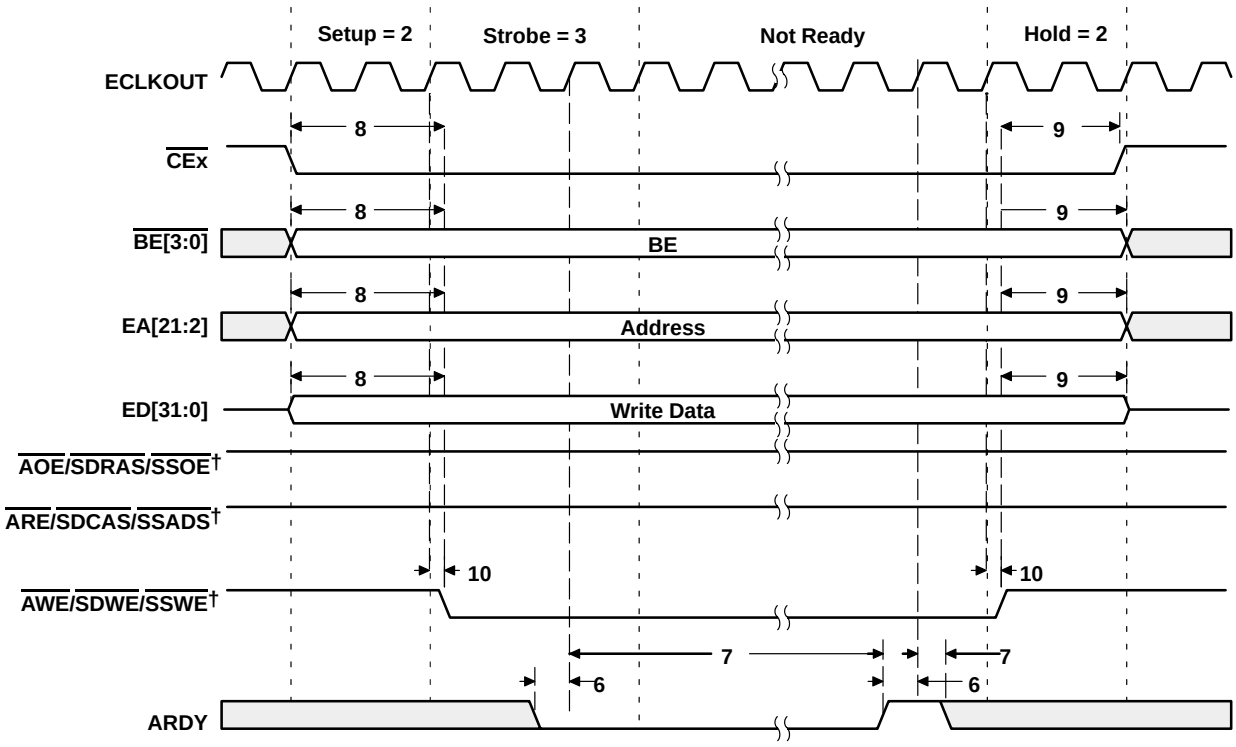
ASYNCHRONOUS MEMORY TIMING (CONTINUED)



† AOE/SDRAS/SSOE, ARE/SDCAS/SSADS, and AWE/SDWE/SSWE operate as AOE (identified under select signals), ARE, and AWE, respectively, during asynchronous memory accesses.

Figure 22. Asynchronous Memory Read Timing

ASYNCHRONOUS MEMORY TIMING (CONTINUED)



† AOE/SDRAS/SSOE, ARE/SDCAS/SSADS, and AWE/SDWE/SSWE operate as AOE (identified under select signals), ARE, and AWE, respectively, during asynchronous memory accesses.

Figure 23. Asynchronous Memory Write Timing

PRODUCT PREVIEW

SYNCHRONOUS-BURST MEMORY TIMING

timing requirements for synchronous-burst SRAM cycles† (see Figure 24)

NO.			–150 –225		UNIT
			MIN	MAX	
6	$t_{su(EDV-EKOH)}$	Setup time, read EDx valid before ECLKOUT high			
7	$t_{h(EKOH-EDV)}$	Hold time, read EDx valid after ECLKOUT high			

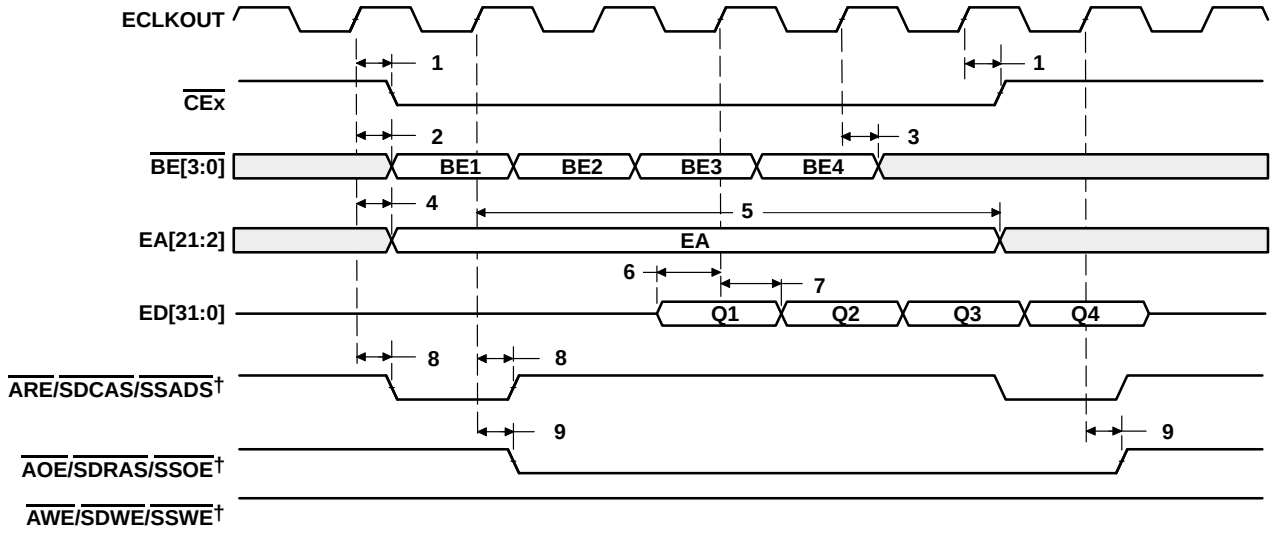
† The C6713 SBSRAM interface takes advantage of the internal burst counter in the SBSRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

switching characteristics over recommended operating conditions for synchronous-burst SRAM cycles†‡ (see Figure 24 and Figure 25)

NO.	PARAMETER		–150 –225		UNIT
			MIN	MAX	
1	$t_{d(EKOH-CEV)}$	Delay time, ECLKOUT high to $\overline{CEx}$ valid			
2	$t_{d(EKOH-BEV)}$	Delay time, ECLKOUT high to $\overline{BEx}$ valid			
3	$t_{d(EKOH-BEIV)}$	Delay time, ECLKOUT high to $\overline{BEx}$ invalid			
4	$t_{d(EKOH-EAV)}$	Delay time, ECLKOUT high to EAx valid			
5	$t_{d(EKOH-EAIV)}$	Delay time, ECLKOUT high to EAx invalid			
8	$t_{d(EKOH-ADSV)}$	Delay time, ECLKOUT high to $\overline{ARE}/\overline{SDCAS}/\overline{SSADS}$ valid			
9	$t_{d(EKOH-OEV)}$	Delay time, ECLKOUT high to, $\overline{AOE}/\overline{SDRAS}/\overline{SSOE}$ valid			
10	$t_{d(EKOH-EDV)}$	Delay time, ECLKOUT high to $\overline{EDx}$ valid			
11	$t_{d(EKOH-EDIV)}$	Delay time, ECLKOUT high to $\overline{EDx}$ invalid			
12	$t_{d(EKOH-WEV)}$	Delay time, ECLKOUT high to $\overline{AWE}/\overline{SDWE}/\overline{SSWE}$ valid			

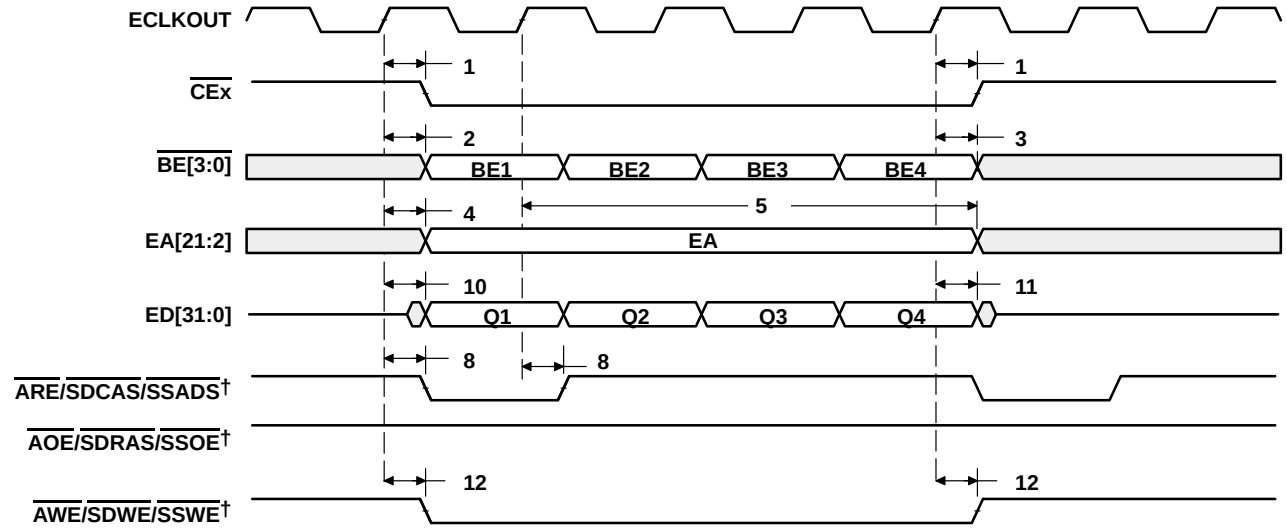
† The C6713 SBSRAM interface takes advantage of the internal burst counter in the SBSRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.
‡ $\overline{ARE}/\overline{SDCAS}/\overline{SSADS}$, $\overline{AOE}/\overline{SDRAS}/\overline{SSOE}$, and $\overline{AWE}/\overline{SDWE}/\overline{SSWE}$ operate as $\overline{SSADS}$, $\overline{SSOE}$, and $\overline{SSWE}$, respectively, during SBSRAM accesses.

SYNCHRONOUS-BURST MEMORY TIMING (CONTINUED)



† ARE/SDCAS/SSADS, AOE/SDRAS/SSOE, and AWE/SDWE/SSWE operate as SSADS, SSOE, and SSWE, respectively, during SBSRAM accesses.

Figure 24. SBSRAM Read Timing



† ARE/SDCAS/SSADS, AOE/SDRAS/SSOE, and AWE/SDWE/SSWE operate as SSADS, SSOE, and SSWE, respectively, during SBSRAM accesses.

Figure 25. SBSRAM Write Timing

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SYNCHRONOUS DRAM TIMING

timing requirements for synchronous DRAM cycles† (see Figure 26)

NO.			–150 –225		UNIT
			MIN	MAX	
6	$t_{su(EDV-EKOH)}$	Setup time, read EDx valid before ECLKOUT high			
7	$t_{h(EKOH-EDV)}$	Hold time, read EDx valid after ECLKOUT high			

† The C6713 SDRAM interface takes advantage of the internal burst counter in the SDRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

switching characteristics over recommended operating conditions for synchronous DRAM cycles†‡ (see Figure 26–Figure 32)

NO.	PARAMETER		–150 –225		UNIT
			MIN	MAX	
1	$t_{d(EKOH-CEV)}$	Delay time, ECLKOUT high to $\overline{CEx}$ valid			
2	$t_{d(EKOH-BEV)}$	Delay time, ECLKOUT high to $\overline{BEx}$ valid			
3	$t_{d(EKOH-BEIV)}$	Delay time, ECLKOUT high to $\overline{BEx}$ invalid			
4	$t_{d(EKOH-EAV)}$	Delay time, ECLKOUT high to EAx valid			
5	$t_{d(EKOH-EAIV)}$	Delay time, ECLKOUT high to EAx invalid			
8	$t_{d(EKOH-CASV)}$	Delay time, ECLKOUT high to $\overline{ARE}/\overline{SDCAS}/\overline{SSADS}$ valid			
9	$t_{d(EKOH-EDV)}$	Delay time, ECLKOUT high to $\overline{EDx}$ valid			
10	$t_{d(EKOH-EDIV)}$	Delay time, ECLKOUT high to $\overline{EDx}$ invalid			
11	$t_{d(EKOH-WEV)}$	Delay time, ECLKOUT high to $\overline{AWE}/\overline{SDWE}/\overline{SSWE}$ valid			
12	$t_{d(EKOH-RAS)}$	Delay time, ECLKOUT high to, $\overline{AOE}/\overline{SDRAS}/\overline{SSOE}$ valid			

† The C6713 SDRAM interface takes advantage of the internal burst counter in the SDRAM. Accesses default to incrementing 4-word bursts, but random bursts and decrementing bursts are done by interrupting bursts in progress. All burst types can sustain continuous data flow.

‡ $\overline{ARE}/\overline{SDCAS}/\overline{SSADS}$, $\overline{AWE}/\overline{SDWE}/\overline{SSWE}$, and $\overline{AOE}/\overline{SDRAS}/\overline{SSOE}$ operate as $\overline{SDCAS}$, $\overline{SDWE}$, and $\overline{SDRAS}$, respectively, during SDRAM accesses.

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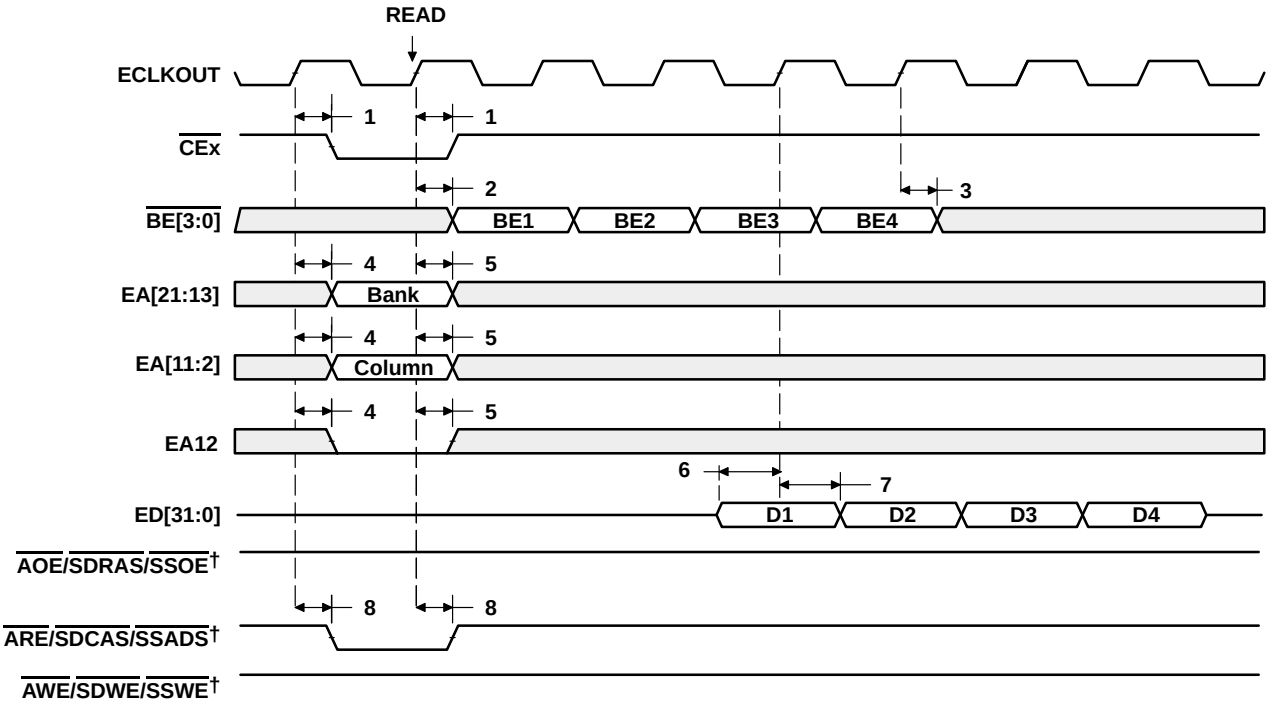
SYNCHRONOUS DRAM TIMING (CONTINUED)



† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

Figure 26. SDRAM Read Command (CAS Latency 3)

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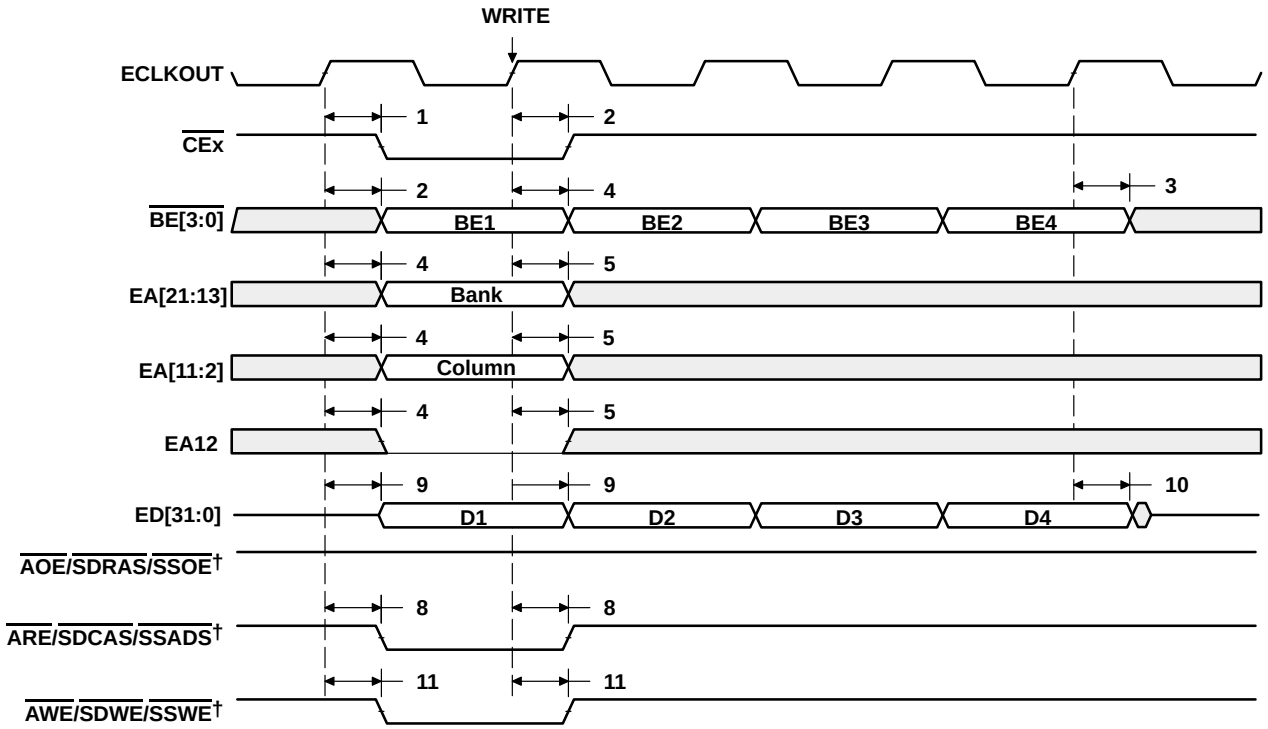
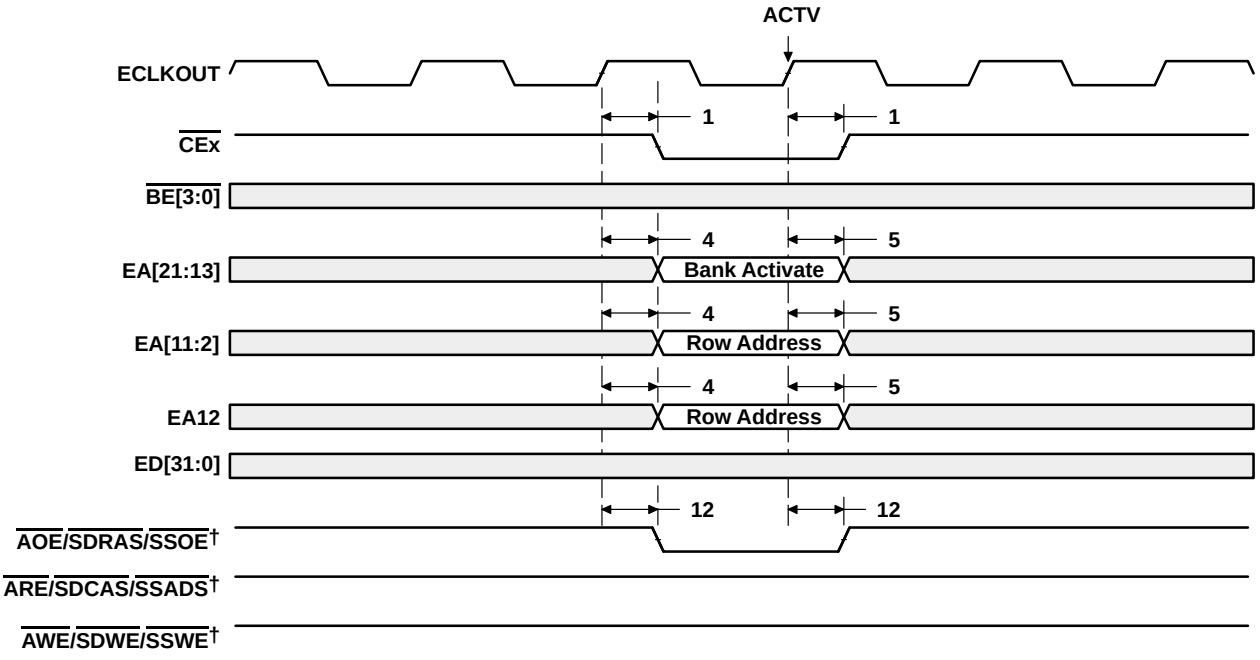
SYNCHRONOUS DRAM TIMING (CONTINUED)



† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

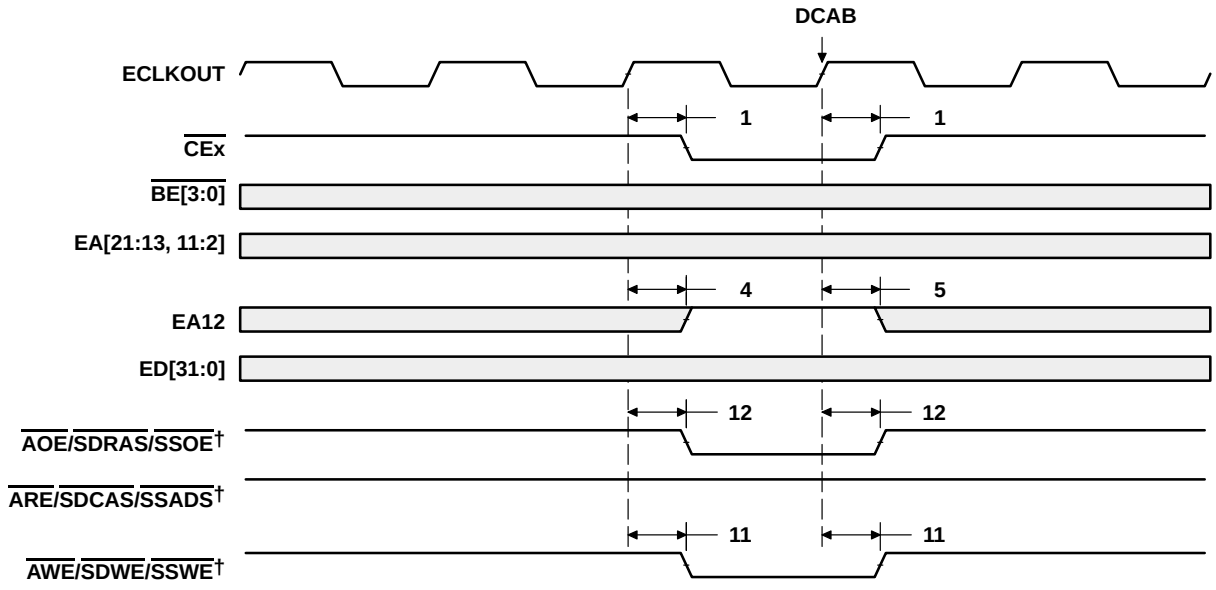
Figure 27. SDRAM Write Command

SYNCHRONOUS DRAM TIMING (CONTINUED)



† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

Figure 28. SDRAM ACTV Command

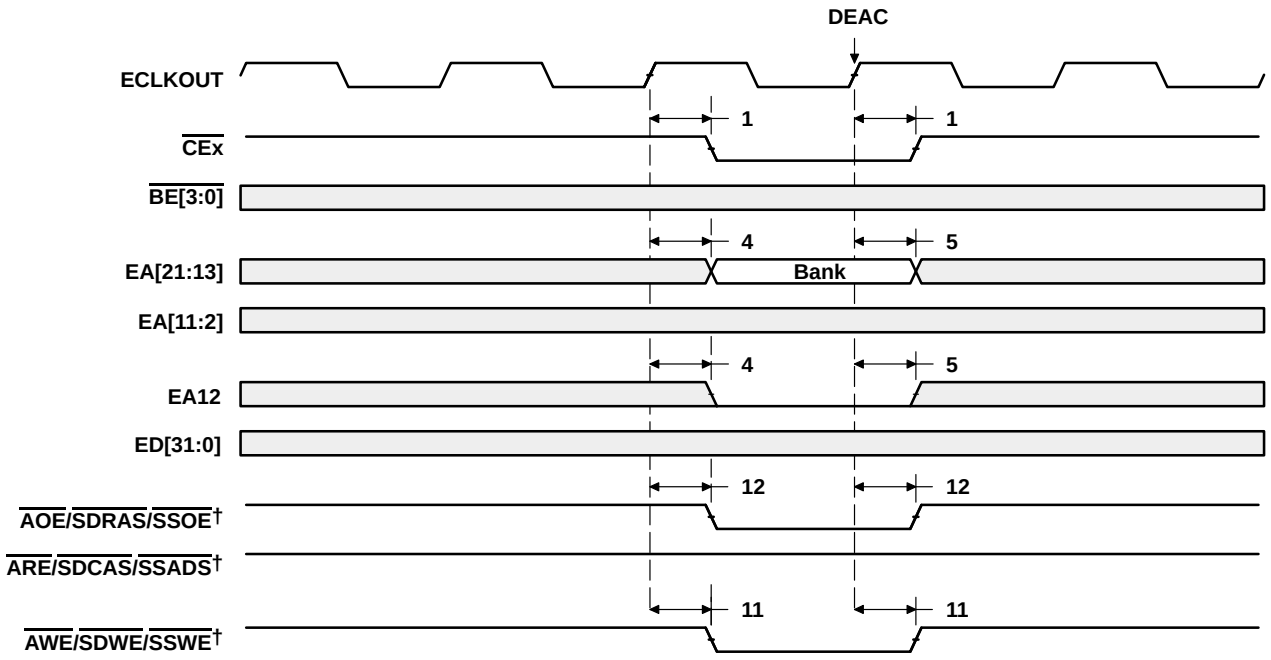


† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

Figure 29. SDRAM DCAB Command

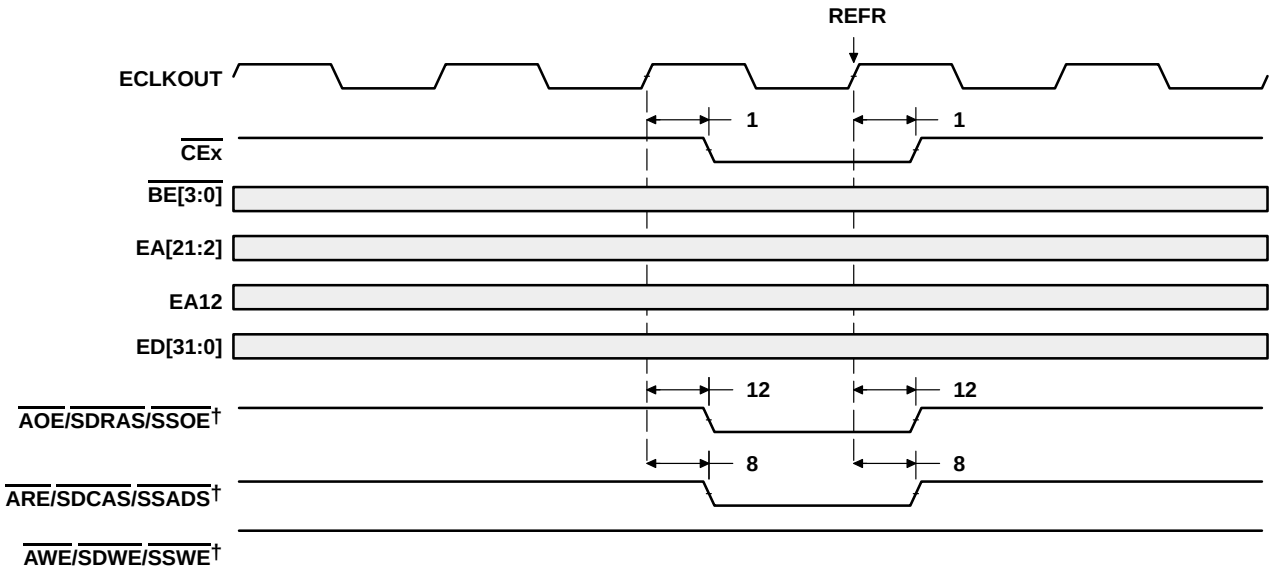
PRODUCT PREVIEW

SYNCHRONOUS DRAM TIMING (CONTINUED)



† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

Figure 30. SDRAM DEAC Command



† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

Figure 31. SDRAM REFR Command

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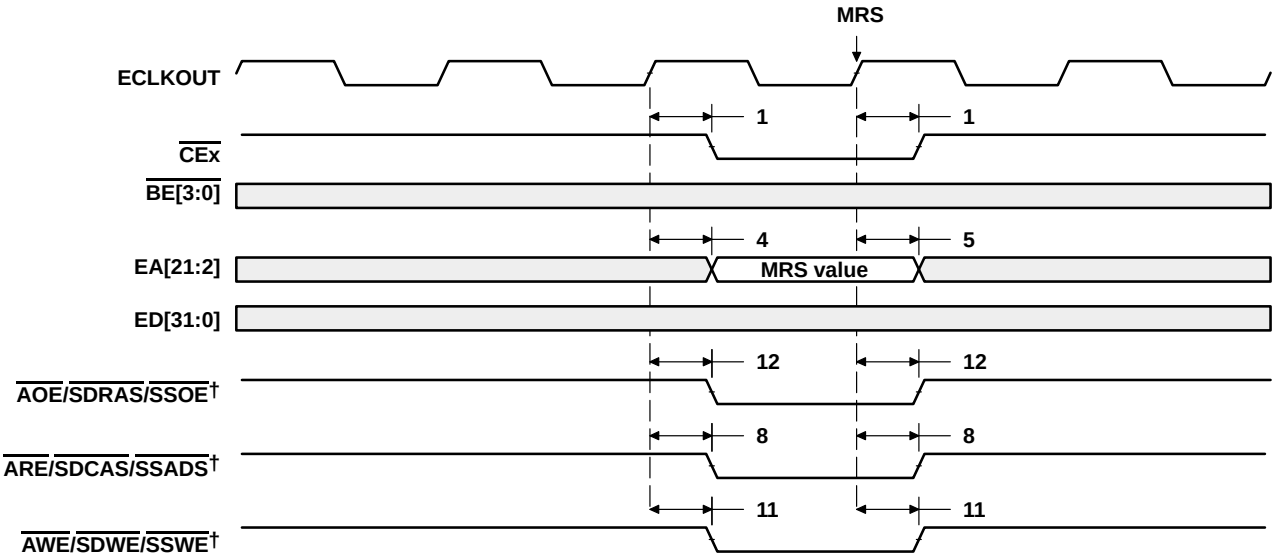
SYNCHRONOUS DRAM TIMING (CONTINUED)



† ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE operate as SDCAS, SDWE, and SDRAS, respectively, during SDRAM accesses.

Figure 32. SDRAM MRS Command

HOLD/HOLDA TIMING

timing requirements for the HOLD/HOLDA cycles† (see Figure 33)

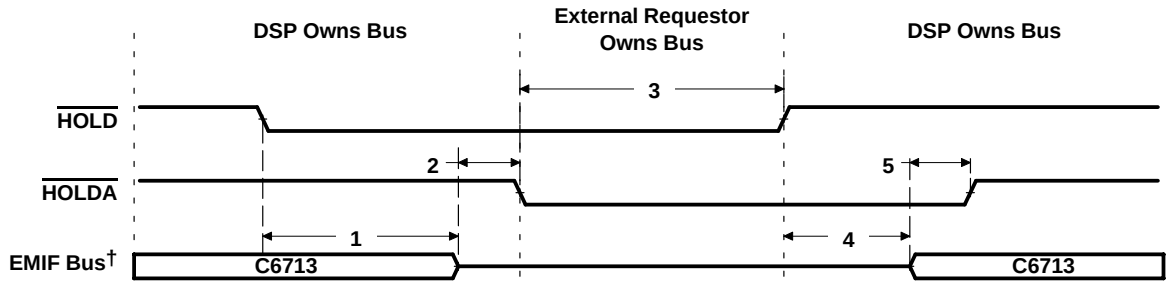
NO.		–150 –225		UNIT
		MIN	MAX	
3	$t_{oh(HOLDAL-HOLDL)}$ Output hold time, HOLD low after HOLDA low			

† E = ECLKIN period in ns

switching characteristics over recommended operating conditions for the HOLD/HOLDA cycles†‡ (see Figure 33)

NO.	PARAMETER		–150 –225		UNIT
			MIN	MAX	
1	$t_{d(HOLDL-EMHZ)}$	Delay time, HOLD low to EMIF Bus high impedance			
2	$t_{d(EMHZ-HOLDAL)}$	Delay time, EMIF Bus high impedance to HOLDA low			
4	$t_{d(HOLDH-EMLZ)}$	Delay time, HOLD high to EMIF Bus low impedance			
5	$t_{d(EMLZ-HOLDAH)}$	Delay time, EMIF Bus low impedance to HOLDA high			

† E = ECLKIN period in ns
‡ EMIF Bus consists of CE[3:0], BE[3:0], ED[31:0], EA[21:2], ARE/SDCAS/SSADS, AOE/SDRAS/SSOE, and AWE/SDWE/SSWE.
§ All pending EMIF transactions are allowed to complete before HOLDA is asserted. If no bus transactions are occurring, then the minimum delay time can be achieved. Also, bus hold can be indefinitely delayed by setting NOHOLD = 1.



† EMIF Bus consists of CE[3:0], BE[3:0], ED[31:0], EA[21:2], ARE/SDCAS/SSADS, AOE/SDRAS/SSOE, and AWE/SDWE/SSWE.

Figure 33. HOLD/HOLDA Timing

BUSREQ TIMING

switching characteristics over recommended operating conditions for the BUSREQ cycles (see Figure 34)

NO.	PARAMETER		–150 –225		UNIT
			MIN	MAX	
1	$t_{d(EKOH-BUSRV)}$	Delay time, ECLKOUT high to BUSREQ valid			

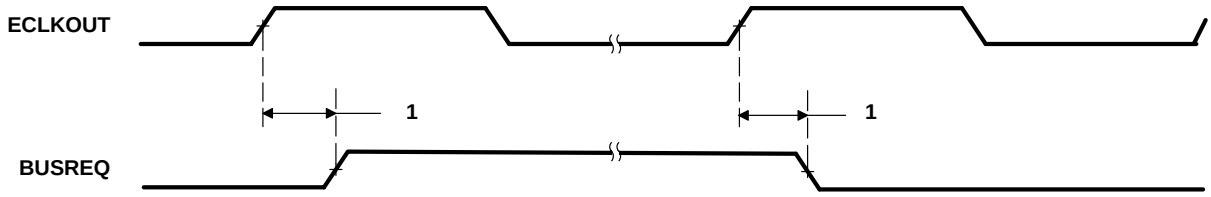


Figure 34. BUSREQ Timing

RESET TIMING

timing requirements for reset† (see Figure 35)

NO.			–150 –225		UNIT
			MIN	MAX	
1	$t_{w(RST)}$	Width of the RESET pulse (PLL stable)‡			
		Width of the RESET pulse (PLL needs to sync up)§			
14	$t_{su(HD)}$	Setup time, HD boot configuration bits valid before RESET high¶			
15	$t_{h(HD)}$	Hold time, HD boot configuration bits valid after RESET high¶			

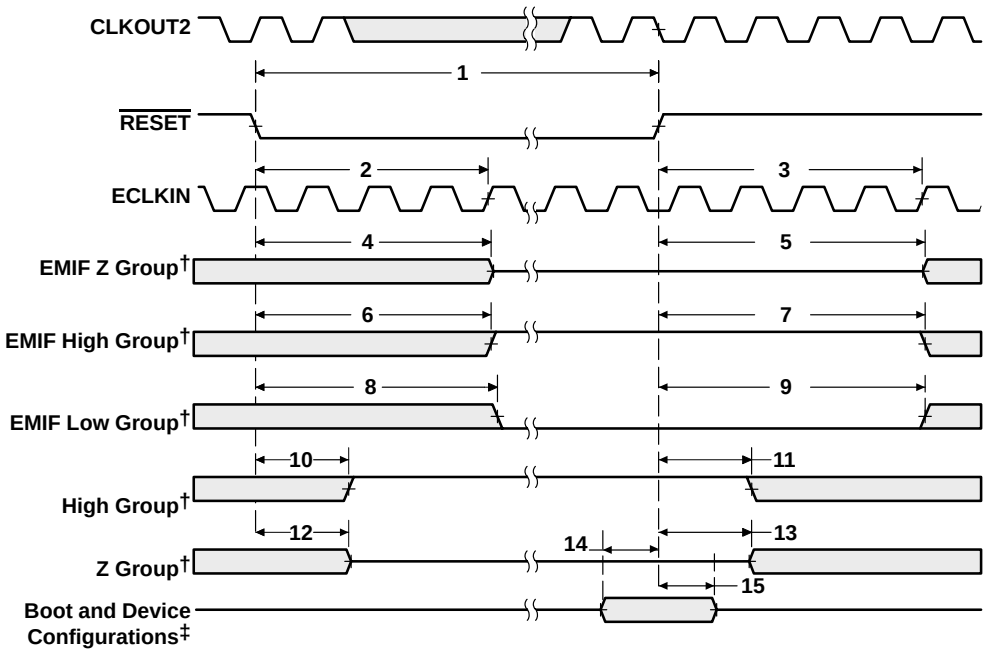
† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ This parameter applies to CLKMODE x1 when CLKIN is stable, and applies to CLKMODE x4 when CLKIN and PLL are stable.
§ This parameter applies to CLKMODE x4 only (it does not apply to CLKMODE x1). The RESET signal is not connected internally to the clock PLL circuit. The PLL, however, may need up to 250 µs to stabilize following device power up or after PLL configuration has been changed. During that time, RESET must be asserted to ensure proper device operation. See the *clock generator, oscillator, and PLL* section for PLL lock times.
¶ Boot and device configurations consist of: HD[15:12, 8, 4:3].

switching characteristics over recommended operating conditions during reset†#‖ (see Figure 35)

NO.	PARAMETER		–150 –225		UNIT
			MIN	MAX	
2	$t_{d(RSTL-ECKI)}$	Delay time, RESET low to ECLKIN synchronized internally			
3	$t_{d(RSTH-ECKI)}$	Delay time, RESET high to ECLKIN synchronized internally			
4	$t_{d(RSTL-EMIFZHZ)}$	Delay time, RESET low to EMIF Z group high impedance			
5	$t_{d(RSTH-EMIFZV)}$	Delay time, RESET high to EMIF Z group valid			
6	$t_{d(RSTL-EMIFHIV)}$	Delay time, RESET low to EMIF high group invalid			
7	$t_{d(RSTH-EMIFHV)}$	Delay time, RESET high to EMIF high group valid			
8	$t_{d(RSTL-EMIFLIV)}$	Delay time, RESET low to EMIF low group invalid			
9	$t_{d(RSTH-EMIFLV)}$	Delay time, RESET high to EMIF low group valid			
10	$t_{d(RSTL-HIGHIV)}$	Delay time, RESET low to high group invalid			
11	$t_{d(RSTH-HIGHV)}$	Delay time, RESET high to high group valid			
12	$t_{d(RSTL-ZHZ)}$	Delay time, RESET low to Z group high impedance			
13	$t_{d(RSTH-ZV)}$	Delay time, RESET high to Z group valid			

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
# E = ECLKIN period in ns
‖ EMIF Z group consists of: EA[21:2], ED[31:0], CE[3:0], BE[3:0], ARE/SDCAS/SSADS, AWE/SDWE/SSWE, and AOE/SDRAS/SSOE
EMIF high group consists of: HOLDA
EMIF low group consists of: BUSREQ
High group consists of: HRDY/ACLKR1 and HINT/GP[1]
Z group consists of: HD[11:9, 7:5, 2:0], CLKX0, CLKX1, FSX0, FSX1, DX0, DX1, CLKR0, CLKR1, FSR0, FSR1, TOUT0, and TOUT1.

RESET TIMING (CONTINUED)



† EMIF Z group consists of: EA[21:2], ED[31:0], $\overline{\text{CE}}$[3:0], $\overline{\text{BE}}$[3:0], $\overline{\text{ARE}}$/SDCAS/SSADS, $\overline{\text{AWE}}$/SDWE/SSWE, and $\overline{\text{AOE}}$/SDRAS/SSOE
EMIF high group consists of: $\overline{\text{HOLDA}}$
EMIF low group consists of: $\overline{\text{BUSREQ}}$
High group consists of: $\overline{\text{HRDY}}$/ACLKR1 and $\overline{\text{HINT}}$/GP[1]
Z group consists of: HD[11:9, 7:5, 2:0], CLKX0/ACLKX0, CLKX1/AMUTE0, FSX0/AFSX0, FSX1, DX0/AXR0[1], DX1/AXR0[5], CLKR0/ACLKR0, CLKR1/AXR0[6], FSR0/AFSR0, FSR1/AXR0[7], TOUT0/AXR0[2], and TOUT1/AXR0[4].

‡ Boot and device configurations consist of: HD[15:12, 8, 4:3].

Figure 35. Reset Timing

EXTERNAL INTERRUPT TIMING

timing requirements for external interrupts† (see Figure 36)

NO.			–150 –225		UNIT
			MIN	MAX	
1	$t_{w(ILOW)}$	Width of the interrupt pulse low			
2	$t_{w(IHIGH)}$	Width of the interrupt pulse high			

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

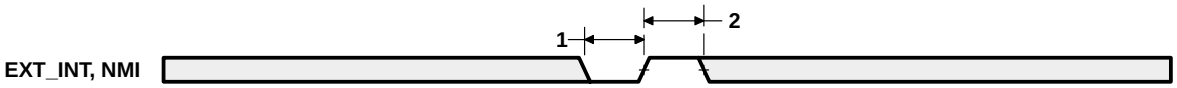


Figure 36. External/NMI Interrupt Timing

MULTICHANNEL AUDIO SERIAL PORT (McASP) TIMING

timing requirements for McASP†‡ (see Figure 37 and Figure 38)

NO.				–150 –225		UNIT
				MIN	MAX	
1	$t_{c(AHCKRX)}$	Cycle time, AHCLKR/X				
2	$t_{w(AHCKRX)}$	Pulse duration, AHCLKR/X high or low				
3	$t_{c(CKRX)}$	Cycle time, ACLKR/X	ACLKR/X int			
			ACLKR/X ext			
4	$t_{w(CKRX)}$	Pulse duration, ACLKR/X high or low	ACLKR/X int			
			ACLKR/X ext			
5	$t_{su(FRXC-KRX)}$	Setup time, AFSR/X input valid before ACLKR/X latches data	ACLKR/X int			
			ACLKR/X ext			
6	$t_{h(CKRX-FRX)}$	Hold time, AFSR/X input valid after ACLKR/X latches data	ACLKR/X int			
			ACLKR/X ext			
7	$t_{su(AXR-CKRX)}$	Setup time, AXR input valid before ACLKR/X latches data	ACLKR/X int			
			ACLKR/X ext			
8	$t_{h(CKRX-AXR)}$	Hold time, AXR input valid after ACLKR/X latches data	ACLKR/X int			
			ACLKR/X ext			

switching characteristics over recommended operating conditions for McASP (see Figure 37 and Figure 38)

NO.	PARAMETER			–150 –225		UNIT
				MIN	MAX	
9	$t_{c(AHCKRX)}$	Cycle time, AHCLKR/X				
10	$t_{w(AHCKRX)}$	Pulse duration, AHCLKR/X high or low				
11	$t_{c(CKRX)}$	Cycle time, ACLKR/X	ACLKR/X int			
			ACLKR/X ext			
12	$t_{w(CKRX)}$	Pulse duration, ACLKR/X high or low	ACLKR/X int			
			ACLKR/X ext			
13	$t_{d(CKRX-FRX)}$	Delay time, ACLKR/X transmit edge to AFSX/R output valid	ACLKR/X int			
			ACLKR/X ext			
14	$t_{d(CKRX-AXR1V)}$	Delay time, ACLKR/X transmit edge to AXR first bit valid	ACLKR/X int			
			ACLKR/X ext			
15	$t_{d(CKRX-AXRV)}$	Delay time, ACLKR/X transmit edge to AXR output valid	ACLKR/X int			
			ACLKR/X ext			
16	$t_{dis(CKRX–AXRHZ)}$	Disable time, AXR high impedance following last data bit from ACLKR/X transmit edge	ACLKR/X int			
			ACLKR/X ext			

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MULTICHANNEL AUDIO SERIAL PORT (McASP) TIMING (CONTINUED)

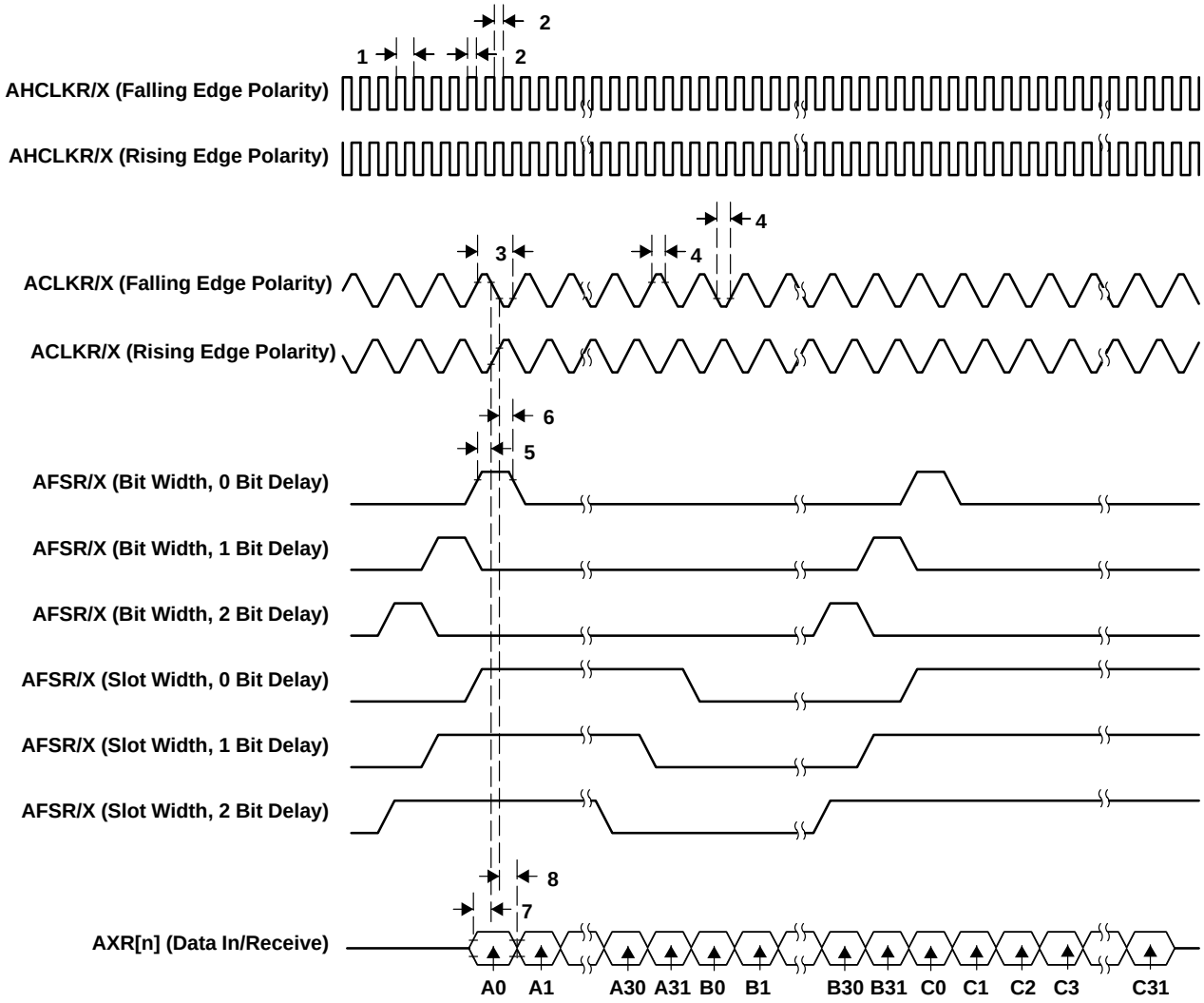


Figure 37. McASP Input Timings

MULTICHANNEL AUDIO SERIAL PORT (McASP) TIMING (CONTINUED)

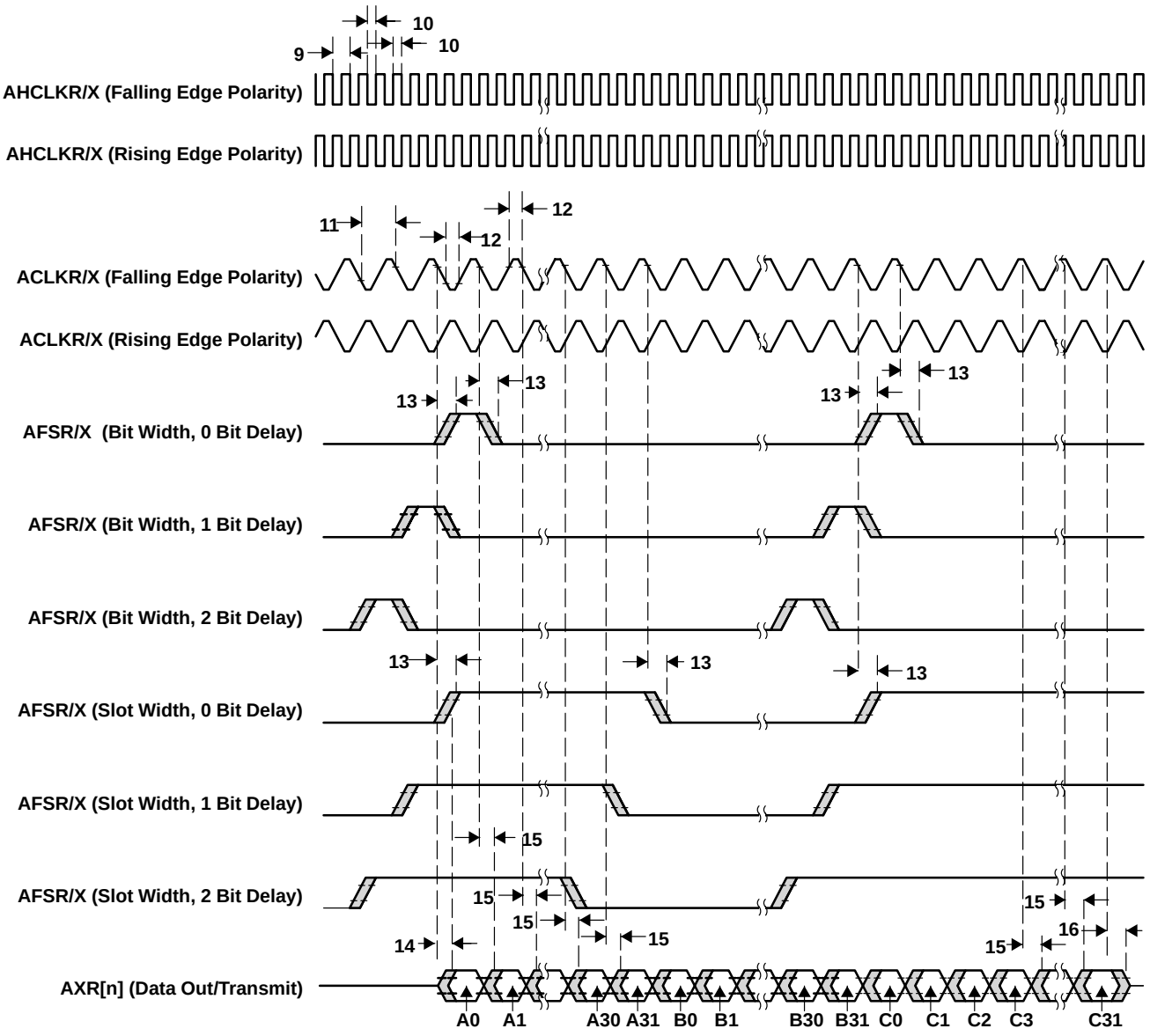


Figure 38. McASP Output Timings

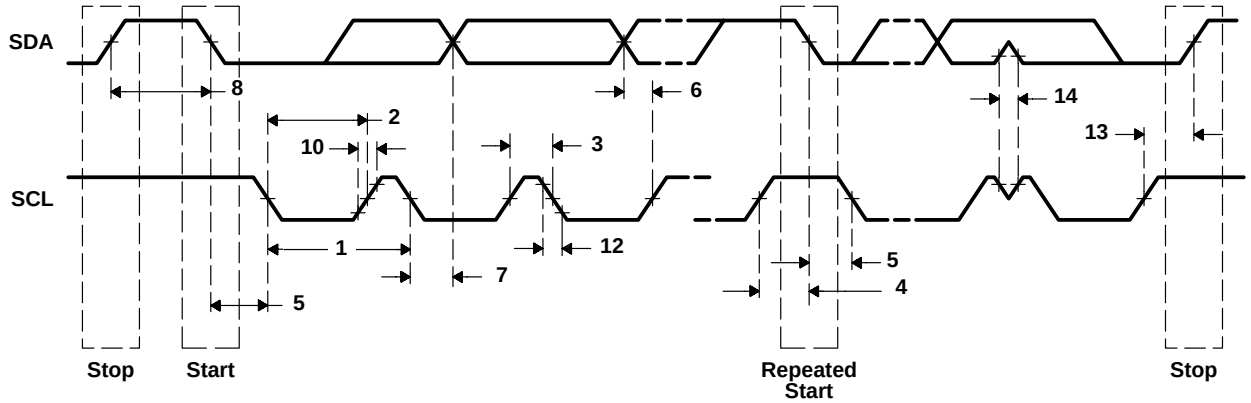
PRODUCT PREVIEW

INTER-INTEGRATED CIRCUITS (I2C) TIMING

switching characteristics for I2C timings† (see Figure 39)

NO.				–150 –225				UNIT
				STANDARD MODE		FAST MODE		
				MIN	MAX	MIN	MAX	
1	$t_{c(SCL)}$	Cycle time, SCL						
2	$t_{w(SCLL)}$	Pulse duration, SCL low						
3	$t_{w(SCLH)}$	Pulse duration, SCL high						
4	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)						
5	$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a repeated START condition)						
6	$t_{su(SDA-SDLH)}$	Setup time, SDA valid before SCL high						
7	$t_{h(SDA-SDLL)}$	Hold time, SDA valid after SCL low	For CBUS compatible masters					
			For I2C bus devices					
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions						
9	$t_{r(SDA)}$	Rise time, SDA						
10	$t_{r(SCL)}$	Rise time, SCL						
11	$t_{f(SDA)}$	Fall time, SDA						
12	$t_{f(SCL)}$	Fall time, SCL						
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)						
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)						
15	C_b§	Capacitive load for each bus line						

† The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
‡ The maximum $t_{h(SCLL-SDAL)}$ has only to be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the SCL signal.
§ C_b = The total capacitance of one bus line in pF.



NOTES: A. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
B. The maximum $t_{h(SCLL–SDAL)}$ has only to be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the SCL signal.
C. A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA–SDLH)}$ • 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA–SDLH)}$ = 1000 + 250 = 1250 ns (according to the standard-mode I2C-bus specification) before the SCL line is released.
D. C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed

Figure 39. I2C Timings

HOST-PORT INTERFACE TIMING

timing requirements for host-port interface cycles†‡ (see Figure 40, Figure 41, Figure 42, and Figure 43)

NO.			–150 –225		UNIT
			MIN	MAX	
1	$t_{su(SELV-HSTBL)}$	Setup time, select signals§ valid before $\overline{\text{HSTROBE}}$ low			
2	$t_{h(HSTBL-SELV)}$	Hold time, select signals§ valid after $\overline{\text{HSTROBE}}$ low			
3	$t_{w(HSTBL)}$	Pulse duration, $\overline{\text{HSTROBE}}$ low			
4	$t_{w(HSTBH)}$	Pulse duration, $\overline{\text{HSTROBE}}$ high between consecutive accesses			
10	$t_{su(SELV-HASL)}$	Setup time, select signals§ valid before $\overline{\text{HAS}}$ low			
11	$t_{h(HASL-SELV)}$	Hold time, select signals§ valid after $\overline{\text{HAS}}$ low			
12	$t_{su(HDV-HSTBH)}$	Setup time, host data valid before $\overline{\text{HSTROBE}}$ high			
13	$t_{h(HSTBH-HDV)}$	Hold time, host data valid after $\overline{\text{HSTROBE}}$ high			
14	$t_{h(HRDYL-HSTBL)}$	Hold time, $\overline{\text{HSTROBE}}$ low after $\overline{\text{HRDY}}$ low. $\overline{\text{HSTROBE}}$ should not be inactivated until $\overline{\text{HRDY}}$ is active (low); otherwise, HPI writes will not complete properly.			
18	$t_{su(HASL-HSTBL)}$	Setup time, $\overline{\text{HAS}}$ low before $\overline{\text{HSTROBE}}$ low			
19	$t_{h(HSTBL-HASL)}$	Hold time, $\overline{\text{HAS}}$ low after $\overline{\text{HSTROBE}}$ low			

† $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
§ Select signals include: HCNTL[1:0], HR/$\overline{\text{W}}$, and HHWIL.

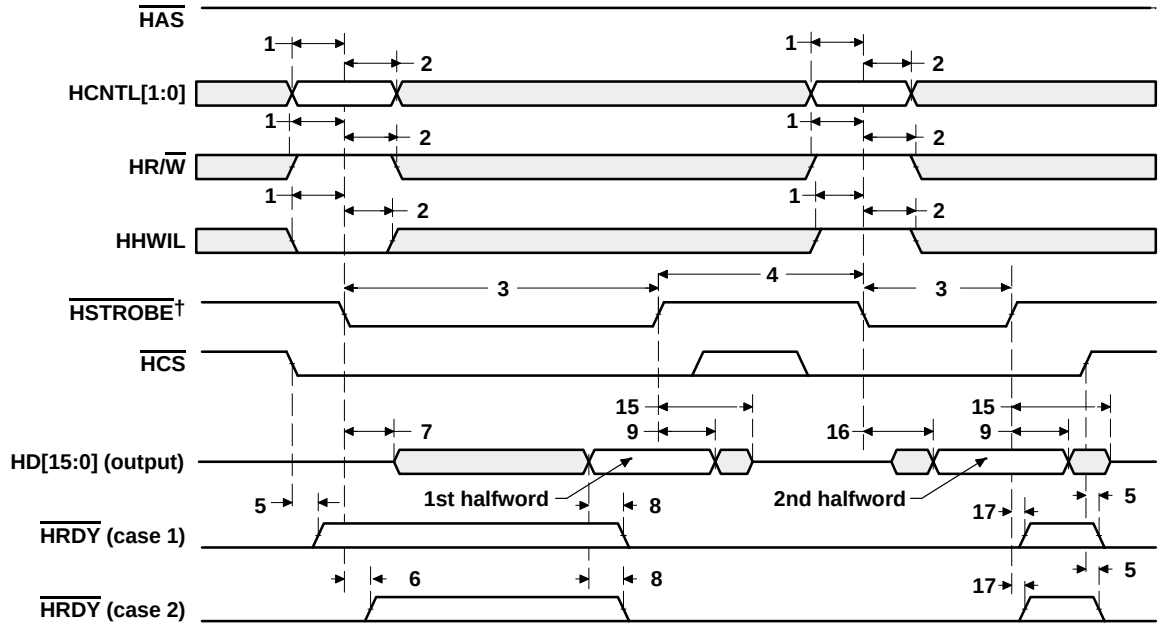
switching characteristics over recommended operating conditions during host-port interface cycles†‡ (see Figure 40, Figure 41, Figure 42, and Figure 43)

NO.	PARAMETER		–150 –225		UNIT
			MIN	MAX	
5	$t_{d(HCS-HRDY)}$	Delay time, $\overline{\text{HCS}}$ to $\overline{\text{HRDY}}$¶			
6	$t_{d(HSTBL-HRDYH)}$	Delay time, $\overline{\text{HSTROBE}}$ low to $\overline{\text{HRDY}}$ high#			
7	$t_{d(HSTBL-HDLZ)}$	Delay time, $\overline{\text{HSTROBE}}$ low to HD low impedance for an HPI read			
8	$t_{d(HDV-HRDYL)}$	Delay time, HD valid to $\overline{\text{HRDY}}$ low			
9	$t_{oh(HSTBH-HDV)}$	Output hold time, HD valid after $\overline{\text{HSTROBE}}$ high			
15	$t_{d(HSTBH-HDHZ)}$	Delay time, $\overline{\text{HSTROBE}}$ high to HD high impedance			
16	$t_{d(HSTBL-HDV)}$	Delay time, $\overline{\text{HSTROBE}}$ low to HD valid			
17	$t_{d(HSTBH-HRDYH)}$	Delay time, $\overline{\text{HSTROBE}}$ high to $\overline{\text{HRDY}}$ high‖			
20	$t_{d(HASL-HRDYH)}$	Delay time, $\overline{\text{HAS}}$ low to $\overline{\text{HRDY}}$ high			

† $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
¶ $\overline{\text{HCS}}$ enables $\overline{\text{HRDY}}$, and $\overline{\text{HRDY}}$ is always low when $\overline{\text{HCS}}$ is high. The case where $\overline{\text{HRDY}}$ goes high when $\overline{\text{HCS}}$ falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.
# This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of $\overline{\text{HSTROBE}}$, the HPI sends the request to the EDMA internal address generation hardware, and $\overline{\text{HRDY}}$ remains high until the EDMA internal address generation hardware loads the requested data into HPID.
‖ This parameter is used after the second half-word of an HPID write or autoincrement read. $\overline{\text{HRDY}}$ remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the $\overline{\text{HRDY}}$ signal.

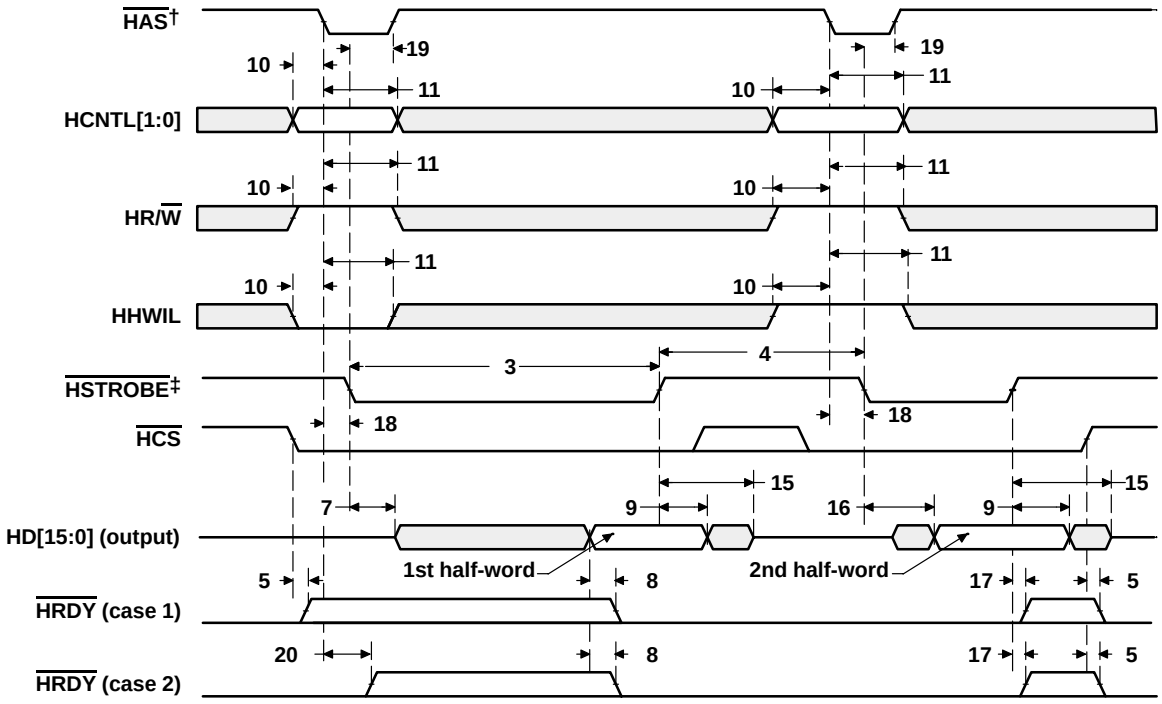
PRODUCT PREVIEW

HOST-PORT INTERFACE TIMING (CONTINUED)



† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

Figure 40. HPI Read Timing (HAS Not Used, Tied High)



† For correct operation, strobe the HAS signal only once per HSTROBE active cycle.
‡ HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

Figure 41. HPI Read Timing (HAS Used)

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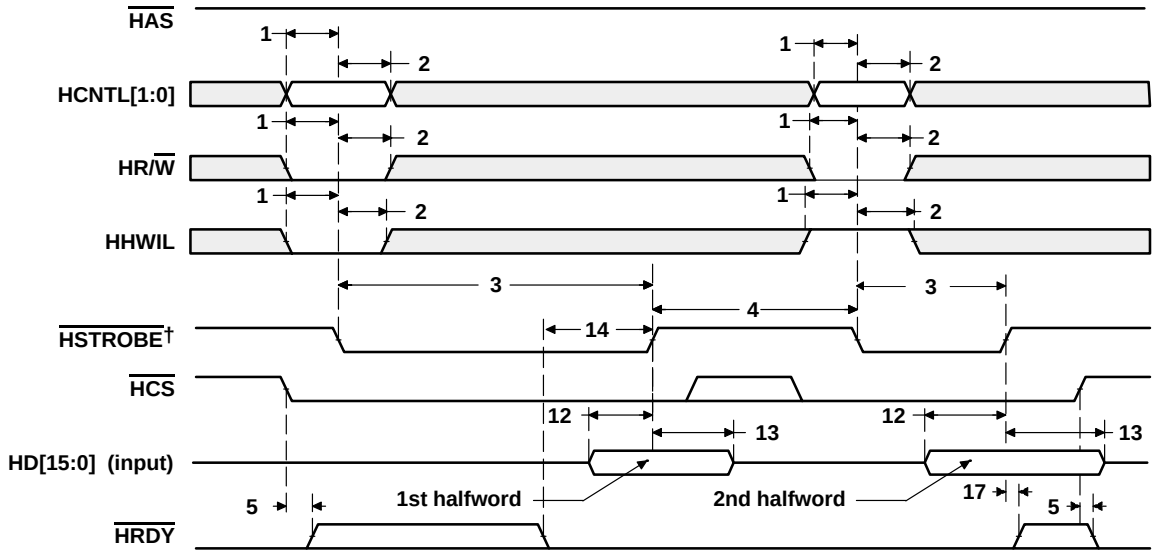
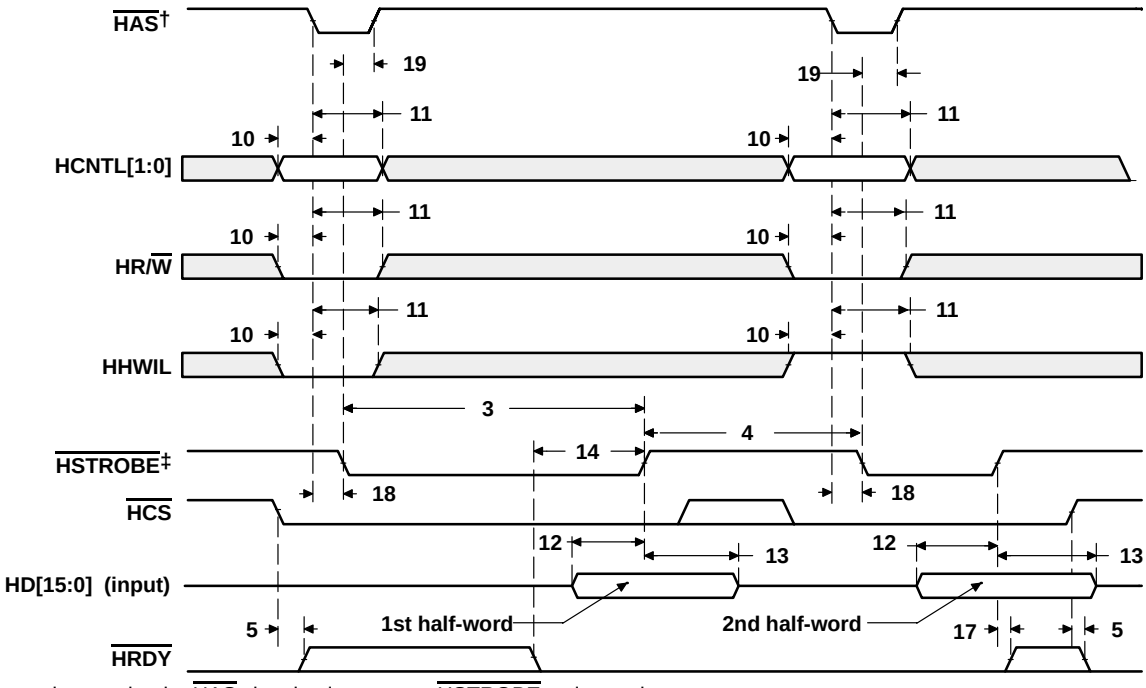
HOST-PORT INTERFACE TIMING (CONTINUED)



† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

Figure 42. HPI Write Timing (HAS Not Used, Tied High)



† For correct operation, strobe the HAS signal only once per HSTROBE active cycle.
‡ HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

Figure 43. HPI Write Timing (HAS Used)

PRODUCT PREVIEW

MULTICHANNEL BUFFERED SERIAL PORT TIMING

timing requirements for McBSP†‡ (see Figure 44)

NO.				–150 –225		UNIT
				MIN	MAX	
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext			
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext			
5	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int			
			CLKR ext			
6	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int			
			CLKR ext			
7	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int			
			CLKR ext			
8	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int			
			CLKR ext			
10	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int			
			CLKX ext			
11	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int			
			CLKX ext			

† CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
§ The minimum CLKR/X period is twice the CPU cycle time (2P). This means that the maximum bit rate for communications between the McBSP and other device is 75 Mbps for 150 MHz CPU clock or 50 Mbps for 100 MHz CPU clock; where the McBSP is either the master or the slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 33 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 30 ns (33 MHz), whichever value is larger. For example, when running parts at 150 MHz (P = 6.7 ns), use 33 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 60 MHz (P = 16.67 ns), use 2P = 33 ns (30 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

switching characteristics over recommended operating conditions for McBSP†‡ (see Figure 44)

NO.	PARAMETER			–150 –225		UNIT
				MIN	MAX	
1	$t_{d(CKSH-CKRXH)}$	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input				
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X int			
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X int			
4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	CLKR int			
9	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	CLKX int			
			CLKX ext			
12	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	CLKX int			
			CLKX ext			
13	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	CLKX int			
			CLKX ext			
14	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	FSX int			
			FSX ext			

† CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ Minimum delay times also represent minimum output hold times.

§ P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

¶ The minimum CLKR/X period is twice the CPU cycle time (2P). This means that the maximum bit rate for communications between the McBSP and other device is 75 Mbps for 150 MHz CPU clock or 50 Mbps for 100 MHz CPU clock; where the McBSP is either the master or the slave. Care must be taken to ensure that the AC timings specified in this data sheet are met. The maximum bit rate for McBSP-to-McBSP communications is 33 Mbps; therefore, the minimum CLKR/X clock cycle is either twice the CPU cycle time (2P), or 30 ns (33 MHz), whichever value is larger. For example, when running parts at 150 MHz (P = 6.7 ns), use 33 ns as the minimum CLKR/X clock cycle (by setting the appropriate CLKGDV ratio or external clock source). When running parts at 60 MHz (P = 16.67 ns), use 2P = 33 ns (30 MHz) as the minimum CLKR/X clock cycle. The maximum bit rate for McBSP-to-McBSP communications applies when the serial port is a master of the clock and frame syncs (with CLKR connected to CLKX, FSR connected to FSX, CLKXM = FSXM = 1, and CLKRM = FSRM = 0) in data delay 1 or 2 mode (R/XDATDLY = 01b or 10b) and the other device the McBSP communicates to is a slave.

# C = H or L
S = sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see ¶ footnote above).

‖ Extra delay from CLKX high to DX valid applies *only* to the first data bit of a device, if and only if DXENA = 1 in SPCR.
If DXENA = 0, then D1 = D2 = 0
If DXENA = 1, then D1 = 2P, D2 = 4P

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MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

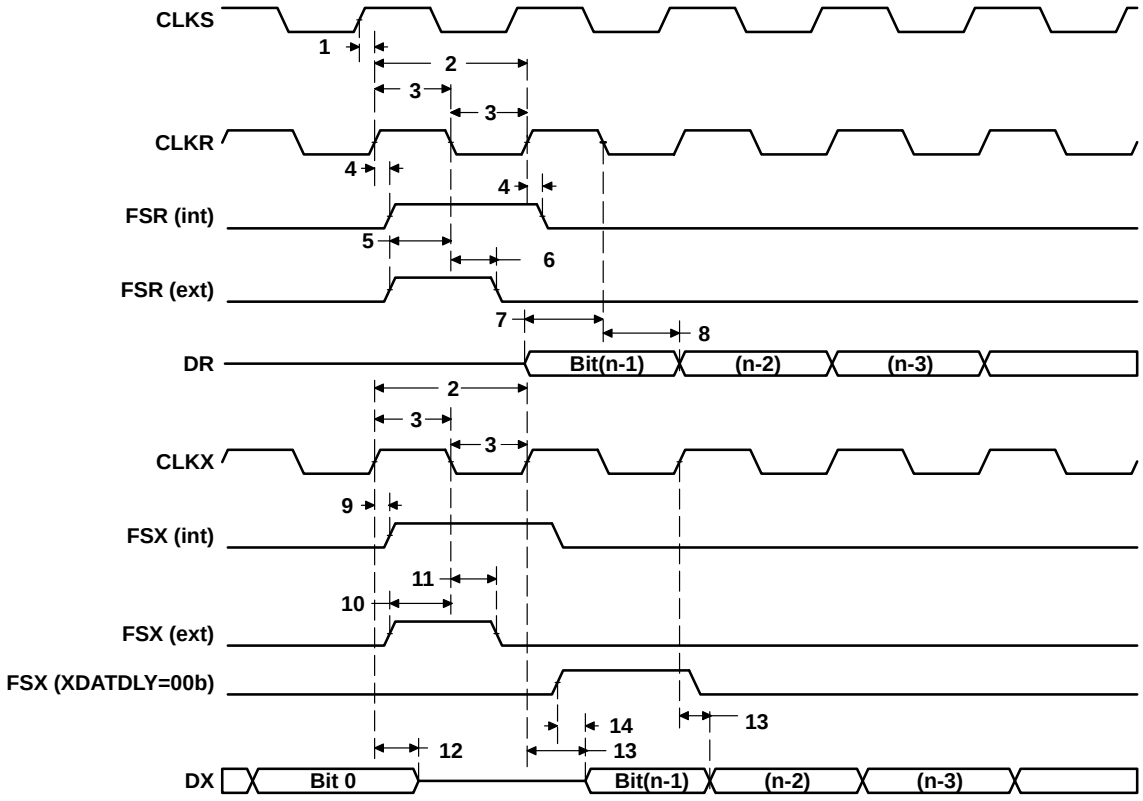

Figure 44. McBSP Timings

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for FSR when GSYNC = 1 (see Figure 45)

NO.			–150 –225		UNIT
			MIN	MAX	
1	$t_{su(FRH-CKSH)}$	Setup time, FSR high before CLKS high			
2	$t_{h(CKSH-FRH)}$	Hold time, FSR high after CLKS high			

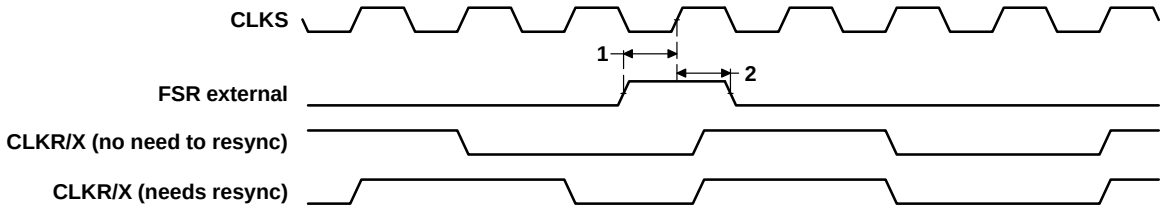

Figure 45. FSR Timing When GSYNC = 1

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MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0†‡ (see Figure 46)

NO.			–150 –225				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low					
5	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low					

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 0†‡ (see Figure 46)

NO.	PARAMETER		–150 –225				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low¶					
2	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high#					
3	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid					
6	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low					
7	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high					
8	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid					

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

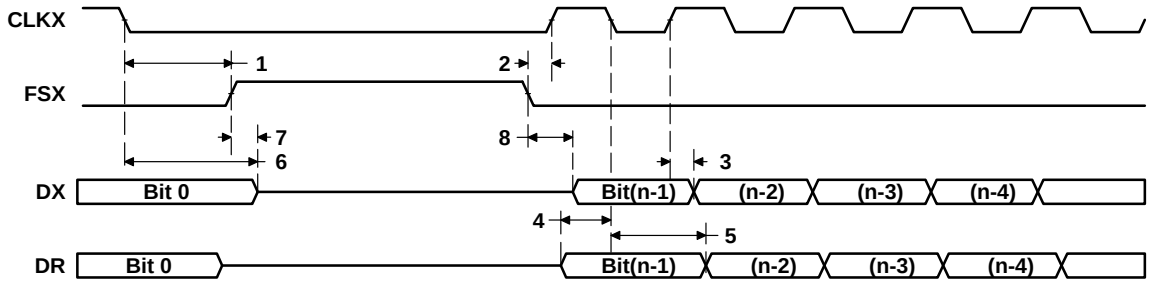

Figure 46. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0†‡ (see Figure 47)

NO.		–150 –225				UNIT
		MASTER		SLAVE		
		MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXH)}$ Setup time, DR valid before CLKX high					
5	$t_{h(CKXH-DRV)}$ Hold time, DR valid after CLKX high					

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0†‡ (see Figure 47)

NO.	PARAMETER		–150 –225				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low¶					
2	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high#					
3	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid					
6	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low					
7	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid					

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

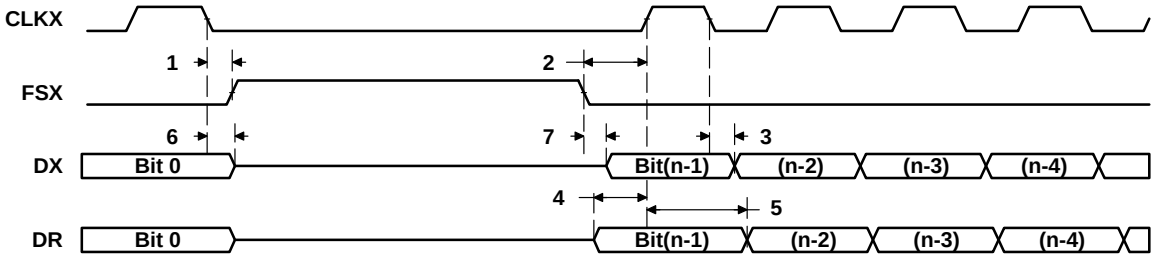

Figure 47. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1†‡ (see Figure 48)

NO.		–150 –225		UNIT
		MASTER	SLAVE	
		MIN MAX	MIN MAX	
4	$t_{su(DRV-CKXH)}$ Setup time, DR valid before CLKX high			
5	$t_{h(CKXH-DRV)}$ Hold time, DR valid after CLKX high			

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 10b, CLKXP = 1†‡ (see Figure 48)

NO.	PARAMETER		–150 –225		UNIT
			MASTER§	SLAVE	
			MIN MAX	MIN MAX	
1	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high¶			
2	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low#			
3	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid			
6	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high			
7	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high			
8	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid			

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

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MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

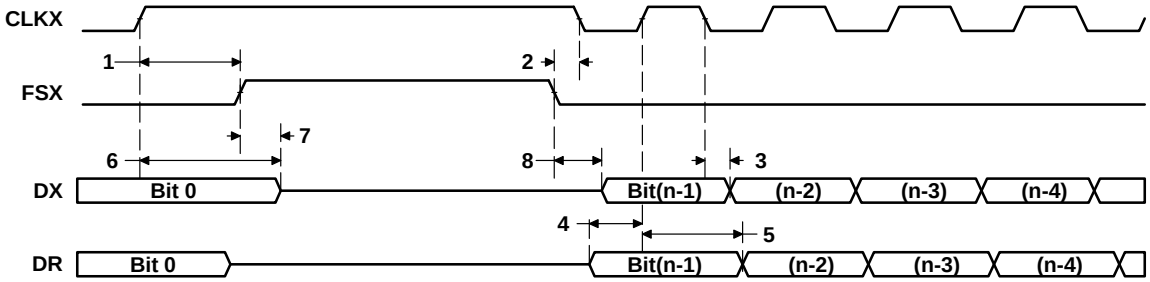

Figure 48. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1†‡ (see Figure 49)

NO.		–150 –225				UNIT
		MASTER		SLAVE		
		MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXH)}$ Setup time, DR valid before CLKX high					
5	$t_{h(CKXH-DRV)}$ Hold time, DR valid after CLKX high					

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1†‡ (see Figure 49)

NO.	PARAMETER		–150 –225				UNIT
			MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	
1	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high¶					
2	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low#					
3	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid					
6	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high					
7	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid					

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

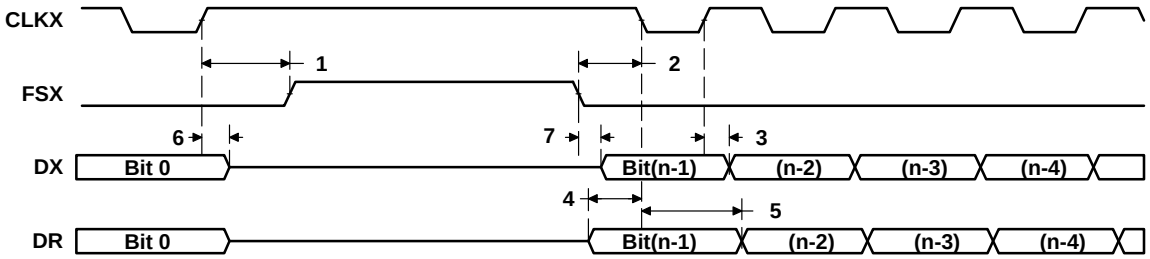

Figure 49. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

TIMER TIMING

timing requirements for timer inputs† (see Figure 50)

NO.			–150 –225		UNIT
			MIN	MAX	
1	$t_{w(TINPH)}$	Pulse duration, TINP high			
2	$t_{w(TINPL)}$	Pulse duration, TINP low			

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

switching characteristics over recommended operating conditions for timer outputs† (see Figure 50)

NO.	PARAMETER		–150 –225		UNIT
			MIN	MAX	
3	$t_{w(TOUTH)}$	Pulse duration, TOUT high			
4	$t_{w(TOUTL)}$	Pulse duration, TOUT low			

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

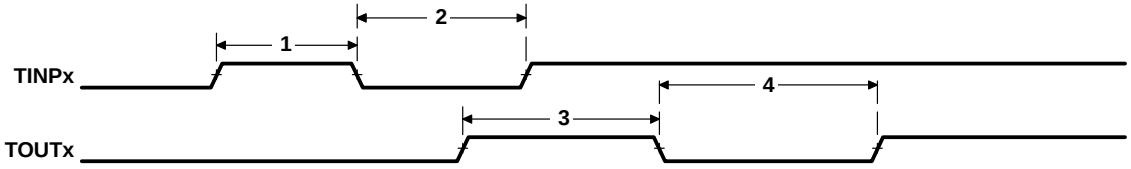

Figure 50. Timer Timing

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GENERAL-PURPOSE INPUT/OUTPUT (GPIO) PORT TIMING

timing requirements for GPIO inputs† (see Figure 51)

NO.			–150 –225		UNIT
			MIN	MAX	
1	$t_{w(GPIH)}$	Pulse duration, GPIx high			
2	$t_{w(GPIL)}$	Pulse duration, GPIx low			

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

switching characteristics over recommended operating conditions for GPIO outputs† (see Figure 51)

NO.	PARAMETER		–150 –225		UNIT
			MIN	MAX	
3	$t_{w(GPOH)}$	Pulse duration, GPOx high			
4	$t_{w(GPOL)}$	Pulse duration, GPOx low			

† P = 1/CPU clock frequency in ns. For example, when running parts at 225 MHz, use P = 4.4 ns.

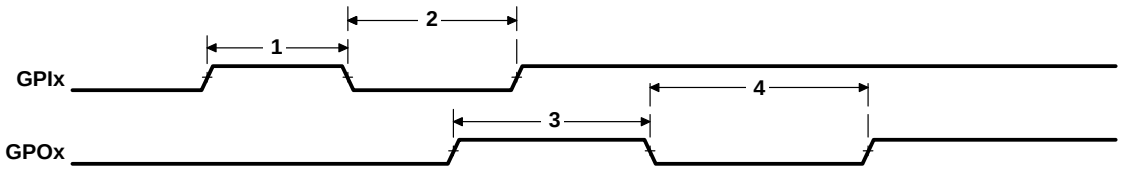


Figure 51. GPIO Port Timing

JTAG TEST-PORT TIMING

timing requirements for JTAG test port (see Figure 52)

NO.			–150 –225		UNIT
			MIN	MAX	
1	$t_{c(TCK)}$	Cycle time, TCK			
3	$t_{su(TDIV-TCKH)}$	Setup time, TDI/TMS/$\overline{TRST}$ valid before TCK high			
4	$t_{h(TCKH-TDIV)}$	Hold time, TDI/TMS/$\overline{TRST}$ valid after TCK high			

switching characteristics over recommended operating conditions for JTAG test port (see Figure 52)

NO.	PARAMETER		–150 –225		UNIT
			MIN	MAX	
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid			

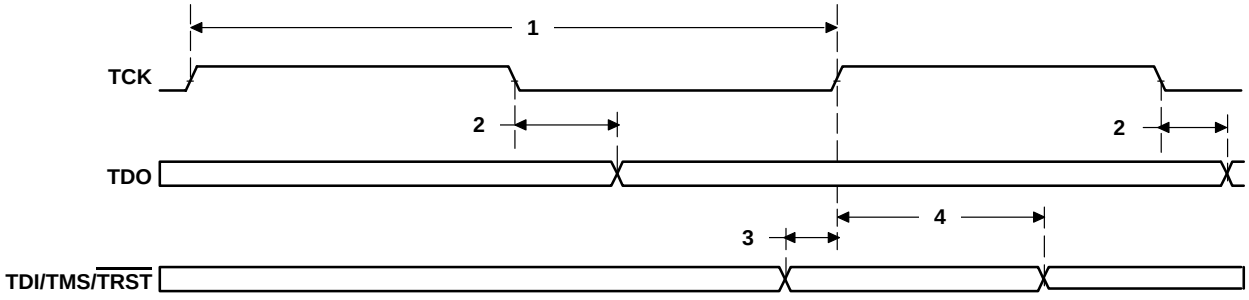


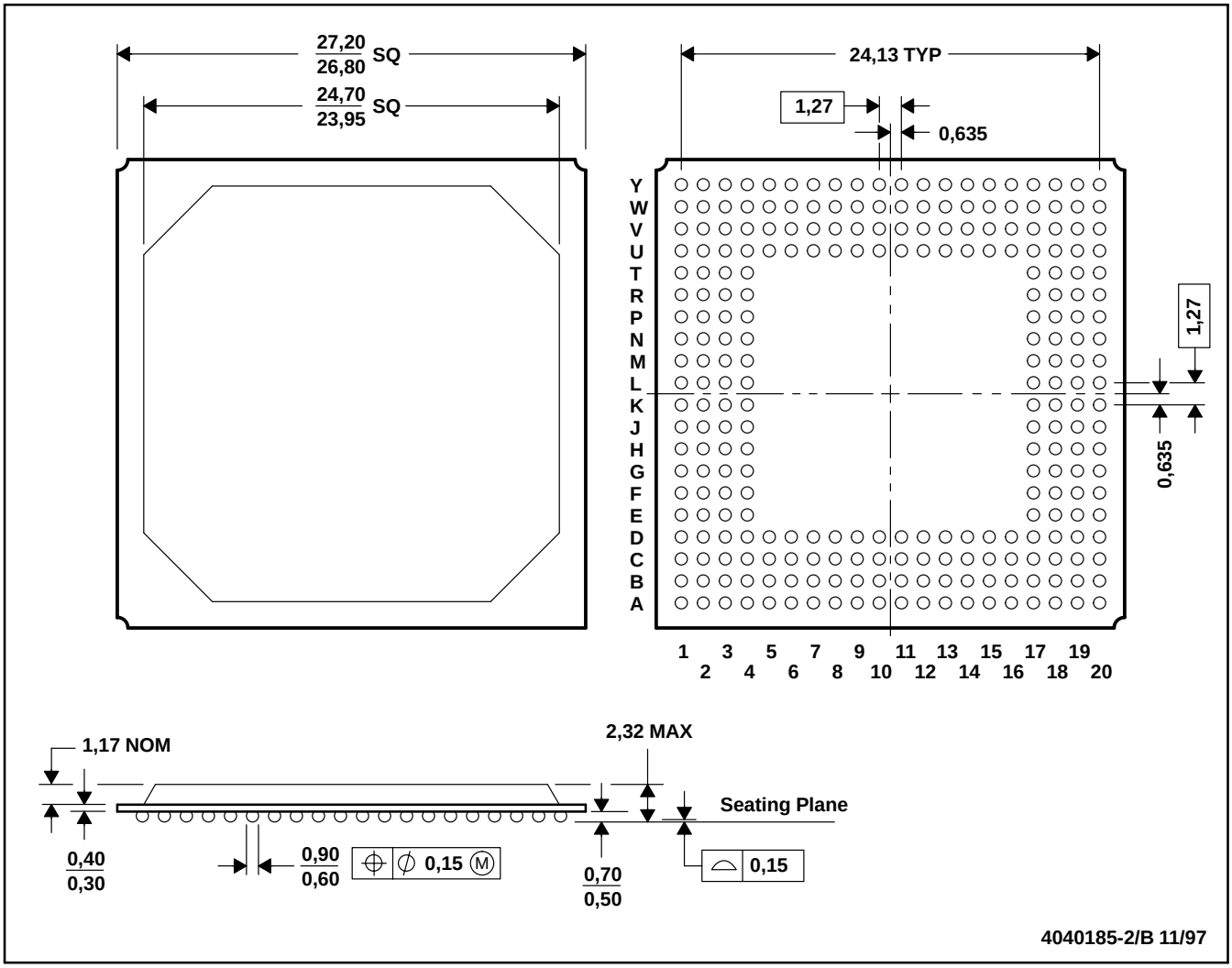
Figure 52. JTAG Test-Port Timing

PRODUCT PREVIEW

PRODUCT PREVIEW

MECHANICAL DATA

GFN (S-PBGA-N256) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

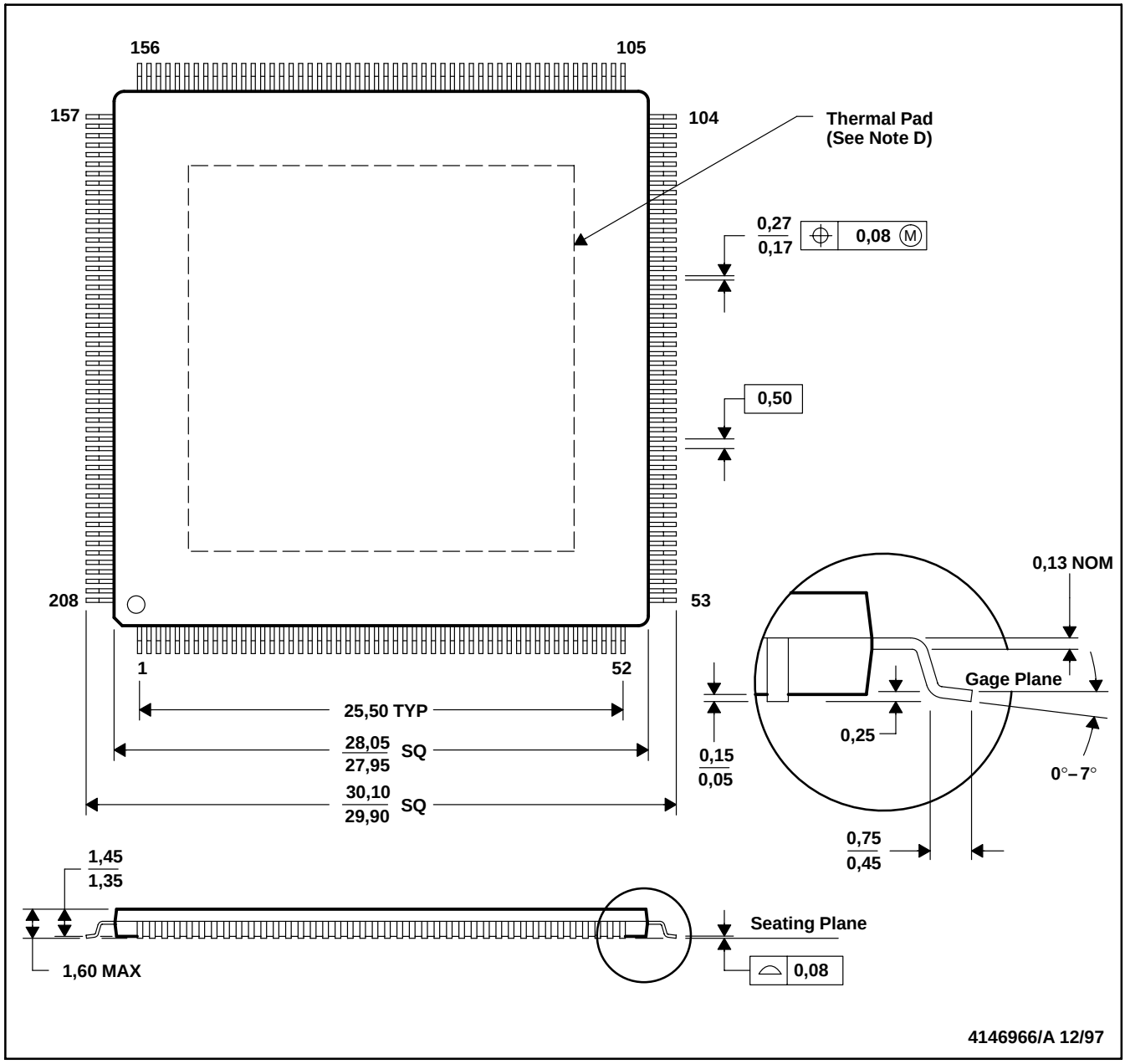
thermal resistance characteristics (S-PBGA package)

NO			°C/W	Air Flow (m/s)†
1	$R\Theta_{JC}$	Junction-to-case		N/A
2	$R\Theta_{JA}$	Junction-to-free air		0.0
3	$R\Theta_{JA}$	Junction-to-free air		0.5
4	$R\Theta_{JA}$	Junction-to-free air		1.0
5	$R\Theta_{JA}$	Junction-to-free air		2.0

† m/s = meters per second

MECHANICAL DATA

PYP (S-PQFP-G208) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

PRODUCT PREVIEW

MECHANICAL DATA (CONTINUED)

thermal resistance characteristics (S-PQFP-G208 package)

NO			°C/W	Air Flow (m/s)†
1	$R\Theta_{JC}$	Junction-to-case		N/A
2	$R\Theta_{JA}$	Junction-to-free air		0.0
3	$R\Theta_{JA}$	Junction-to-free air		0.5
4	$R\Theta_{JA}$	Junction-to-free air		1.0
5	$R\Theta_{JA}$	Junction-to-free air		2.0

† m/s = meters per second

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