PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD444012L-X

4M-BIT CMOS STATIC RAM
256K-WORD BY 16-BIT
EXTENDED TEMPERATURE OPERATION

Description

The μPD444012L-X is a high speed, low power, 4,194,304 bits (262,144 words by 16 bits) CMOS static RAM.

The μPD444012L-X has two chip enable pins (/CE1, CE2) to extend the capacity.

The μPD444012L-X is packed in 48-pin plastic TSOP (I).

Features

- 262,144 words by 16 bits organization
- Fast access time: 70, 85, 100, 120, 150 ns (MAX.)
- Byte data control: /LB (I/O1 - I/O8), /UB (I/O9 - I/O16)
- Low voltage operation
  (B version: V_{CC} = 2.7 to 3.6 V, C version: V_{CC} = 2.2 to 3.6 V, D version: V_{CC} = 1.8 to 3.6 V)
- Operating ambient temperature: T_A = –25 to +85 °C
- Output Enable input for easy application
- Two Chip Enable inputs: /CE1, CE2

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
				At operating mA (MAX.)	At standby μA (MAX.)	At data retention μA (MAX.)
μPD444012L-BxxX	70, 85	2.7 to 3.6	–25 to +85	40	7	7
μPD444012L-CxxX	100, 120	2.2 to 3.6				
μPD444012L-DxxX	120, 150	1.8 to 3.6				

The information in this document is subject to change without notice.

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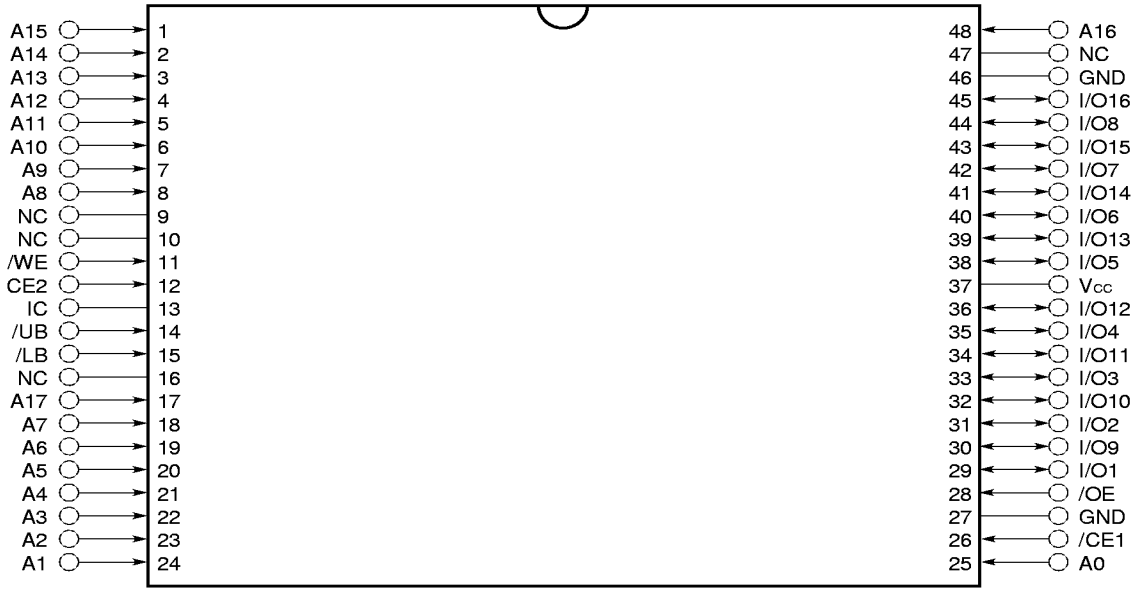
Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark
μPD444012LGY-B70X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	70	2.7 to 3.6	–25 to +85	B version
μPD444012LGY-B70X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012LGY-B85X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	85			
μPD444012LGY-B85X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012LGY-C10X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	100	2.2 to 3.6		C version
μPD444012LGY-C10X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012LGY-C12X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	120			
μPD444012LGY-C12X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012LGY-D12X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	120	1.8 to 3.6		D version
μPD444012LGY-D12X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				
μPD444012LGY-D15X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	150			
μPD444012LGY-D15X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)				

Pin Configuration (Marking Side)

/xxx indicates active low signal.

48-pin Plastic TSOP (I) (12×18 mm) (Normal Bent)
[μPD444012LGY-BxxX-MJH]
[μPD444012LGY-CxxX-MJH]
[μPD444012LGY-DxxX-MJH]



A0 - A17	:	Address inputs
I/O1 - I/O16	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
/LB, /UB	:	Byte data select
V_{CC}	:	Power supply
GND	:	Ground
NC	:	No Connection
IC [Note]	:	Internal Connection

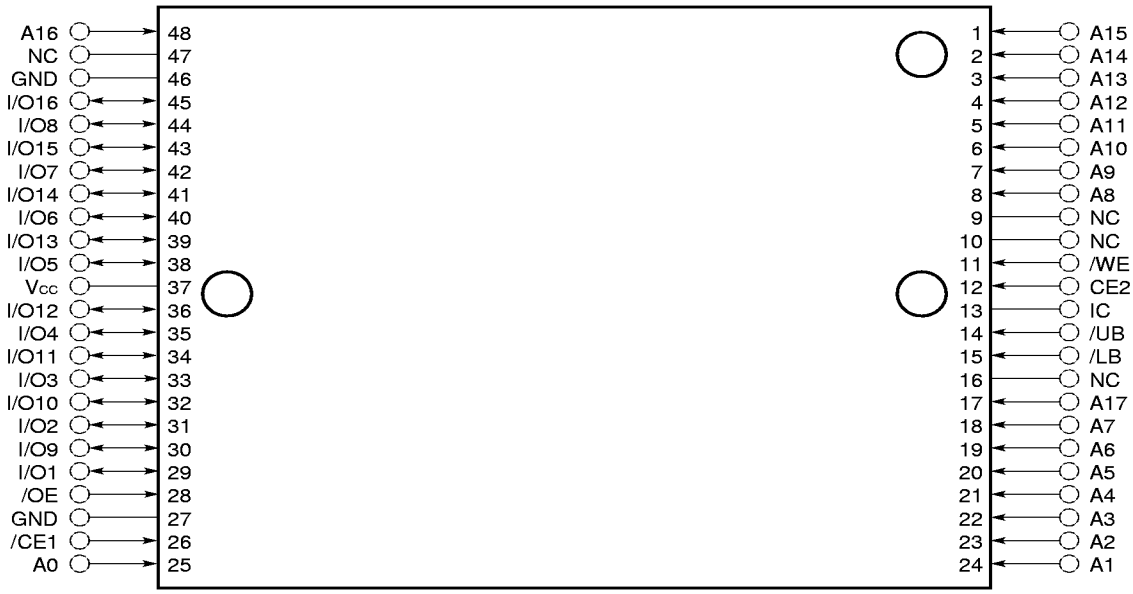
Note Leave this pin unconnected or connect to GND.

48-pin Plastic TSOP (I) (12×18 mm) (Reverse Bent)

[μPD444012LGY-BxxX-MKH]

[μPD444012LGY-CxxX-MKH]

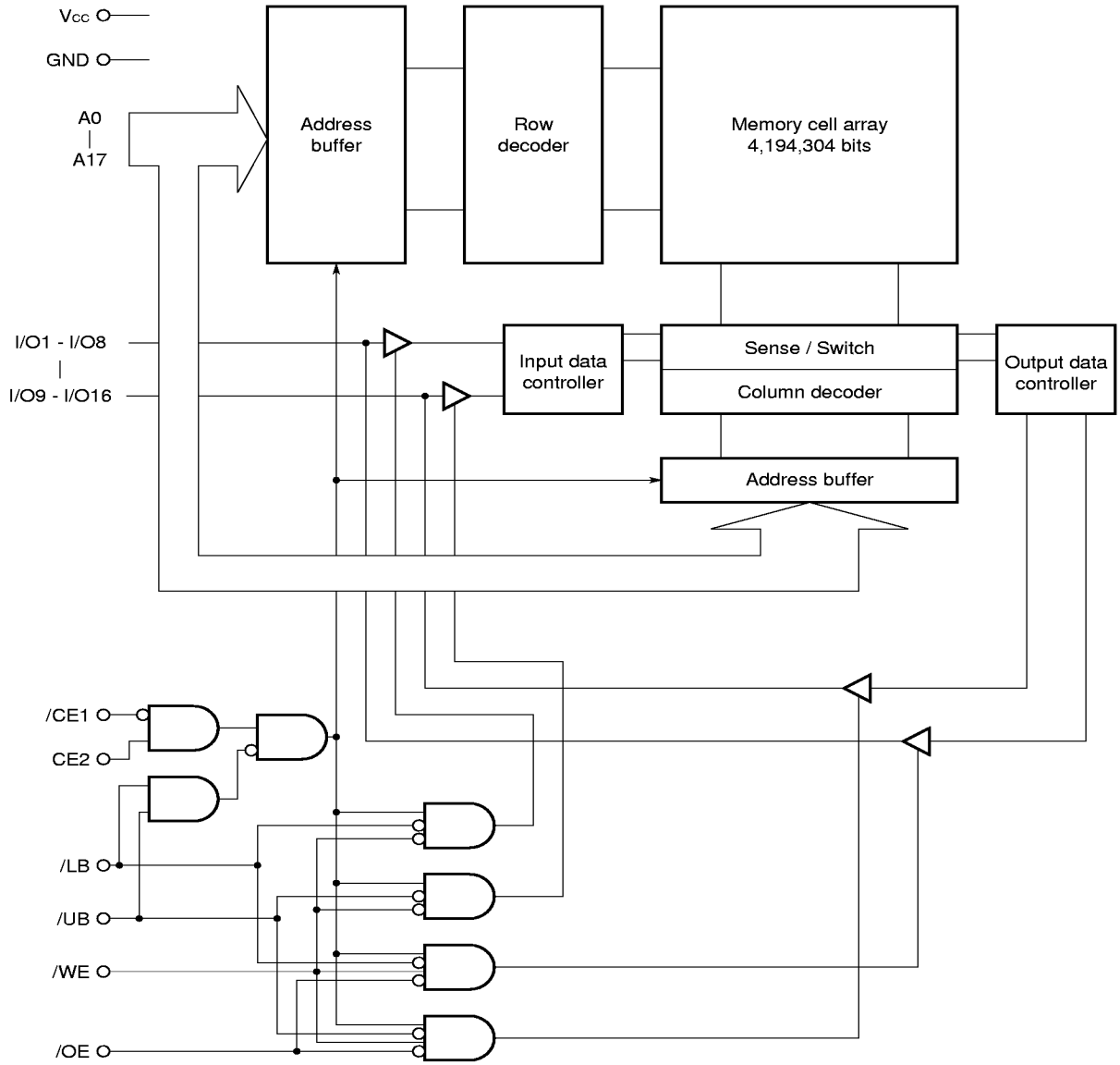
[μPD444012LGY-DxxX-MKH]



A0 - A17	:	Address inputs
I/O1 - I/O16	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
/LB, /UB	:	Byte data select
Vcc	:	Power supply
GND	:	Ground
NC	:	No Connection
IC Note	:	Internal Connection

Note Leave this pin unconnected or connect to GND.

Block Diagram



Truth Table

/CE1	CE2	/OE	/WE	/LB	/UB	Mode	I/O		Supply current
							I/O1 - I/O8	I/O9 - I/O16	
H	×	×	×	×	×	Not selected	High impedance	High impedance	I_{SB}
×	L	×	×	×	×				
L	H	H	H	×	×	Output disable	High impedance	High impedance	I_{CCA}
		L	H	L	L	Word read	D_{OUT}	D_{OUT}	
				L	H	Lower byte read	D_{OUT}	High impedance	
				H	L	Upper byte read	High impedance	D_{OUT}	
		×	L	L	L	Word write	D_{IN}	D_{IN}	
				L	H	Lower byte write	D_{IN}	High impedance	
				H	L	Upper byte write	High impedance	D_{IN}	
×	×	×	×	H	H	Not selected	High impedance	High impedance	I_{SB}[Note]

Note /CE1, CE2 = V_{IH} or V_{IL}

Remark × : Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 Note to +4.0	V
Input / Output voltage	V_T		–0.5 Note to V_{CC}+0.4 (4.0 V MAX.)	V
Operating ambient temperature	T_A		–25 to +85	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width : 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD444012L-BxxX		μPD444012L-CxxX		μPD444012L-DxxX		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		2.7	3.6	2.2	3.6	1.8	3.6	V
High level input voltage	V_{IH}	2.7 V ≤ V_{CC} ≤ 3.6 V	2.4	V_{CC}+0.4	2.4	V_{CC}+0.4	2.4	V_{CC}+0.4	V
		2.2 V ≤ V_{CC} < 2.7 V	–	–	2.0	V_{CC}+0.3	2.0	V_{CC}+0.3	
		1.8 V ≤ V_{CC} < 2.2 V	–	–	–	–	1.6	V_{CC}+0.2	
Low level input voltage	V_{IL}		–0.3 Note	+0.5	–0.3 Note	+0.3	–0.3 Note	+0.2	V
Operating ambient temperature	T_A		–25	+85	–25	+85	–25	+85	°C

Note –1.5 V (MIN.) (Pulse width: 30 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			8	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN} : Input voltage

2. These parameters are periodically sampled and not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition		$V_{CC} \geq 2.7$ V			$V_{CC} \geq 2.2$ V			$V_{CC} \geq 1.8$ V			Unit
				μPD444012L-BxxX			μPD444012L-CxxX			μPD444012L-DxxX			
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	–1.0		+1.0	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CE1 = V_{IH} or CE2 = V_{IL} or /WE = V_{IL} or /OE = V_{IH}		–1.0		+1.0	–1.0		+1.0	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CE1 = V_{IL}, CE2 = V_{IH}, Minimum cycle time, $I_{I/O}$ = 0 mA			–	40		–	40		–	40	mA
			$V_{CC} \leq 2.7$ V		–	–		–	38		–	38	
			$V_{CC} \leq 2.2$ V		–	–		–	–		–	35	
	I_{CCA2}	/CE1 = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0 mA			–	10		–	10		–	10	
			$V_{CC} \leq 2.7$ V		–	–		–	8		–	8	
			$V_{CC} \leq 2.2$ V		–	–		–	–		–	6	
	I_{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA,			–	8		–	8		–	8	
		$V_{IL} \leq 0.2$ V,	$V_{CC} \leq 2.7$ V		–	–		–	6		–	6	
		$V_{IH} \geq V_{CC}$ – 0.2 V	$V_{CC} \leq 2.2$ V		–	–		–	–		–	6	
Standby supply current	I_{SB}	/CE1 = V_{IH} or CE2 = V_{IL} or			–	0.6		–	0.6		–	0.6	mA
		/LB = /UB = V_{IH},	$V_{CC} \leq 2.7$ V		–	–		–	0.6		–	0.6	
		/CE1, CE2 = V_{IH} or V_{IL}	$V_{CC} \leq 2.2$ V		–	–		–	–		–	0.6	
	I_{SB1}	/CE1 ≥ V_{CC} – 0.2 V,			0.5	7		0.5	7		0.5	7	μA
		CE2 ≥ V_{CC} – 0.2 V	$V_{CC} \leq 2.7$ V		–	–		0.4	6		0.4	6	
			$V_{CC} \leq 2.2$ V		–	–		–	–		0.3	5	
	I_{SB2}	CE2 ≤ 0.2 V			0.5	7		0.5	7		0.5	7	
			$V_{CC} \leq 2.7$ V		–	–		0.4	6		0.4	6	
			$V_{CC} \leq 2.2$ V		–	–		–	–		0.3	5	
	I_{SB3}	/LB = /UB ≥ V_{CC} – 0.2 V,			0.5	7		0.5	7		0.5	7	
		/CE1 ≤ 0.2 V,	$V_{CC} \leq 2.7$ V		–	–		0.4	6		0.4	6	
		CE2 ≥ V_{CC} – 0.2 V	$V_{CC} \leq 2.2$ V		–	–		–	–		0.3	5	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA		2.4			2.4			2.4			V
			$V_{CC} \leq 2.7$ V	–			1.8			1.8			
			$V_{CC} \leq 2.2$ V	–			–			1.5			
Low level output voltage	V_{OL}	I_{OL} = 1.0 mA				0.4			0.4			0.4	V

Remarks 1. V_{IN} : Input voltage

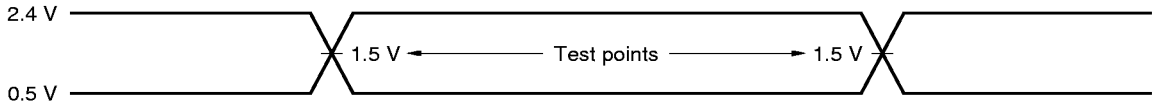
2. These DC characteristics are in common regardless of package types and access time.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

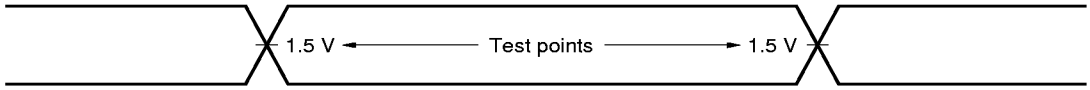
AC Test Conditions

[μPD444012L-B70X, μPD444012L-B85X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

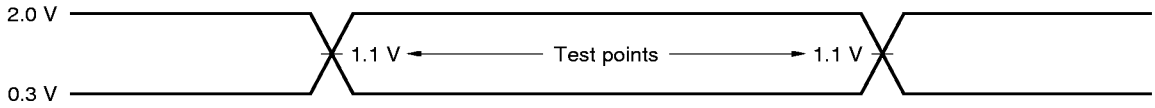


Output Load

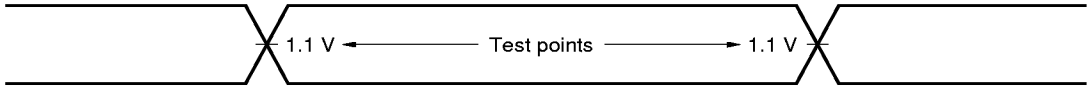
1TTL + 50 pF

[μPD444012L-C10X, μPD444012L-C12X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

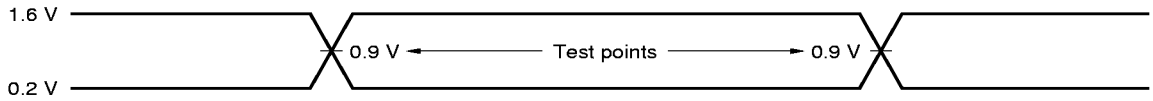


Output Load

1TTL + 30 pF

[μPD444012L-D12X, μPD444012L-D15X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

Output Load

1TTL + 30 pF

Read Cycle

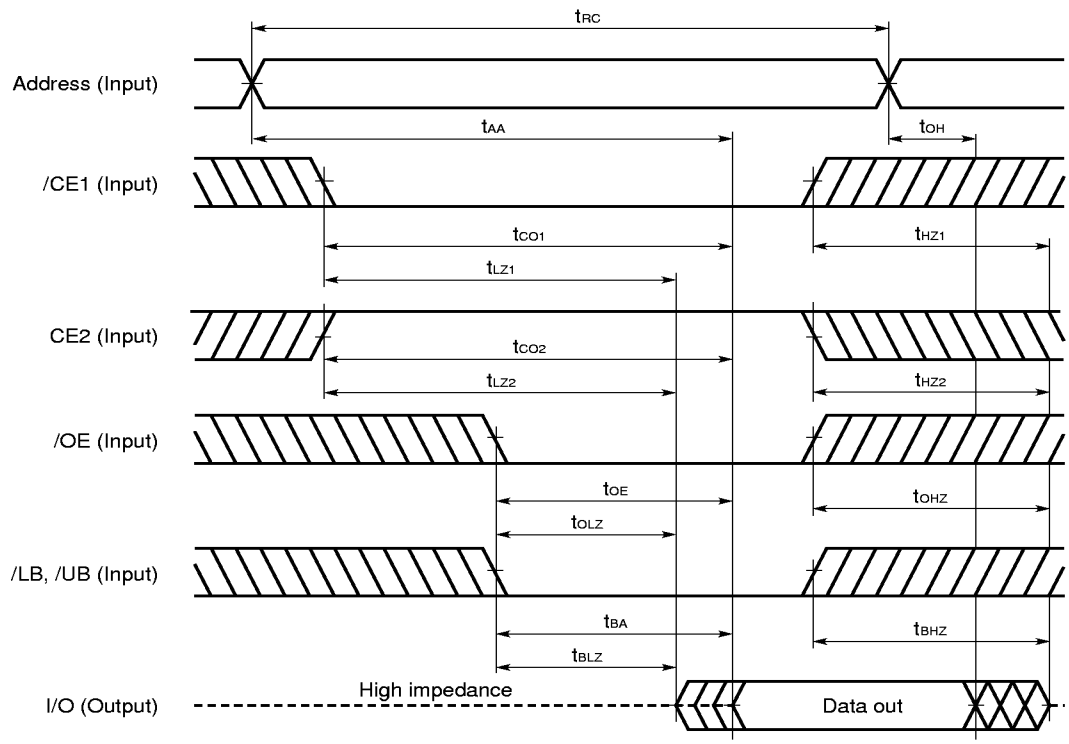
Parameter	Symbol	$V_{CC} \geq 2.7$ V				$V_{CC} \geq 2.2$ V				$V_{CC} \geq 1.8$ V				Unit	Condition
		μPD444012L -B70X		μPD444012L -B85X		μPD444012L -C10X		μPD444012L -C12X		μPD444012L -D12X		μPD444012L -D15X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		100		120		120		150		ns	
Address access time	t_{AA}		70		85		100		120		120		150	ns	**Note 1**
/CE1 access time	t_{CO1}		70		85		100		120		120		150	ns	
CE2 access time	t_{CO2}		70		85		100		120		120		150	ns	
/OE to output valid	t_{OE}		35		40		50		60		60		70	ns	
/LB, /UB to output valid	t_{BA}		70		85		100		120		120		150	ns	
Output hold from address change	t_{OH}	10		10		10		10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		10		10		10		ns	**Note 2**
CE2 to output in low impedance	t_{LZ2}	10		10		10		10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	10		10		10		10		10		10		ns	
/CE1 to output in high impedance	t_{HZ1}		25		30		35		40		40		50	ns	
CE2 to output in high impedance	t_{HZ2}		25		30		35		40		40		50	ns	
/OE to output in high impedance	t_{OHZ}		25		30		35		40		40		50	ns	
/LB, /UB to output in high impedance	t_{BHZ}		25		30		35		40		40		50	ns	

Notes 1. The output load is 1TTL + 50 pF (μPD444012L-BxxX) or 1TTL + 30 pF (μPD444012L-CxxX, -DxxX).

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

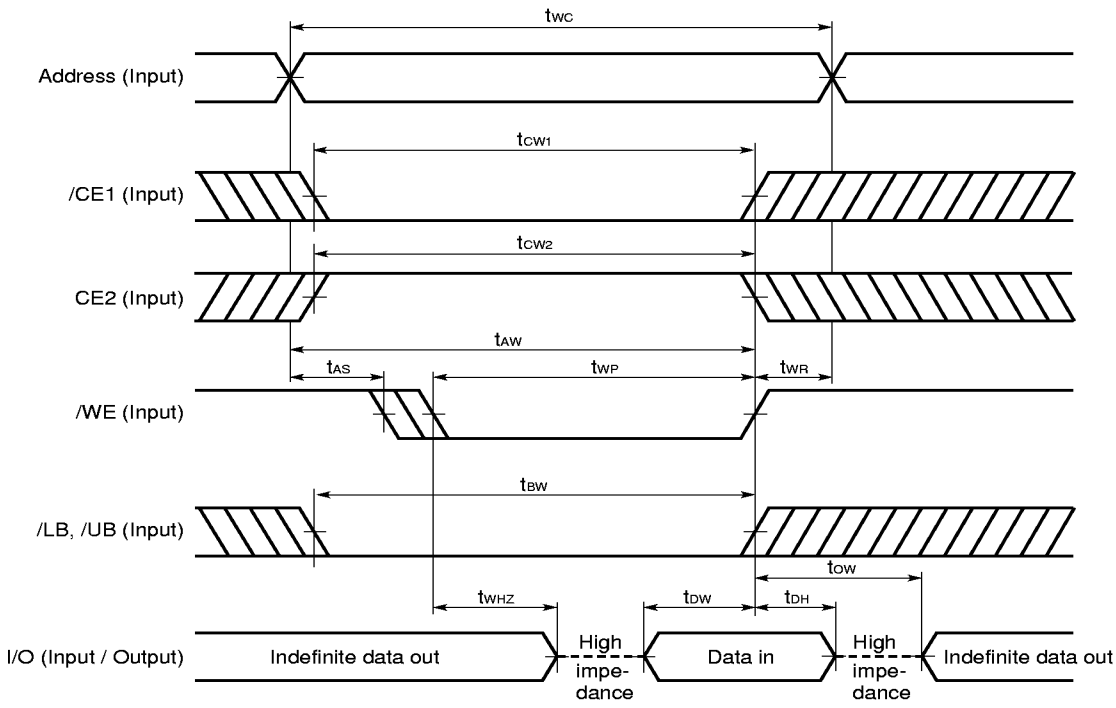
Write Cycle

Parameter	Symbol	$V_{CC} \geq 2.7$ V				$V_{CC} \geq 2.2$ V				$V_{CC} \geq 1.8$ V				Unit	Condition
		μPD444012L -B70X		μPD444012L -B85X		μPD444012L -C10X		μPD444012L -C12X		μPD444012L -D12X		μPD444012L -D15X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		100		120		120		150		ns	
/CE1 to end of write	t_{CW1}	55		70		80		100		100		120		ns	
CE2 to end of write	t_{CW2}	55		70		80		100		100		120		ns	
/LB, /UB to end of write	t_{BW}	55		70		80		100		100		120		ns	
Address valid to end of write	t_{AW}	55		70		80		100		100		120		ns	
Address setup time	t_{AS}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	50		55		60		85		85		100		ns	
Write recovery time	t_{WR}	0		0		0		0		0		0		ns	
Data valid to end of write	t_{DW}	30		35		40		60		60		80		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		25		30		35		40		40		50	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Write Cycle Timing Chart 1 (/WE Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

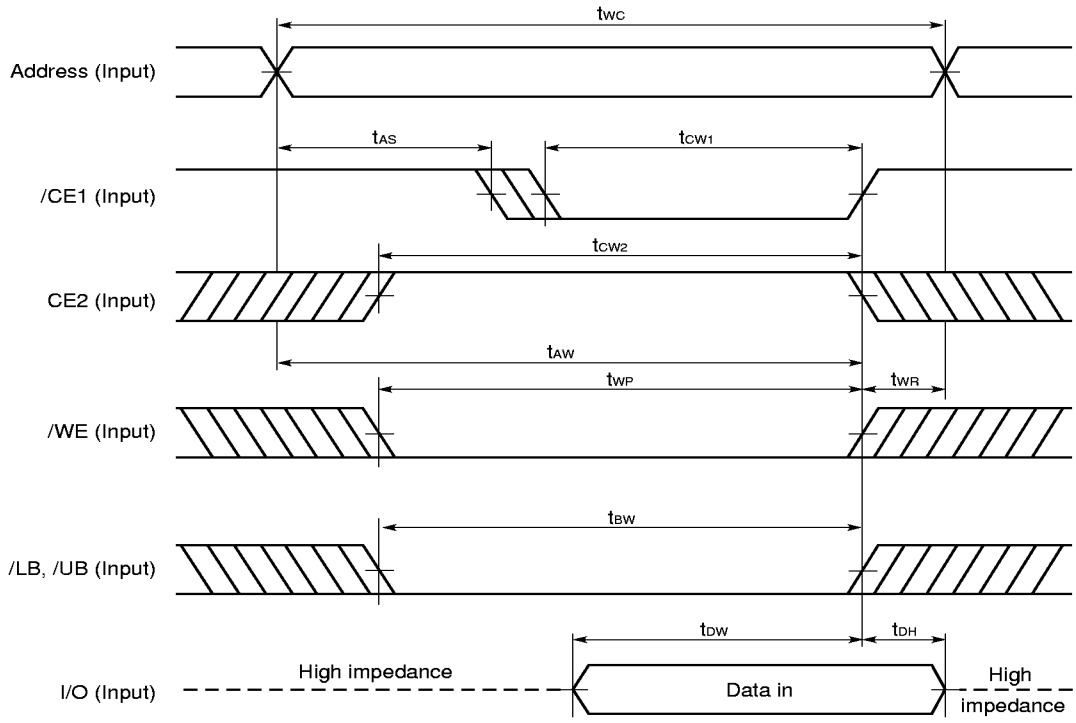
2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remarks 1. Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CE1 Controlled)

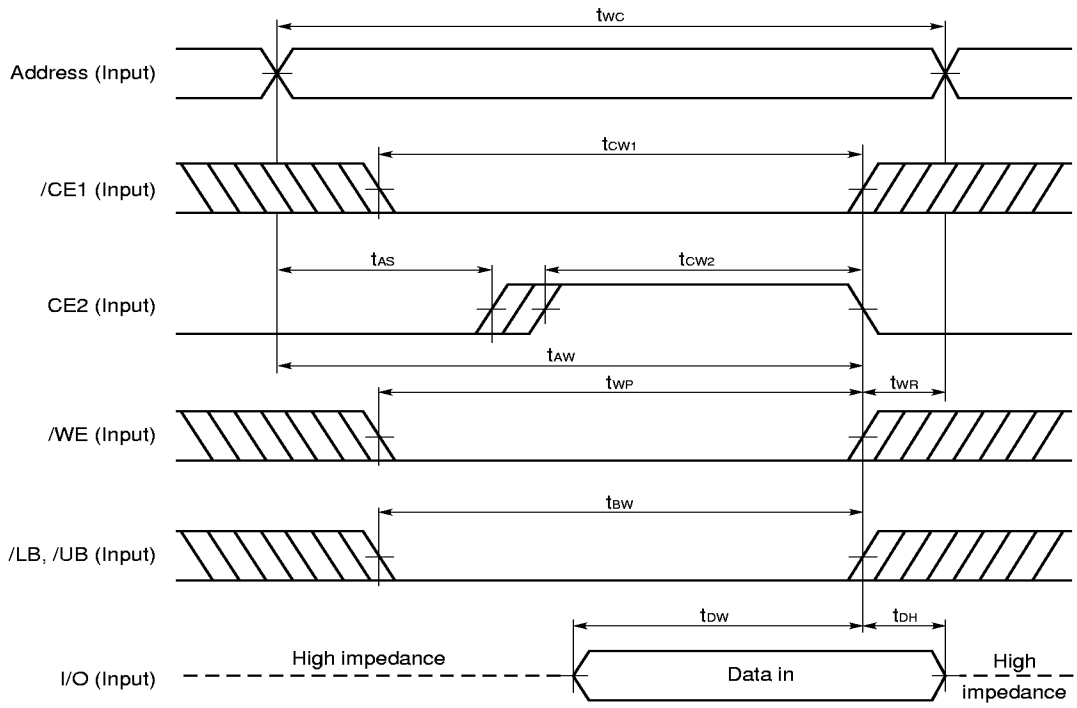


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)

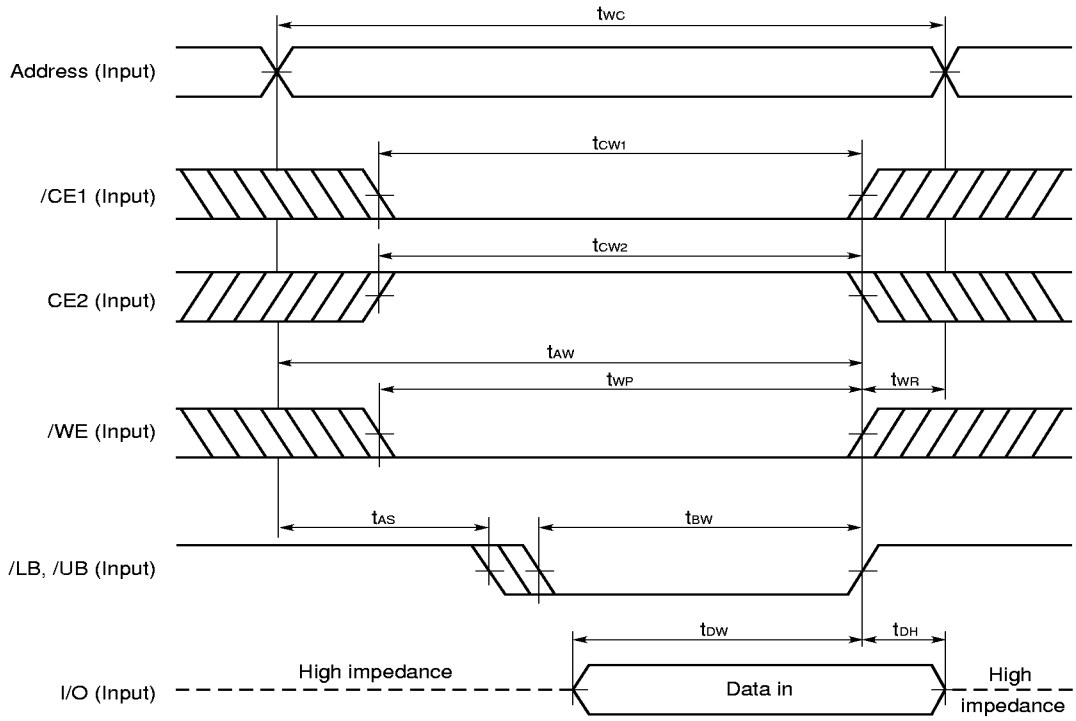


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

Write Cycle Timing Chart 4 (/LB, /UB Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

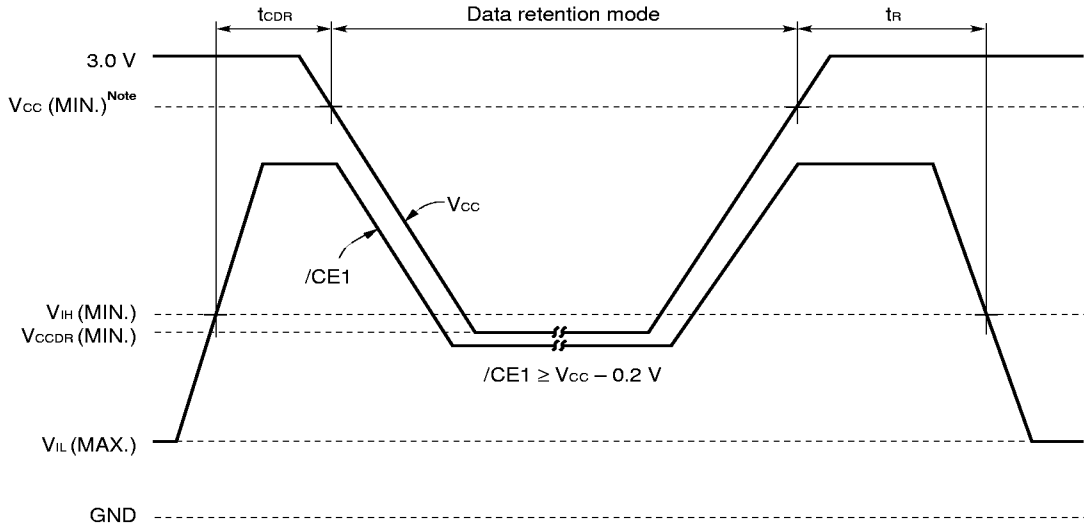
Low V_{CC} Data Retention Characteristics (T_A = –25 to +85 °C)

Parameter	Symbol	Test Condition	V_{CC} ≥ 2.7 V			V_{CC} ≥ 2.2 V			V_{CC} ≥ 1.8 V			Unit
			μPD444012L -B××X			μPD444012L -C××X			μPD444012L -D××X			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention supply voltage	V_{CCDR1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V	2.0		3.6	1.5		3.6	1.5		3.6	V
	V_{CCDR2}	CE2 ≤ 0.2 V	2.0		3.6	1.5		3.6	1.5		3.6	
	V_{CCDR3}	/LB = /UB ≥ V_{CC} – 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V	2.0		3.6	1.5		3.6	1.5		3.6	
Data retention supply current	I_{CCDR1}	V_{CC} = 3.0 V, /CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V or CE2 ≤ 0.2 V		0.5	7		0.5	7		0.5	7	μA
	I_{CCDR2}	V_{CC} = 3.0 V, CE2 ≤ 0.2 V		0.5	7		0.5	7		0.5	7	
	I_{CCDR3}	V_{CC} = 3.0 V, /LB = /UB ≥ V_{CC} – 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V		0.5	7		0.5	7		0.5	7	
Chip deselection to data retention mode	t_{CDR}		0			0			0			ns
Operation recovery time	t_R		t_{RC}[Note]			t_{RC}[Note]			t_{RC}[Note]			ns

Note t_{RC} : Read cycle time

Data Retention Timing Chart

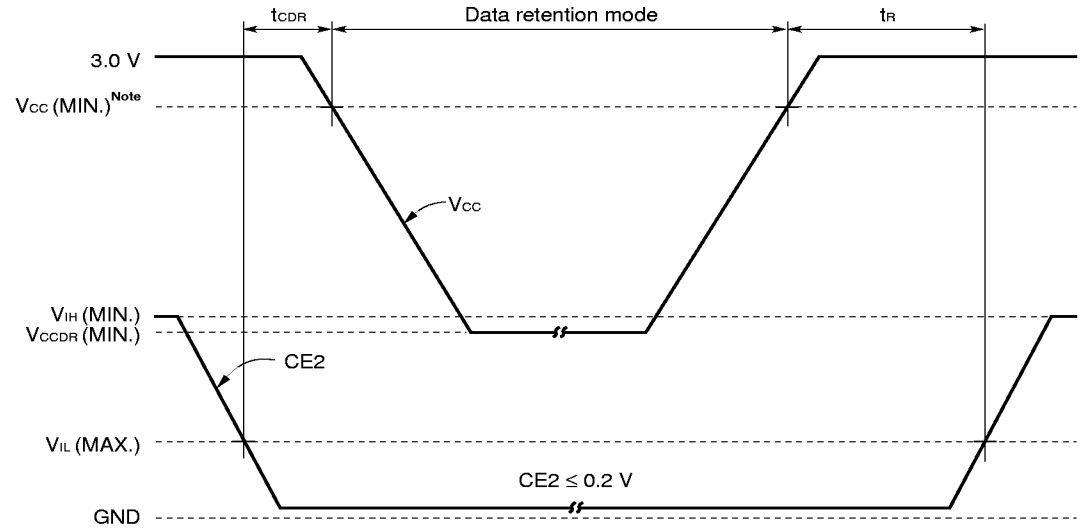
(1) /CE1 Controlled



Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling /CE1, the input level of CE2 must be ≥ V_{CC} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE, /LB, /UB) can be in high impedance state.

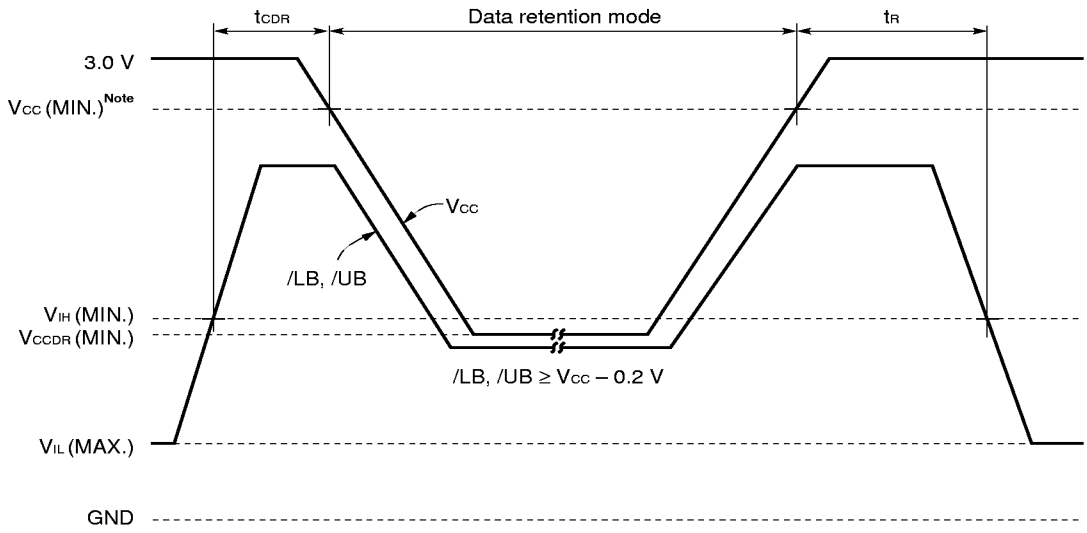
(2) CE2 Controlled



Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark The other pins (/CE1, Address, I/O, /WE, /OE, /LB, /UB) can be in high impedance state.

(3) /LB, /UB Controlled

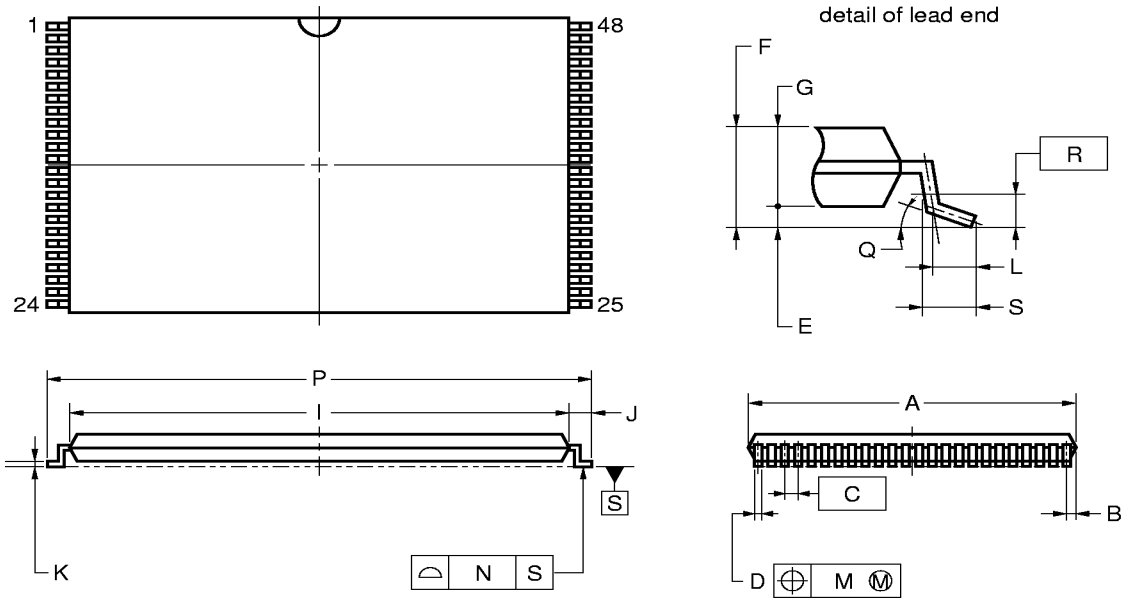


Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling /LB and /UB, the input level of /CE1 and CE2 must be ≥ V_{CC} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawings

48 PIN PLASTIC TSOP (I) (12×18)



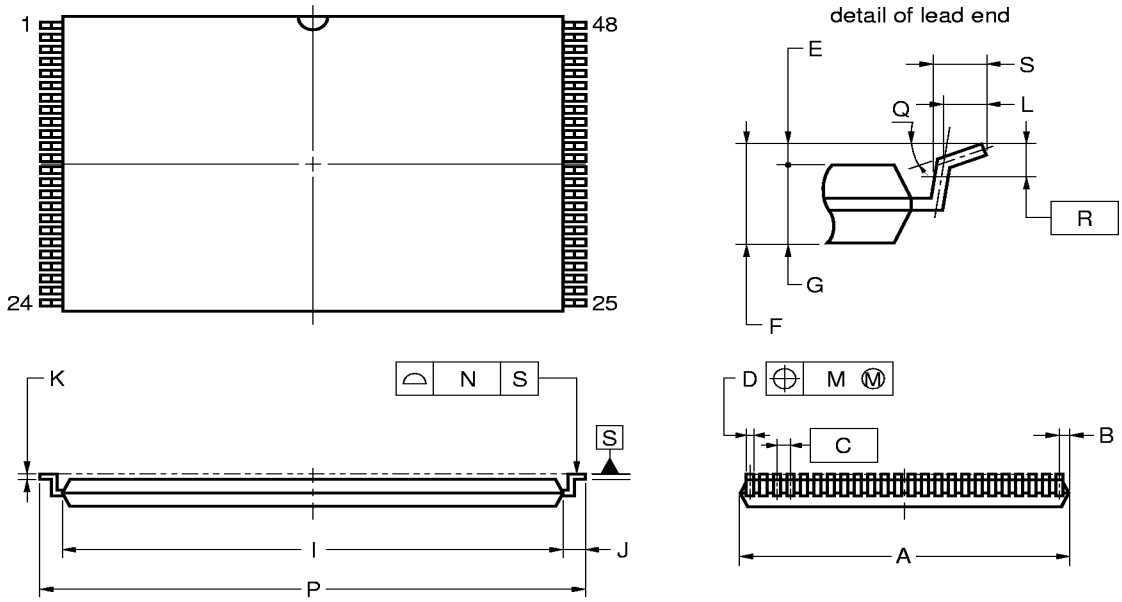
NOTES

1. Controlling dimension — Millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX. <0.489 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	12.0±0.1	$0.472^{+0.005}_{-0.004}$
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	1.0±0.05	$0.039^{+0.003}_{-0.002}$
I	16.4±0.1	$0.646^{+0.004}_{-0.005}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	0.145±0.05	$0.006^{+0.002}_{-0.003}$
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	18.0±0.2	$0.709^{+0.008}_{-0.009}$
Q	$3°^{+5°}_{-3°}$	$3°^{+5°}_{-3°}$
R	0.25	0.010
S	0.60±0.15	$0.024^{+0.006}_{-0.007}$

S48GY-50-MJH1

48 PIN PLASTIC TSOP (I) (12×18)



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S48GY-50-MKH1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD444012L-X.

Type of Surface Mount Device

μPD444012LGY-BxxX-MJH: 48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)
μPD444012LGY-BxxX-MKH: 48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)
μPD444012LGY-CxxX-MJH: 48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)
μPD444012LGY-CxxX-MKH: 48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)
μPD444012LGY-DxxX-MJH: 48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)
μPD444012LGY-DxxX-MKH: 48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)