**Data Sheet**

*2.5 Gbits/sec SONET Compatible*
*8-bit Mux/Demux Chipset*

## Features

- Serial Data Rates up to 2.5 Gb/s
- Parallel Data Rates up to 312.5 Mb/s
- ECL 100K Compatible Parallel Data I/Os
- Divide-by-8 Clock for Synchronization of Parallel Data to Interfacing Chips
- SONET Frame Recovery Circuitry (VS8022)
- Compatible with STS-3 to STS-48 SONET Applications
- Differential or Single-Ended Inputs and Outputs
- Low Power Dissipation: 2.3W (Typ. Per Chip)
- Standard ECL Power Supplies: VEE = -5.2 V, VTT = -2.0 V
- Available in Commercial (0° to +70° C) or Industrial (-40° to +85° C) Temperature Ranges
- Proven E/D Mode GaAs Technology
- 52-pin Leaded Ceramic Chip Carrier

## Functional Description

The VS8021 and VS8022 are high speed SONET interface devices capable of handling serial data at rates up to 2.5 Gbits/second. These products can be used for STS-3 through STS-48 SONET applications.

These products are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation. These products are packaged in a ceramic 52-pin leaded ceramic chip carrier.

## VS8021

The VS8021 contains an 8:1 multiplexer and a self-positioning timer. The 8:1 multiplexer accepts 8 parallel differential ECL data inputs (D1-D8, D1N-D8N) at rates up to 312.5 Mbits/sec and multiplexes them into a serial differential bit stream output (DO, DON) at rates up to 2.5 Gbits/sec.

The internal timing of the VS8021 is built around the high speed clock (up to 2.5 GHz) delivered onto the chip through a differential input (CLKI, CLKIN). This signal is subsequently echoed at the high speed differential output (CO, CON).

The parallel data inputs are clocked to on-chip input registers with an externally supplied differential ECL input (BYCLK, BYCLKN) operating at the same rate as the data inputs. An internal byte clock, which is a divide by 8 version of the high speed clock, is used to transfer the data to a set of buffer registers. This internal byte clock is brought off chip at the ECL output CLK8, CLK8N.

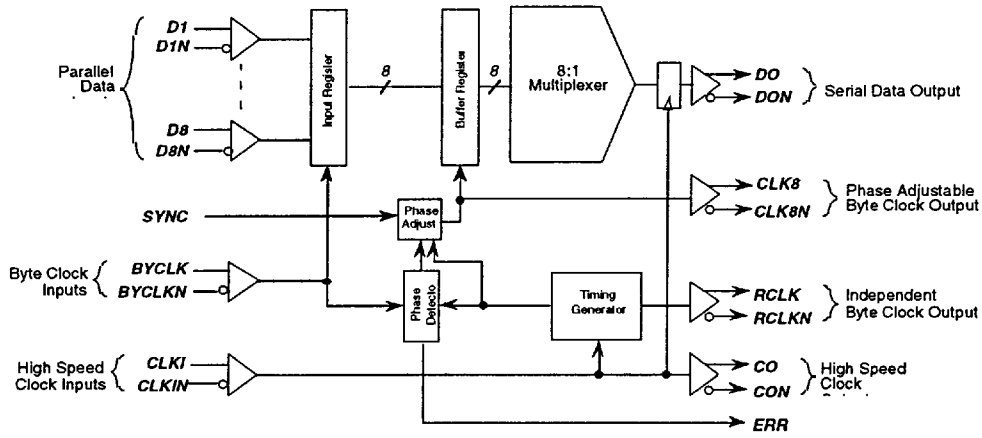
Internal circuitry monitors the internal and external byte clocks and generates an ERR signal if a timing violation is detected. This signal can be gated to the SYNC input which is edge sensitive high. An active SYNC input allows the VS8021 timing to shift, positioning it properly against the external byte clock, CLK8, CLK8N. When a CLK8 timing switch is made, normal data flow will be invalid for 1 byte.

There are two clock inputs, namely the CLKI and BYCLK, going into the VS8021. These two clocks serve as timing references for different parts of the VS8021. The BYCLK is used to trigger the input registers for the parallel data inputs, while the CLKI is used to trigger the high speed serial output register as well as some of the timing circuitry for the parallel to serial conversion. Furthermore, in order to make this part easy to use, the user is not required to assume a known phase relationship between CLKI and the BYCLK.

An internal Phase Detector and Phase Adjust Circuit are used to facilitate the two asynchronous circuits to work with each other. The Phase Detector and the Phase Adjust Circuit work together to adjust the internal clock CLK8 to make sure the set up and hold conditions are met for the internal registers. CLK8 is derived from CLKI and the RCLK is a non-phase varying byte clock output. The edge sensitive SYNC signal is simply the control signal that enables the Phase Detector circuitry.

As a summary, the CLKI is the high speed clock input. The BYCLK is the external byte clock. The CLK8 is the internal byte clock derived from CLKI, phase-adjusted if SYNC is enabled. The RCLK is a non-phase-adjusted divided-by-8 clock generated from CLKI. The phase of RCLK, RCLKN is not affected by the self-adjusting circuitry, therefore it can be used as a system reference clock. RCLK, RCLKN can be used by the system designer to generate BYCLK, BYCLKN. The self-positioning timer and RCLK, RCLKN allow for the creation of very tight parallel data timing for the VS8021.

**Figure 1: VS8021 Block Diagram**



**Data Sheet**

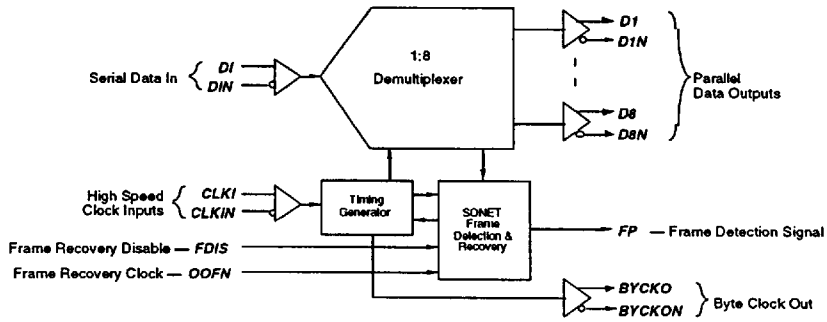
*2.5 Gbits/sec SONET Compatible*
*8-bit Mux/Demux Chipset*

## VS8022

The VS8022 contains both a 1:8 demultiplexer and SONET frame recovery circuitry. The 1:8 demultiplexer accepts a serial data input (DI, DIN) at rates up to 2.5 Gbits/second and converts it into 8 parallel differential ECL data outputs (D1-D8, D1N-D8N) at rates up to 312.5 Mbits/sec. Valid parallel data outputs are indicated by the divide by 8 differential clock outputs BYCKO, BYCKON.

The VS8022 also contains a SONET frame recovery circuit. The frame recovery circuits are enabled by a falling edge on the OOFN ECL input when the FDIS input is low. Once enabled, the frame recovery circuit starts looking for the SONET framing sequence. Once the frame is detected, the word boundary is realigned, a confirmation signal is sent off-chip through the FP ECL output and the frame recovery circuits are disabled. While the frame aligner is hunting for the frame, BYCKO, BYCKON and parallel data are invalid.

**Figure 2: VS8022 Block Diagram**




Frame recovery circuits are disabled by frame detection (resulting in FP) or by a falling edge on the OOFN input while FDIS is high.

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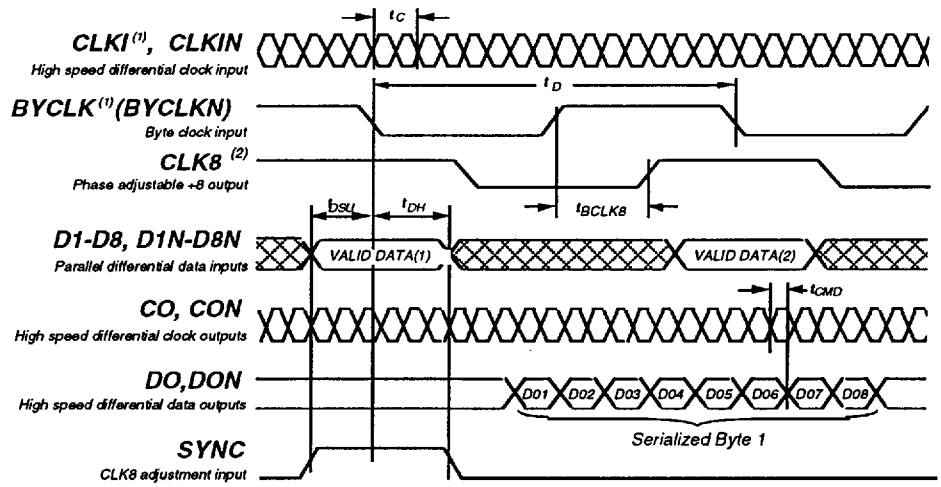
## VS8021 Multiplexer AC Characteristics *(Over recommended operating conditions)*

| Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_C$ (1) | Clock period | 400 | - | - | ps |
| $t_D$ | BYTE clock period ($t_D = t_C \times 8$) | 3.2 | - | - | ns |
| $t_{DSU}$ | Parallel data set-up time | 0.6 | - | - | ns |
| $t_{DH}$ | Data hold time | 1.4 | - | - | ns |
| $t_{CMD}$ | High speed clock output (CO, CON) timing, falling edge of CO to muxed data output, (DO, DON) timing | 220 | - | 350 | ps |
| $t_{BCLK8}$ (2) | Byte clock to CLK8 timing | 0.5 | 1.0 | 1.5 | ns |
| jitter(pk-to-pk) | CLKI, CLKIN to DO, DON (max-min), (HI to LO), same part, same pin at constant conditions | - | <50 | - | ps |

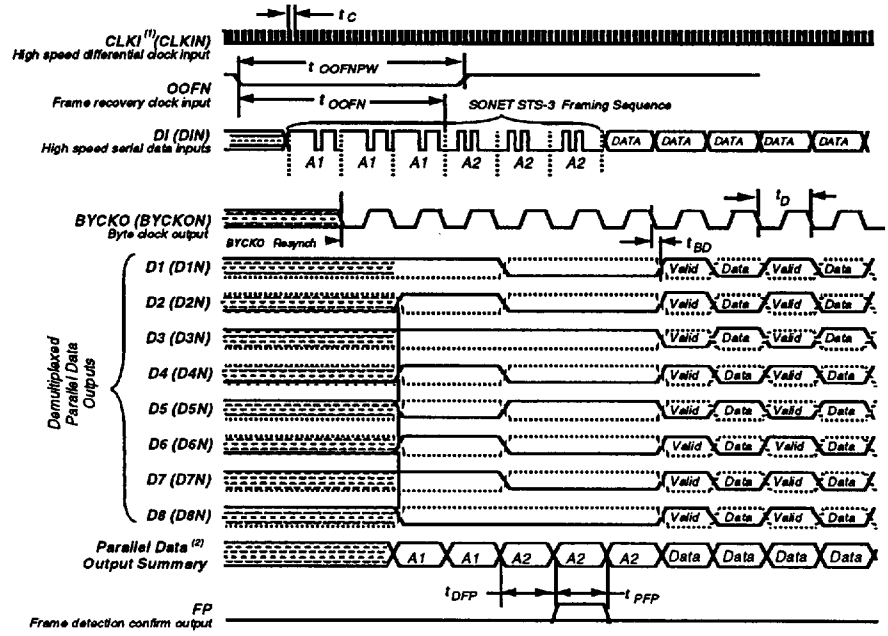
*Note: (1) The parts are guaranteed by design to operate from DC to a maximum frequency of 2.5 GHz.*
*(2) Required when SYNC not connected to ERR*

**Figure 3: VS8021 Multiplexer Waveforms**




*NOTES: (1) Negative edge is active edge.*
*(2) BYCLK/CLK8 timing required when SYNC not connected to ERR.*
*CLKI (CLKIN) period x 8 = BYCLK (BYCLKN) period.*
*= Don't care.*

**Figure 4: VS8022 Demultiplexer Waveforms**




*NOTES:*

*1) Negative edge is active edge.*

*2) The parallel data outputs only begin showing valid data after the last A2 of the SONET framing sequence. The example waveforms shown above use an STS-3 framing sequence for convenience, thus valid data is output after the third A2 in the sequence.*

= *Don't care.*

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## VS8022 Demultiplexer AC Characteristics *(Over recommended operating conditions)*

| Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_C$ | Clock period * | 400 | - | - | ps |
| $t_D$ | BYTE clock period ($t_D = t_C$ x 8) (framed) | 3.2 | - | - | ns |
| $t_{BD}$ | BYTE clock output to valid data | 0.5 | 1.0 | 2.0 | ns |
| $t_{DFP}$ | FP rising edge from parallel data output change from A1 to A2 ($t_{DFP} = t_D$) | - | 3.2 | - | ns |
| $t_{PFP}$ | FP pulse width ($t_{PFP} = t_D$) | 3.2 | - | - | ns |
| $t_{OOFN}$ | OOFN falling edge before A1 changes to A2 ($t_{OOFN} = t_D$ x 4) | 12.8 | - | - | ns |
| $t_{OOFNPW}$ | OOFN pulse width ($t_{OOFNPW} = t_D$) | 3.2 | - | - | ns |
| Phase Margin | Serial data phase timing margin with respect fo high speed clock: *Phase Margin* = $\left(1 - \frac{t_{SU} + t_H}{t_C}\right)360°$ | 135 | 180 | - | degrees |

*Note: If $t_c$ changes, all the remaining parameters change as indicated by the equations.*

## VS8022 SONET Frame Recovery and Detection

The SONET framing sequence is a string of A1 bytes followed by a string of A2 bytes. (A1 = 11110110 and A2 = 00101000) The first serial bit starts at the left of the byte. The table below shows the number of A1 and A2 bytes in each SONET frame for different line rates. The VS8022 contains a frame recovery circuit and a frame detection circuit..

| STS Level | Line Rate (Mb/s) | # of A1 Bytes | # of A2 Bytes |
|---|---|---|---|
| STS-3 | 155.520 | 3 | 3 |
| STS-12 | 622.080 | 12 | 12 |
| STS-48 | 2488.32 | 48 | 48 |

### Frame Recovery Circuit

The frame recovery circuit is designed to scan the serial data stream, looking for the A1 byte. When it finds the A1 pattern, it adjusts internal timing so that the serial data is properly demultiplexed onto the eight parallel outputs. Subsequently, the MSB of the A1 byte will appear in the D1 position and LSB of the A1 byte will appear in the D8 position. This word boundary alignment causes the BYCKO, BYCKON output to be resynchronized. While the frame aligner is hunting for the frame, BYCKO and parallel data are invalid. Frame recovery circuits are disabled by frame detection (resulting in FP) or by a falling edge on the OOFN input while FDIS is high.

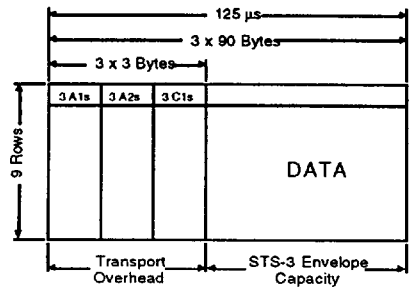
### Frame Detection Circuit

The frame detection circuit monitors the demultiplexed data, and senses the boundary between A1 and A2 bytes. This pulse on the FP output will reset the frame recovery circuit, so that no further resynchronization will occur until permission is given through OOFN.

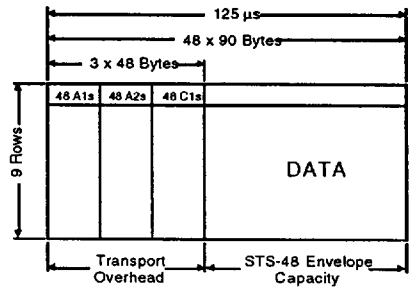
### Circuit Operation

The frame recovery circuits are initialized and enabled on the falling edge of the OOFN ECL input with FDIS held low. The OOFN must be at least one byte clock period wide. It must occur at least four byte clock periods before the A1/A2 boundary. The circuit requires at least three A1 bytes followed by 3 A2 bytes for successful alignment. The first A1 byte is used by the frame recovery circuit to obtain initial word boundary alignment, while the following two A1 and three A2 bytes are used to reset the frame recovery circuit and maintain alignment for the subsequent bit stream. Frame recognition will occur for each word boundary aligned A1A1A2A2A2 sequence in the data stream. Frame recognition is signaled by a one byte clock period high pulse on the FP ECL output pin. This FP pulse will appear one byte period after the first A2 byte appears on the parallel data output pins.

*STS-3 Frame*




*STS-48 Frame*




*Note: A1's and A2's: SONET framing sequence*
*C1's: STS Frame ID*

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## Absolute Maximum Ratings(1)

Power Supply Voltage ($V_{TT}$) ..... -3.0V to + 0.5V
Power Supply Voltage ($V_{EE}$) ..... $V_{TT}$ + 0.7V to -6.0V
ECL Input Voltage Applied (2) ($V_{ECLIN}$) ..... -2.5V to + 0.5V
High Speed Input Voltage Applied (2) ($V_{HSIN}$) ..... $V_{EE}$ -0.7V to $V_{CC}$ + 0.7V
Output Current (DC, output HIGH) ($I_{OUT}$) ..... -50 mA
Case Temperature Under Bias ($T_C$) ..... -55° to + 125°C
Storage Temperature (3) ($T_{STG}$) ..... -65° to + 150°C

## Recommended Operating Conditions

ECL Power Supply Voltage (4) ($V_{TT}$) ..... -2.0V ± 0.1V
Power Supply Voltage ($V_{EE}$) ..... -5.2V ± 0.26V
Operating Temperature Range (3) ($T$) ..... (Commercial) 0° to 70°C, (Industrial) -40° to + 85°C

*Notes: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*

*(2) $V_{TT}$ must be applied before any input signal voltage magnitude ( $|V_{ECLIN}|$ and $|V_{HSIN}|$ ) can be greater than $|V_{TT}$ -0.5V.|*

*(3) Lower limit of specification is ambient temperature and upper limit is case temperature.*

*(4) When using internal ECL 100K reference level.*

## DC Characteristics

### Table 1: Low Speed ECL Inputs and Outputs

*(Over recommended operating range with internal $V_{REF}$, $V_{CC}$ = GND, Output load = 50 Ω to -2.0V)*

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH voltage | -1020 | - | -700 | mV | $V_{IN} = V_{IH}$ (max) or $V_{IL}$ (min) |
| $V_{OL}$ | Output LOW voltage | $V_{TT}$ | - | -1620 | mV | $V_{IN} = V_{IH}$ (max) or $V_{IL}$ (min) |
| $V_{IH}$ | Input HIGH voltage | -1150 | - | -600 | mV | Guaranteed HIGH signal for all inputs |
| $V_{IL}$ | Input LOW voltage | $V_{TT}$ | - | -1500 | mV | Guaranteed LOW signal for all inputs |
| $\Delta V_{OUT}$ | Output voltage swing | 0.8 | 1.0 | 1.4 | V | Output load 50Ω to $V_{TT}$ |

*Note: Differential ECL output pins must be terminated identically.*

### Table 2: Power Dissipation

*(Over recommended operating conditions, $V_{CC}$ = GND, outputs open circuit)*

| Parameter | Description | VS8021 (Min) | VS8021 (Typ) | VS8021 (Max) | VS8022 (Min) | VS8022 (Typ) | VS8022 (Max) | Units |
|---|---|---|---|---|---|---|---|---|
| $I_{EE}$ | Power supply current from $V_{EE}$ | - | 400 | 600 | - | 450 | 600 | mA |
| $I_{TT}$ | Power supply current from $V_{TT}$ | - | 110 | 200 | - | 120 | 200 | mA |
| $P_D$ | Power dissipation | | 2.3 | 3.75 | - | 2.6 | 3.75 | W |

### Table 3: High Speed Inputs and Outputs

*(Over recommended operating conditions, $V_{CC}$ = GND, Output load = 50 Ω to -2.0V)*

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $\Delta V_{IN}$ | Input voltage swing | 0.8 | 1.0 | 1.2 | V | AC Coupled |
| $V_{OH}$ | Output HIGH voltage | - | -0.9 | - | V | Output load, 50 Ω to -2.0V |
| $V_{OL}$ | Output LOW voltage | - | -1.8 | - | V | Output load, 50 Ω to -2.0V |
| $\Delta V_{OUT(data)}$ | Output voltage swing for data | 0.6 | 0.8 | 1.2 | V | Output load, 50 Ω to -2.0V |
| $\Delta V_{OUT(clk)}$ | Output voltage swing for clock | 0.6 | 0.7 | 1.2 | V | Output load, 50 Ω to -2.0V |

*Notes: 1) A reference generator is built in to each high speed input, and these inputs are designed to be AC coupled.*

*2) If a high speed input is used single-ended, a 150 pF capacitor must be connected between the unused high speed or complement input and the power supply ($V_{TT}$).*

*3) Differential high speed outputs must be terminated identically.*

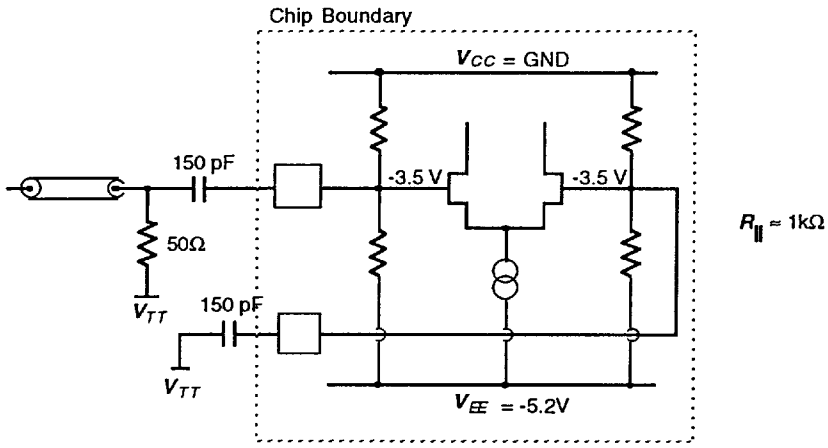
*4) ESD protection is minimal for the high speed input pins, therefore, proper procedures should be used when handling this product*

### High Speed Inputs

In the past, the high speed inputs, which are typically used for serial data and high speed clock inputs with frequencies greater than 1Ghz, were specified with absolute minimum and maximum voltage values. Since these inputs are intended for AC coupled applications, they have been re-specified in terms of a voltage swing ($\Delta V_{IN}$).

High speed clocks are intended for AC coupled operation. In most situations high speed serial data will have high transition density and contain no DC offsets, making them candidates for AC coupling as well. However, it is possible to employ DC coupling when the serial input data contains a DC component.

The structure of the high speed input circuit is shown below. DC coupled circuits may be used to operate this input provided that the input swing is centered around the reference voltage. Since the internal resistor divider which forms the -3.5V reference presents an attenuation factor of only 0.6 to the $V_{EE}$ power supply, it is recommended that, in single-ended DC coupling situations, the user provide an external reference which has better temperature and power supply rejection than the simple on chip resistive attenuator. This external reference should have a nominal value of -3.5 V and can be connected to the complimentary input. This complication can be avoided in DC coupled situations by using differential signals.



## Example Application: STS-48 SONET System Link

The objective in this example is to multiplex/demultiplex 8 channels at the STS-48 line rate with SONET frame recovery capability. The system can be implemented using the VS8021 and VS8022 as follows:

### 8:1 Multiplexer

Data at a line rate of 311.04 Mbytes/sec is registered at the inputs using the externally provided 311.04 MHz byte clock. ERR is gated into SYNC which is edge triggered for retiming of the input word. The 2488.32 MHz clock is used to generate timing signals for the mutiplexing function. The muxed output at 2488.32 Mbits/sec is generated at the serial data output of VS8021.

### 1:8 Demultiplexer

The 1:8 demultiplexer receives serial data at 2488.32 Mbits/sec and generates parallel data at 311.04 Mbytes/sec along with a byte clock output of 311.04 MHz. The demux also has the SONET frame recovery and detection circuitry.

During system start-up OOFN input receives a falling edge from the system control to permit recovery of the SONET frame and align on byte boundaries. Once the frame is aligned, the FP pulse is generated on every SONET frame. If for any reason the FP pulse disappears on frame boundaries then this signals the system that the frame synchronization is lost. The system then asserts the OOFN input (High to Low) to recover the SONET frame and align on byte boundaries, bringing the system back to a synchronized condition. After synchronization is achieved, the FP pulse starts again on every frame.

### ESD Protection

Electrostatic discharge protection is provided for ECL I/O's and high speed clock and data I/O's to the following minimum limits:

ECL I/O ..... *1000V*
High Speed Clock and Data Inputs ..... *500V*

**Figure 5: STS-48 SONET System Link**

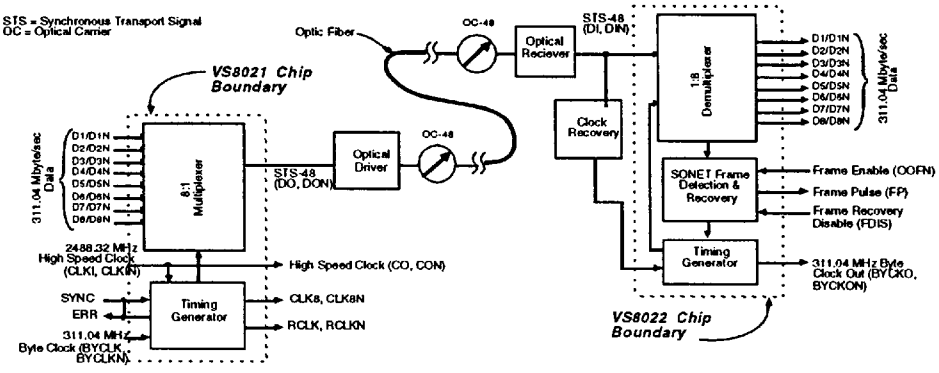


**Figure 6: VS8021 Pin Diagram**

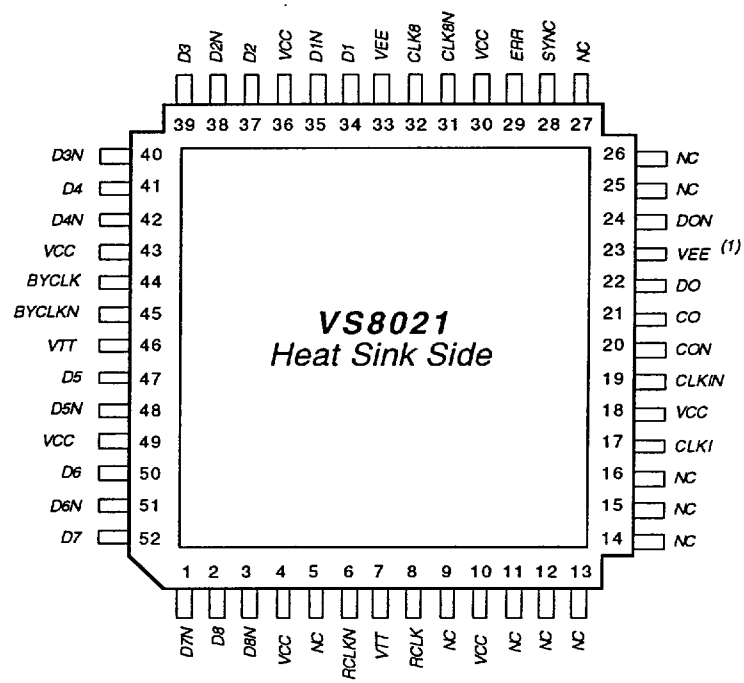


**Table 4: VS8021 Pin Description.**

| Pin # | Name | I/O | I/O Type | Description |
|---|---|---|---|---|
| 1-3, 34, 35, 37-42,47, 48, 50-52 | D1-D8, D1N-D8N | I | ECL | Parallel ECL differential datas inputs |
| 17, 19 | CLKI, CLKIN | I | HS | High speed differential clock inputs |
| 44, 45 | BYCLK, BYCLKN | I | ECL | Divide by 8 clock ECL input |
| 22, 24 | DO, DON | O | HS | High speed serial data output |
| 21, 20 | CO, CON | O | HS | High speed differential clock output |
| 32, 31 | CLK8, CLK8N | O | ECL | Phase adjustable CLK + 8 differential ECL clock output |
| 8, 6 | RCLK, RCLKN | O | ECL | Independent CLK + 8 differential ECL clock output |
| 29 | ERR | O | ECL | Error detection ECL output |
| 28 | SYNC | I | ECL | Error correction ECL input |
| 4, 10, 18, 30 ,36, 43, 49 | $V_{CC}$ | | | Ground connection |
| 7, 46 | $V_{TT}$ | | | -2.0V supply for internal reference generation & low power logic |
| 23(1), 33 | $V_{EE}$ | | | -5.2V supply for high speed logic |
| 5, 9, 11-16, 25, 26, 27 | NC | | | No connection |

*Note: 1) Pin #23 on both parts is connected to the heat sink. Connect to VEE or most negative chip voltage.*

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**Figure 7: VS8022 Pin Diagram**

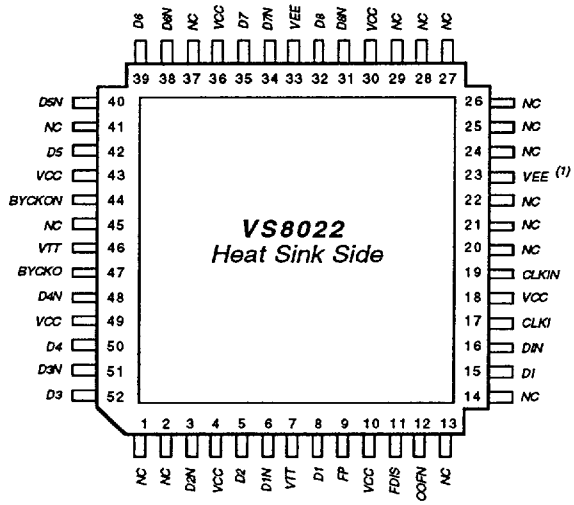



**Table 5: VS8022 Pin Description**

| *Pin #* | *Name* | *I/O* | *I/O TYPE* | *Description* |
|---|---|---|---|---|
| 3, 5, 6, 8, 31, 32, 34, 35, 38-40, 42, 48, 50-52 | D1-D8, D1N-D8N | O | ECL | Parallel ECL differential data outputs |
| 17, 19 | CLKI, CLKIN | I | HS | High speed differential clock inputs |
| 47, 44 | BYCKO, BYCKON | O | ECL | Divide by 8 clock ECL outputs |
| 15, 16 | DI, DIN | I | HS | High speed differential serial data inputs |
| 11 | FDIS | I | ECL | Frame recovery disable input |
| 12 | OOFN | I | ECL | Frame recovery enable ECL input |
| 4, 10, 18, 30, 36, 43, 49 | $V_{CC}$ | I | | Ground connection |
| 7, 46 | $V_{TT}$ | | | -2.0V supply for internal reference generation & low power logic |
| 23(1), 33 | $V_{EE}$ | | | -5.2V supply for high speed logic |
| 1, 2, 13, 14, 20-22, 24-29, 37, 41, 45 | NC | | | No connection |

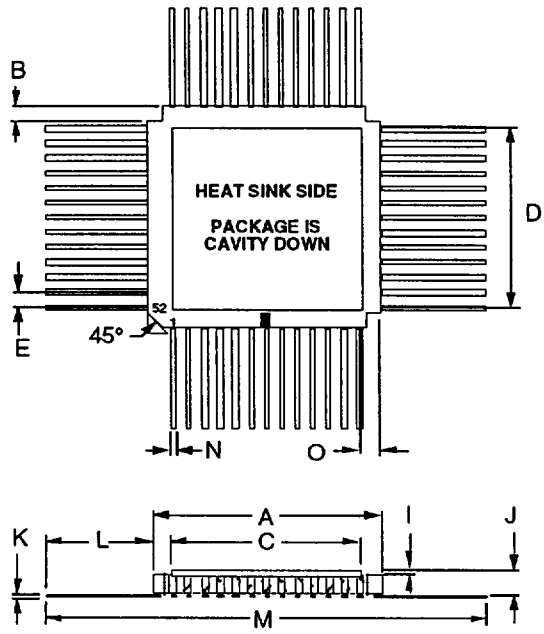
*Note: 1) Pin #23 on both parts is connected to the heat sink. Connect to VEE or most negative chip voltage.*

**Data Sheet**

*2.5 Gbits/sec SONET Compatible*
*8-bit Mux/Demux Chipset*



## Package Information




*52-Pin Leaded*
*Ceramic Package (LDCC)*

*NOTES:*
*Drawing not to scale.*
*Packages: Ceramic (alumina);*
*Heat sink: Copper-tungsten;*
*Leads: Alloy 42 with gold plating.*

| *Item* | *mm (Min/Max)* | *in (Min/Max)* | *Item* | *mm (Min/Max)* | *in (Min/Max)* |
|---|---|---|---|---|---|
| A | 18.54/19. 56 | 0.730/0.770 | I | 0.41/0.61 | 0.016/0.024 |
| B | 1.02/1.52 | 0.040/0.060 | J | 2.03/2.79 | 0.080/0.110 |
| C* | 15.49/16.51 | 0.610/0.650 | K* | 0.09/0.24 | 0.003/0.009 |
| D* | 15.24 TYP | 0.600 TYP | L | 4.57/5.34 | 0.180/0.210 |
| E | 1.27 TYP | 0.050 TYP | M | 27.69/30.22 | 1.090/1.190 |
| F | 0.76/1.02 | 0.030/0.040 | N | 0.36/0.56 | 0.014/0.022 |
| G | 16.94 TYP | 0.667 TYP | O | 1.75/1.90 | 0.069/0.075 |
| H | 1.91/2.41 | 0.075/0.095 | — | — | — |

**At package body.*





15

## DUT Boards

The VS8021/VS8022 DUT boards are special purpose circuit boards which provide a test bed suitable for evaluating the performance characteristics of the VS8021 8:1 Multiplexer or the VS8022 1:8 Demultiplexer in the 52 pin LDCC package.

The figure below is a schematic representation of these circuit boards. These boards provide a controlled impedance transmission line for all signals, and suitable decoupling for the power supplies. The signal traces have a characteristic impedance of 50Ω All ECL input lines are terminated with 50Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 150pF blocking capacitors as shown. These capacitors are shorted in applications which require DC connection to these inputs. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated in the measuring instrument such as an oscilloscope.

Normally, the VS8021 and VS8022 circuits operate in an ECL environment with standard ECL power buses: 0V, -2V, -5.2V. In order to simplify interface to standard ground referenced test equipment, however, the circuit board power buses are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power bus. The device to be tested is held in place with a pressure retaining fixture. The figures on the following two pages indicate the physical dimensions and the connections labels for the evaluation boards.

**Figure 8: VS8021/VS8022 DUT Board Schematics**

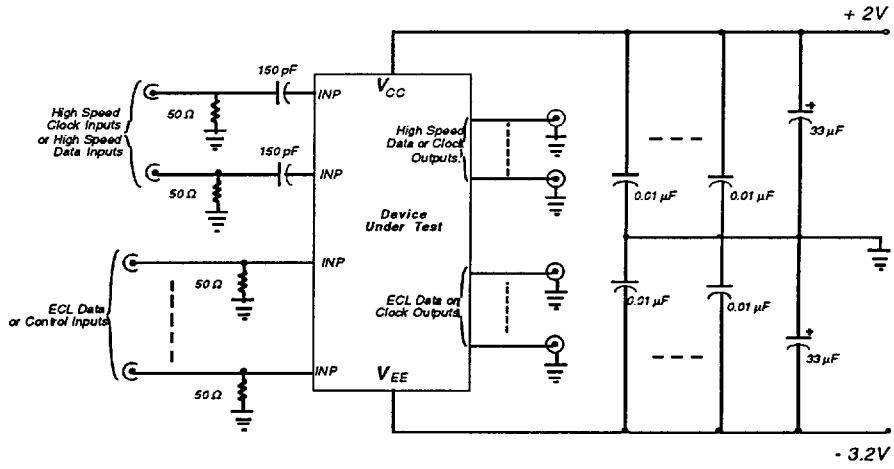


**Figure 9: VS8021 DUT Dimensions and Connection Diagram**

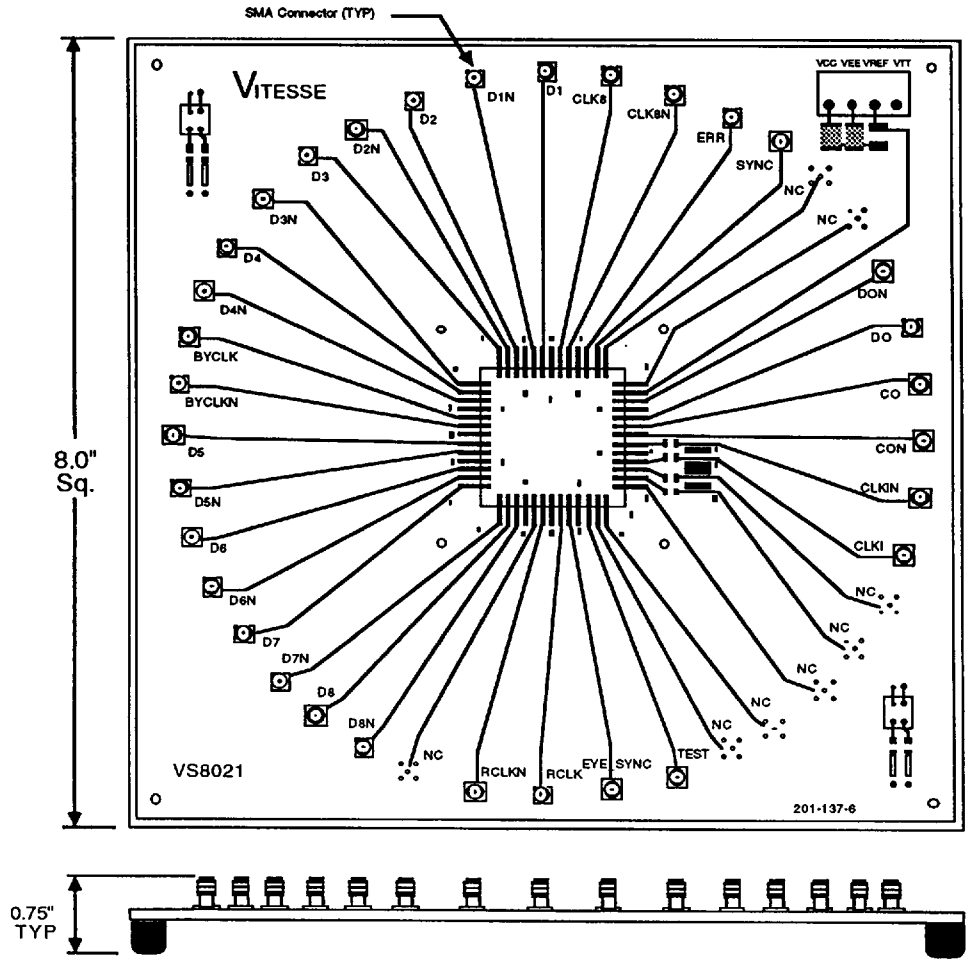
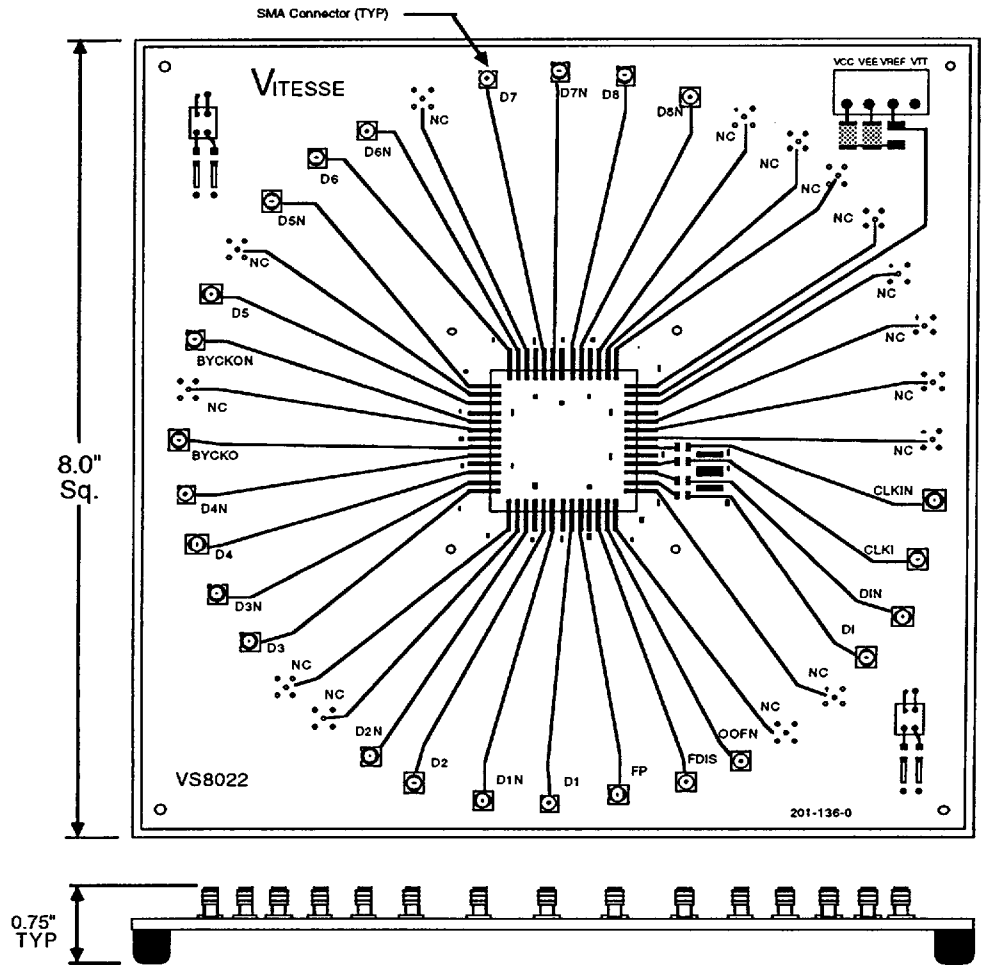


**Figure 10: VS8022 DUT Dimensions and Connection Diagram**



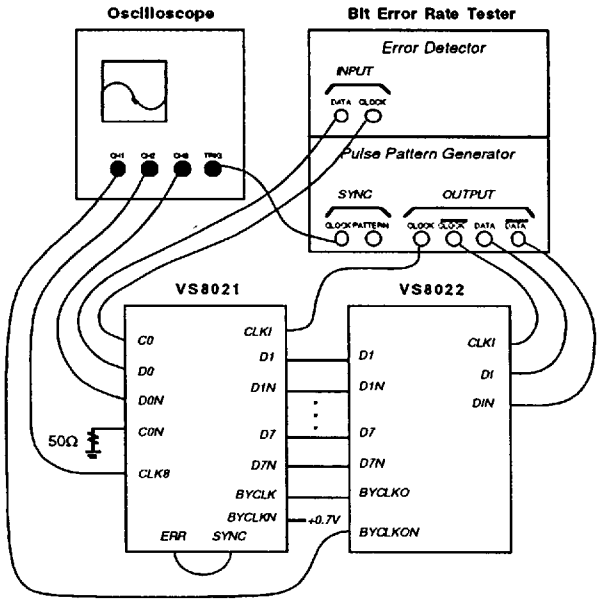
## DUT Test Setup

Test equipment that is equal to or better than the following is recommended for testing the VS8021 and VS8022 DUT boards:

- 5 GHZ Oscilloscope
- 2.5 GHz Bit Error Rate Tester
- Power Supplies
  -3.2 V, 1 Amp per board
  +2.0 V, 1 Amp per board

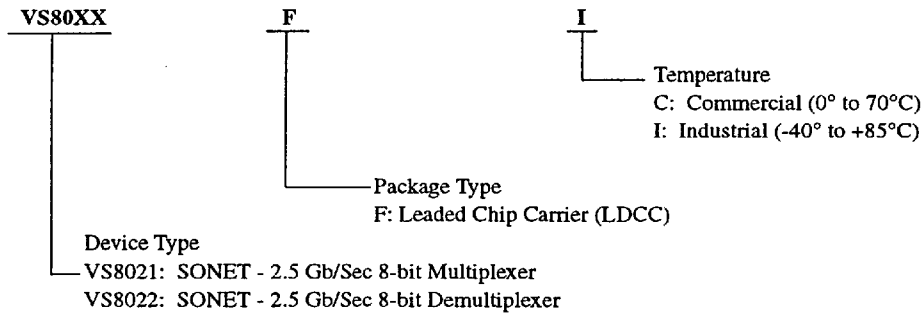
The figure below shows one possible test setup for the VS8021 and VS8022 DUT boards. In this configuration the Bit Error Rate Tester sends a clock and serial bit pattern into the VS8022 DUT board. This data is demultiplexed into a byte wide pattern which is transferred via matched cables to the VS8021 DUT board where the byte wide data is multiplexed into a serial bit stream which is sent into the error detector. The bit error rate tester will verify that the bit stream that is sent out of the generator matches the bit stream that is fed back into the error detector. Always use matched delay cables between complementary signals and between data and clock signals. The oscilloscope can be used to view signal integrity of various signals and to monitor rise and fall times.

**Figure 11: VSC8021/8022 DUT Test Setup**



## Ordering Information

Vitesse products are available in a variety of packages and operating ranges. The order number for this product is formed by using a combination of the following: *Device Type, Package Type, and Operating Temperature Range.*




### Notice

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