

**SWITCHING**  
**N-CHANNEL POWER MOS FET**  
**INDUSTRIAL USE**

**Description**

The 2SK3114 is N-Channel DMOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

**Ordering Information**

Part Number	Package
2SK3114	Isolated TO-220

**Features**

- Low gate charge :  
 $Q_G = 15 \text{ nC TYP. (} V_{DD} = 450 \text{ V, } V_{GS} = 10 \text{ V, } I_D = 4.0 \text{ A)}$
- Gate voltage rating :  $\pm 30 \text{ V}$
- Low On-state resistance :  
 $R_{DS(on)} = 2.2 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 2.0 \text{ A)}$
- Avalanche Capability Ratings
- Isolated TO-220 package

**Absolute Maximum Ratings (T<sub>A</sub> = 25 °C)**

Drain to source voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	600	V
Gate to source voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±30	V
Drain current (DC) (T <sub>C</sub> = 25 °C)	I <sub>D(DC)</sub>	±4.0	A
Drain current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±16	A
Total power dissipation (T <sub>A</sub> = 25 °C)	P <sub>T1</sub>	2.0	W
Total power dissipation (T <sub>C</sub> = 25 °C)	P <sub>T2</sub>	30	W
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C
Single avalanche current <sup>Note2</sup>	I <sub>AS</sub>	4.0	A
Single avalanche energy <sup>Note2</sup>	E <sub>AS</sub>	10.7	mJ
Diode recovery dv/dt <sup>Note3</sup>	dv/dt	3.5	V/ns

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1 %

**2.** Starting T<sub>ch</sub> = 25 °C, V<sub>DD</sub> = 150 V, R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = 20 V → 0 V

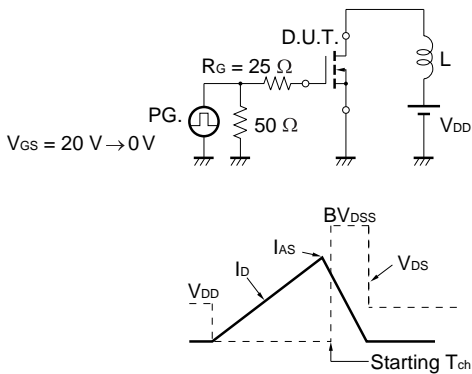
**3.** I<sub>F</sub> ≤ 2.0 A, V<sub>clamp</sub> = 600 V, di/dt ≤ 100 A / μs, T<sub>A</sub> = 25 °C

The information in this document is subject to change without notice

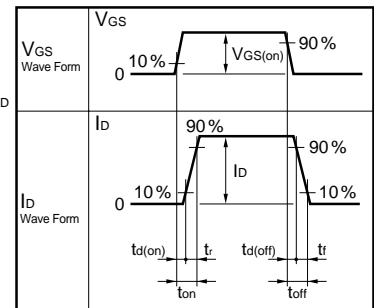
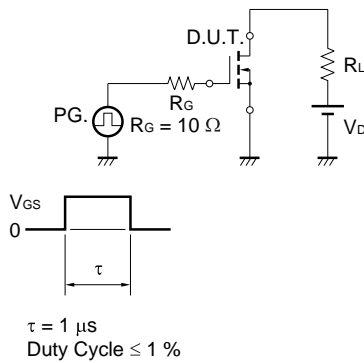
**Electrical Characteristics (T<sub>A</sub> = 25 °C)**

Characteristics	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Drain leakage current	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V
Gate leakage current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V
Gate cutoff voltage	V <sub>GS(off)</sub>	2.5		3.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward transfer admittance	y <sub>fs</sub>	1.0			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2.0 A
Drain to source on-state resistance	R <sub>DS(on)</sub>		1.6	2.2	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.0 A
Input capacitance	C <sub>iss</sub>		550		pF	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz
Output capacitance	C <sub>oss</sub>		115		pF	
Reverse transfer capacitance	C <sub>rss</sub>		13		pF	
Turn-on delay time	t <sub>d(on)</sub>		12		ns	V <sub>DD</sub> = 150 V, I <sub>D</sub> = 2.0 A, V <sub>GS(on)</sub> = 10 V, R <sub>G</sub> = 10 Ω, R <sub>L</sub> = 10 Ω
Rise time	t <sub>r</sub>		6		ns	
Turn-off delay time	t <sub>d(off)</sub>		35		ns	
Fall time	t <sub>f</sub>		12		ns	
Total gate charge	Q <sub>G</sub>		15		nC	V <sub>DD</sub> = 450 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.0 A
Gate to source charge	Q <sub>GS</sub>		4		nC	
Gate to drain charge	Q <sub>GD</sub>		4.4		nC	
Diode forward voltage	V <sub>F(S-D)</sub>		0.9		V	I <sub>F</sub> = 4.0 A, V <sub>GS</sub> = 0 V
Reverse recovery time	t <sub>rr</sub>		1.3		μs	I <sub>F</sub> = 4.0 A, V <sub>GS</sub> = 0 V, di/dt = 50 A/μs
Reverse recovery charge	Q <sub>rr</sub>		4.3		μC	

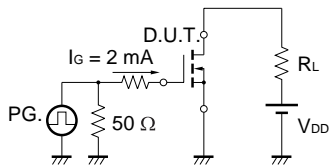
**Test Circuit 1 Avalanche Capability**



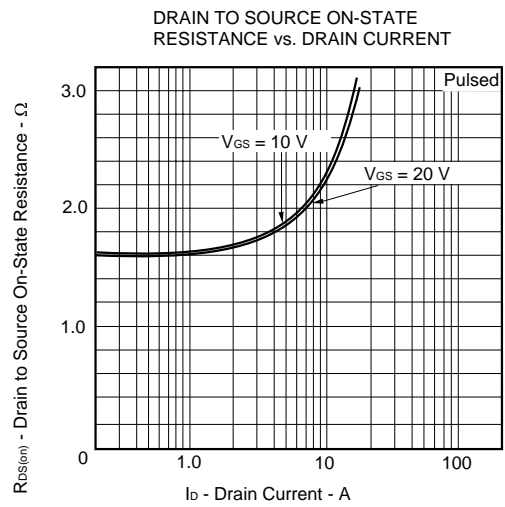
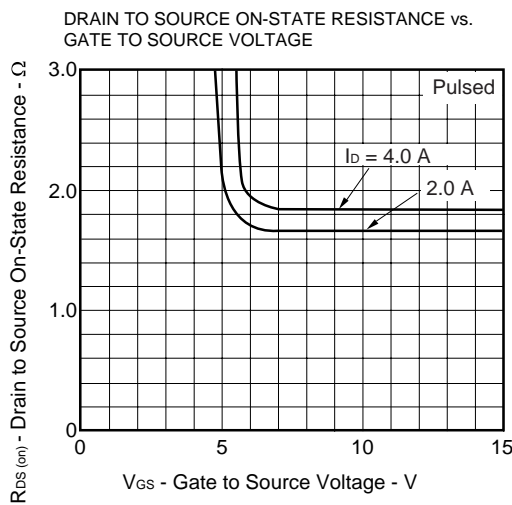
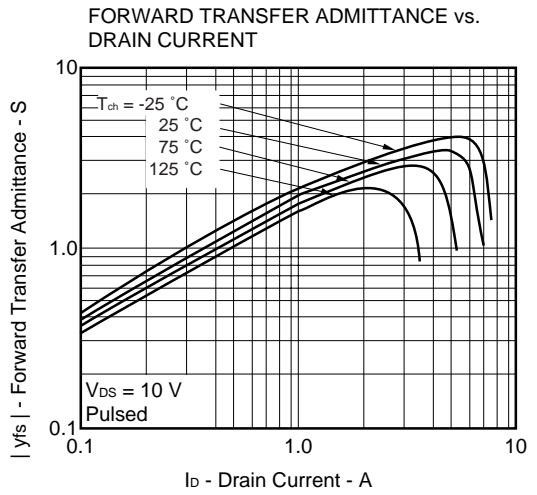
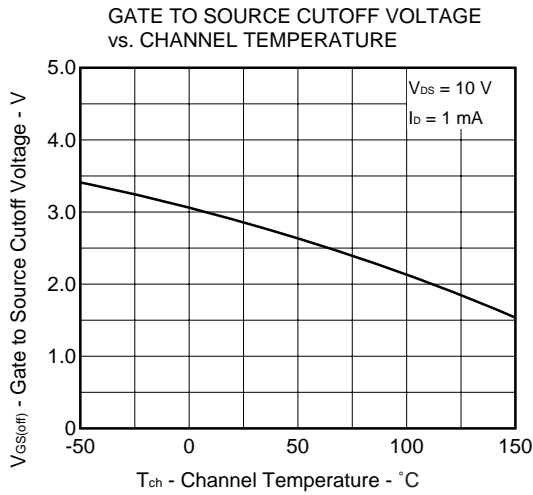
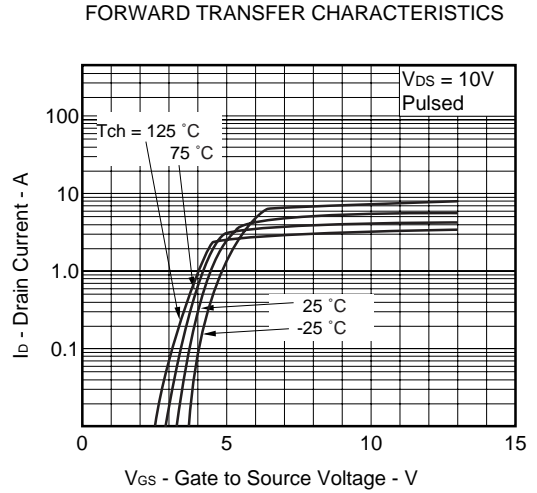
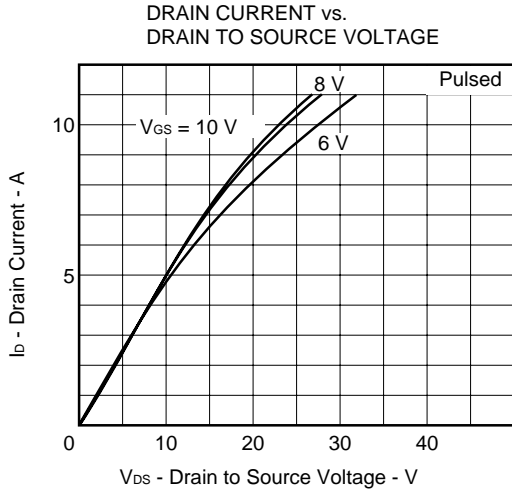
**Test Circuit 2 Switching Time**



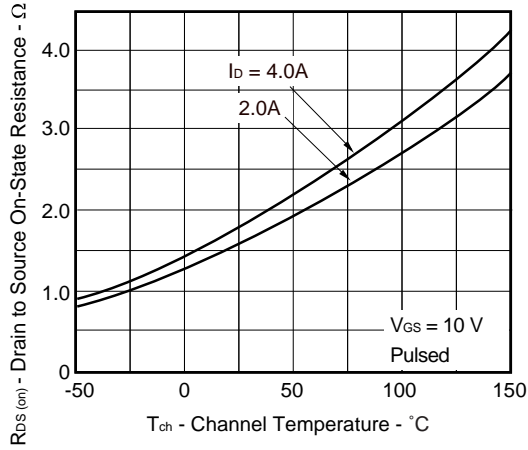
**Test Circuit 3 Gate Charge**



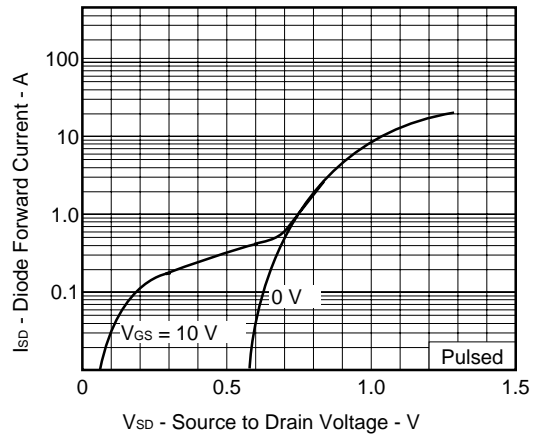
Typical Characteristics (T<sub>A</sub> = 25 °C)



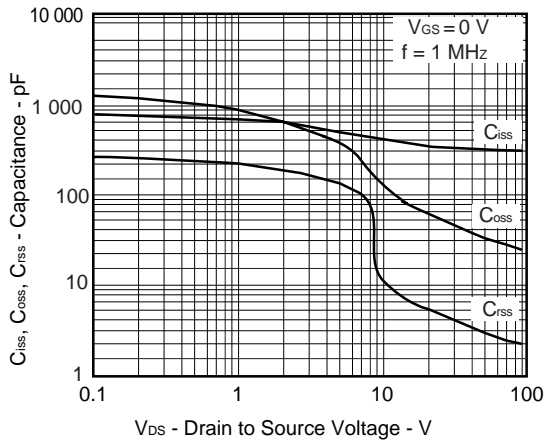
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



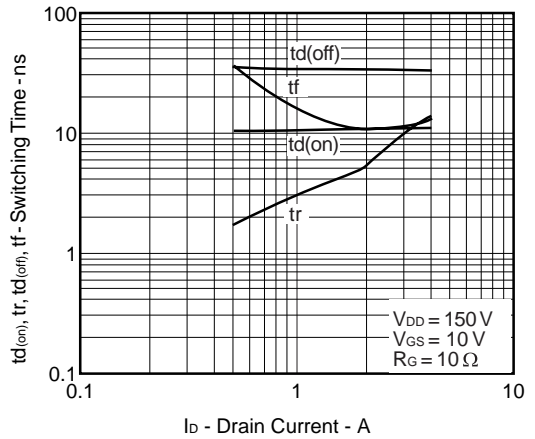
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



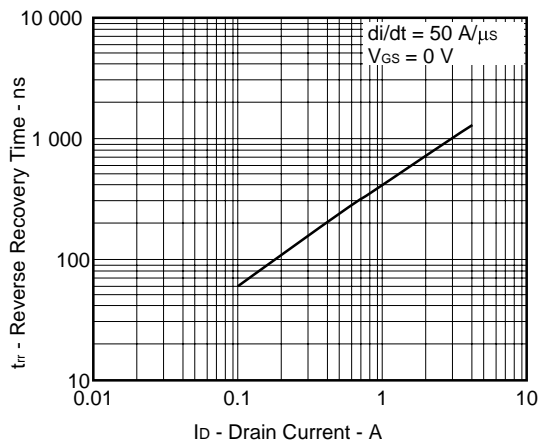
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



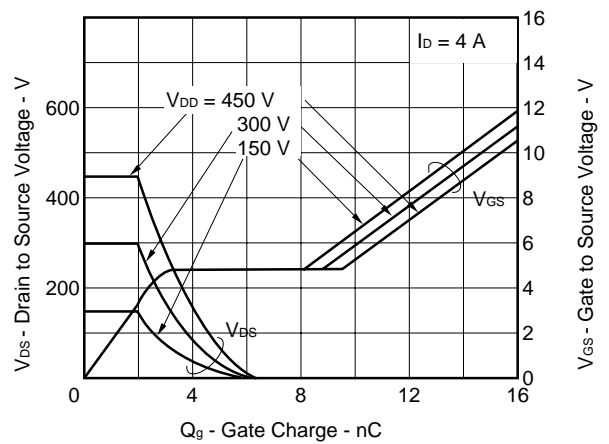
SWITCHING CHARACTERISTICS



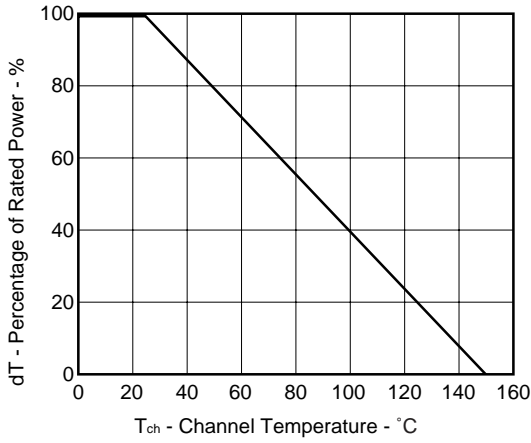
REVERSE RECOVERY TIME vs. DRAIN CURRENT



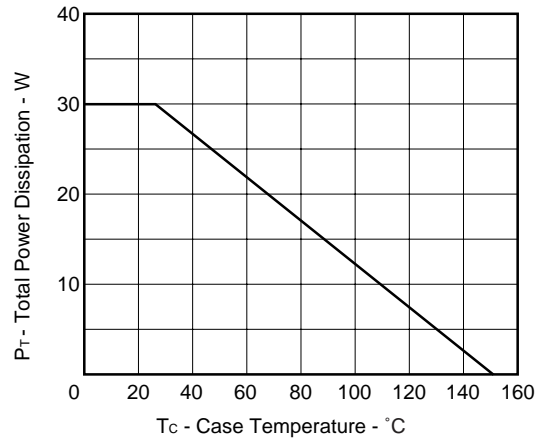
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



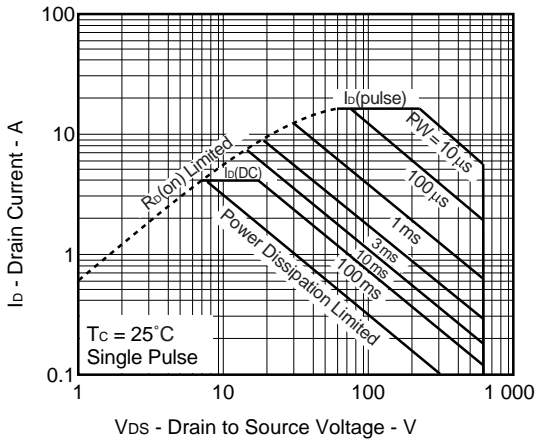
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



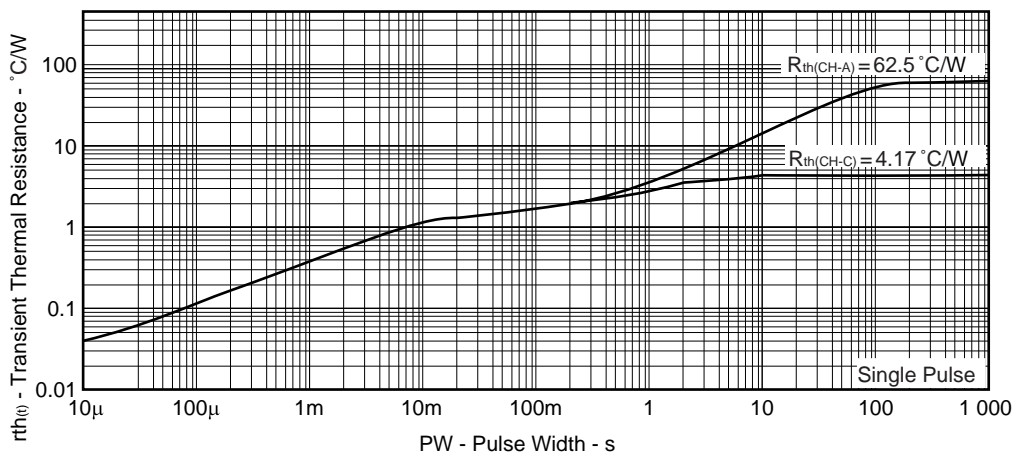
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

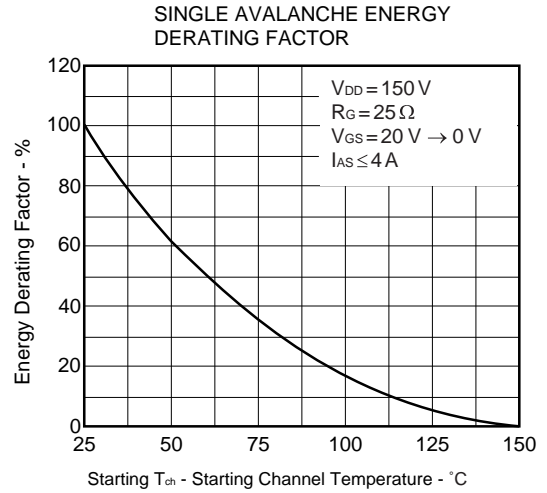
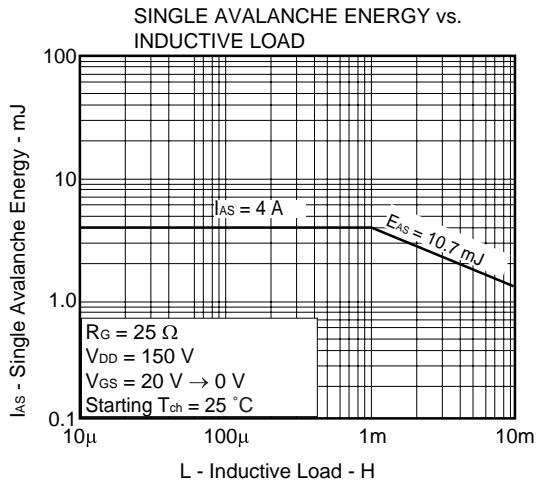


FORWARD BIAS SAFE OPERATING AREA



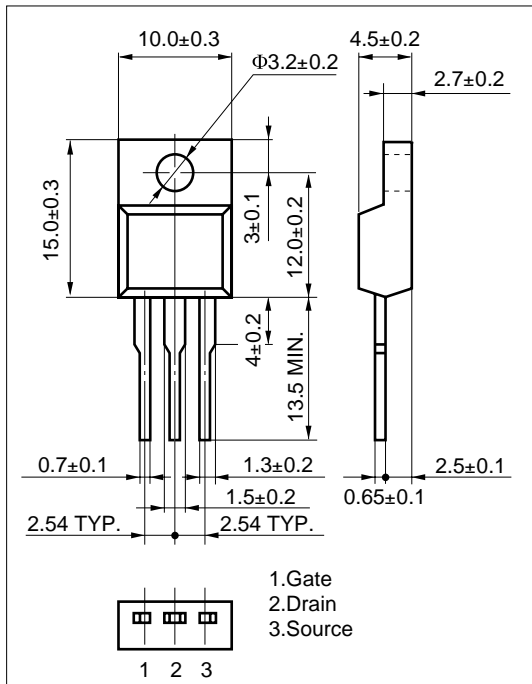
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



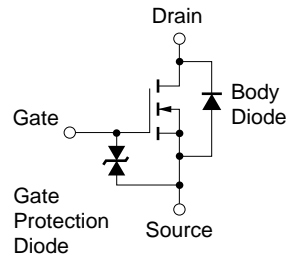


Package Drawing (Unit : mm)

Isolated TO-220 (MP-45F)



Equivalent Circuit



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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