CY7C4808V25
CY7C4806V25
CY7C4804V25

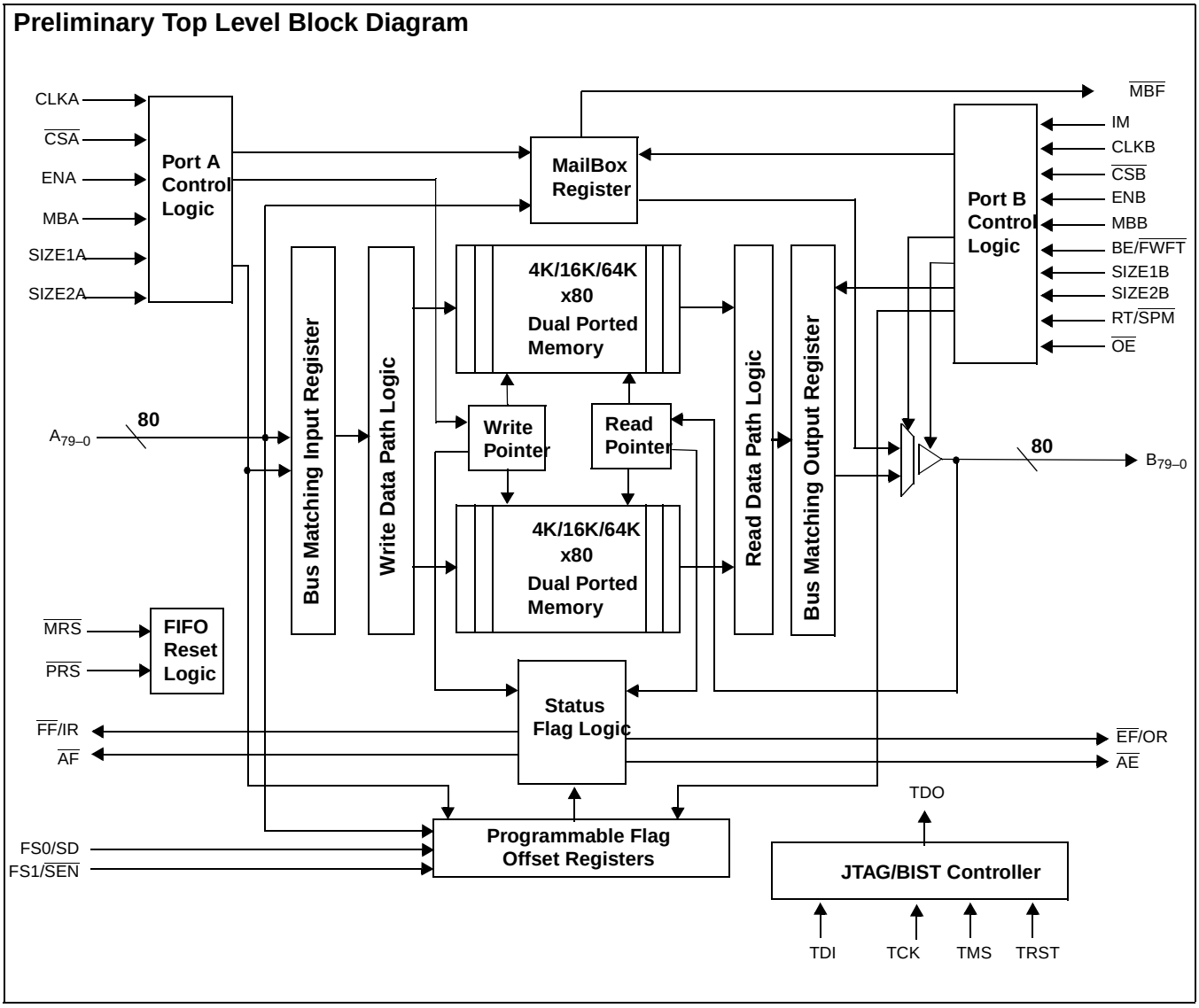
ADVANCE INFORMATION

2.5V 4K/16K/64K x 80 Unidirectional Synchronous FIFO w/Bus Matching

Features

- **High-speed, low-power, unidirectional, first-in first-out (FIFO) memories w/bus matching capabilities**
- **64K x 80 (CY7C4808V25)**
- **16K x 80 (CY7C4806V25)**
- **4K x 80 (CY7C4804V25)**
- **2.5V ± 125 mV power supply**
- **Fabricated using Cypress 0.21-micron CMOS Technology for optimum speed/power**
- **Individual clock frequency up to 200 MHz (5 ns read/write cycle times)**
- **High-speed access with t_A = 3.5**
- **Bus matching on both ports: x80, x40, x20, x10**
- **Free-running CLKA and CLKB. Clocks may be asynchronous or coincident**
- **CY standard or First-Word Fall-Through modes**
- **Serial and parallel programming of Almost Empty/Full flags, each with 3 default values (8, 16, 64)**
- **Master and Partial reset capability**
- **Retransmit capability**
- **All I/Os are 1.5V HSTL**
- **Big or Little Endian format on Port B**
- **288 FBGA 19 mm x 19 mm (1.0-mm ball pitch) packaging**
- **Width and depth expansion capability**

Preliminary Top Level Block Diagram



For the most recent information, visit the Cypress web site at www.cypress.com

Functional Description

The CY7C480XV25 family of FIFOs is high-speed, low-power, CMOS Synchronous (clocked) FIFO memories, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of the clock on either port by the enable signal. The clocks for each port are independent of one another and can be asynchronous or coincident. The enable for each port is arranged to provide a simple unidirectional interface between microprocessors and/or buses with synchronous control.

Two kinds of reset are available on the CY7C480XV25: Master Reset and Partial Reset. Master Reset initializes the read and write pointers to the first location of the memory array, configures the FIFO for Big Endian or Little Endian byte arrangement, selects the CY standard or First-Word Fall-Through (FWFT) mode, and determines the configuration of the programmable flags. The flags can be programmed either in serial mode or in parallel mode. The FIFO also comes with three possible default flag offset settings: 8, 16, or 64.

Partial Reset also sets the read and write pointers to the first location of the memory. Unlike Master Reset, any settings existing prior to Partial Reset (i.e., programming method and partial flag default offsets) are retained. Partial Reset is useful since it permits flushing of the FIFO memory without changing any configuration settings.

The CY7C480XV25 have two modes of operation: CY Standard Mode or First-Word Fall-Through Mode (FWFT). In the CY Standard Mode, the first word written to an empty FIFO is deposited into the memory array. A read operation is required to access that word (along with all other words residing in memory). In the FWFT Mode, the first long-word (80-bit-wide) written to an empty FIFO appears automatically on the outputs, and no read operation is required. Nevertheless, accessing subsequent words does necessitate a formal read request. FWFT mode is primarily used for cascading 2 or more FIFOs.

The FIFO has an $\overline{EF}$_OR flag on port B and $\overline{FF}$_IR flag on Port A. The $\overline{EF}$ and $\overline{FF}$ functions are selected in the CY Standard Mode. $\overline{EF}$ indicates whether or not the FIFO memory is empty. $\overline{FF}$ shows whether or not the memory is full. The IR and OR functions are selected in the First-Word Fall-Through mode. IR indicates whether or not the FIFO has memory locations available. OR shows whether the FIFO has data available for reading or not. It marks the presence of valid data on the outputs.

The FIFO has a programmable Almost Empty flag ($\overline{AE}$) and a programmable Almost Full flag ($\overline{AF}$). $\overline{AE}$ indicates the number of words left in the FIFO memory is at the user-defined amount. $\overline{AF}$ indicates the number of words written into the FIFO memory has achieved a predetermined amount.

$\overline{FF}$_IR and $\overline{AF}$ flags are synchronized to port A clock that writes data into its array. $\overline{EF}$_OR and $\overline{AE}$ flags are synchronized to Port B clock that reads data from its array. Programmable offsets for $\overline{AE}$ and $\overline{AF}$ are loaded in parallel via Port A or in serial via the SD input. The Serial Programming Mode pin ($\overline{SPM}$) makes this selection. Three default offsets setting are also provided. The $\overline{AE}$ threshold can be set at 8, 16 or 64 locations from the empty boundary and $\overline{AF}$ threshold can be set at 8, 16, or 64 locations from the full boundary. All these choices are made using the FS0 and FS1 inputs during Master Reset.

Two or more devices may be used in parallel to create wider data paths. If, at any time, the FIFO is not actively performing a function, the chip will automatically power down. During the Power-Down state, supply current consumption (I_{CC}) is at a minimum. Initiating any operation (by activating control inputs) will immediately take the device out of the Power-Down state.

The CY7C480XV25 FIFOs are characterized for operation from 0°C to 70°C commercial, and from –40°C to 85°C industrial.

Selection Guide

	CY7C480XV25-200	CY7C480XV25-166
Maximum Frequency (MHz)	200	166
Maximum Access Time (ns)	3.5	4
Minimum Cycle Time (ns)	5	6
Minimum Data or Enable Set-Up (ns)	0.6	0.6
Minimum Data or Enable Hold (ns)	0.6	0.6
Maximum Flag Delay (ns)	3.5	4

	CY7C4808V25	CY7C4806V25	CY7C4804V25
Density	64K x 80	16K x 80	4K x 80
Package	288 FBGA	288 FBGA	288 FBGA

Pin Description

Pin	Description
V_{CC_IO}	Power supply for I/Os
GND_io	Ground pins for I/Os
V_{CC_INT}	Power supply for internal logic
GND_int	Ground pins for internal logic
Vref	Reference voltage
$\overline{MR}$	Master reset
$\overline{PR}$	Partial reset
A_0–A_{79}	Input data bus
B_0–B_{79}	Output data bus
ENA	Port A enable pin
ENB	Port B enable pin
MBA	Port A Mailbox select
MBB	Port B Mailbox select
$\overline{CSA}$	Port A chip select
$\overline{CSB}$	Port B chip select
$\overline{OE}$	Output enable
CLKA	Port A clock
CLKB	Port B clock
BE_$\overline{FWFT}$	Big/Little Endian and CY Standard/First-Word Fall-Through mode select pin
SIZE1A, SIZE2A	Port A bus size configuration pins
SIZE1B, SIZE2B	Port B bus size configuration pins
RT_$\overline{SPM}$	Retransmit pin/serial programming select
TDI, TDO, TCK, TMS, TRST	JTAG pins
FS1_$\overline{SEN}$, FS0_SD	Programmable flags configuration pins
$\overline{EF}$_OR	Empty/output ready flag (Port B)
$\overline{FF}$_IR	Full/input ready flag (Port A)
$\overline{AE}$	Programmable almost empty flag (Port B)
$\overline{AF}$	Programmable almost full flag (Port A)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied .....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .....–0.5V to V_{CC}+0.5V

DC Input Voltage.....–0.5V to V_{CC}+0.5V

Output Current into Outputs (LOW) .....20 mA

Static Discharge Voltage .....>2001V (per MIL-STD-883, Method 3015)

Latch-Up Current.....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	2.5V ± 125 mV
Industrial	–40°C to +85°C	2.5V ± 125 mV

DC Specifications (All I/Os will be at HSTL level)

Parameter	Description	Test Conditions	CY7C480XV25		Unit
			Min.	Max.	
V_{CC_INT}	Power Supply Voltage		2.4	2.6	V
V_{CC_IO}	I/O Supply Voltage		1.4	1.9	V
V_{REF}	Input Reference Voltage	Typical value = 0.75V	0.7	1.0	V
V_{OH}	Output HIGH Voltage	$I_{OH} \geq$ 16 mA	1	1.9	V
V_{OL}	Output LOW Voltage	$I_{OL} \geq$ 1–16 mA	V_{SS}	0.7	V
V_{IH}	Input HIGH Voltage		0.7	1.6	V
V_{IL}	Input LOW Voltage		– 0.3	0.9	V
I_{IX}	Input Leakage Current		–10	+10	µA
I_{OZL},I_{OZH}	Output OFF, High Z Current		–10	+10	µA
I_{CC}	Active Power Supply Current	V_{CC_INT} = Max. I_{OUT} = 0 mA		100	mA
I_{SB}	Average Standby Current			10	mA

AC Specifications (A 50Ω load terminated into 0.75V is used with V_{CC} of 2.5V ± 125 mV)

Parameter	Description	CY7C4D80XV25		Unit
		Min.	Max.	
F_{MAX}	Max. Frequency		200	MHz
t_{CYC}	Clock Cycle Time	5		ns
t_{SD}	Input Data Set-Up Time	0.6		ns
t_{HD}	Input Data Hold Time	0.6		ns
t_A	Access Time	3.5		ns

Timing Parameters

Parameter	7C480XV25–200		7C480XV25–166		Unit
	Min.	Max.	Min.	Max.	
f_S		200		166	MHz
t_{CLK}	5		6		ns
t_{CLKH}	2.5		3		ns
t_{CLKL}	2.5		3		ns
t_{DS}	0.6		0.6		ns
t_{ENS}	1.5		2		ns
t_{RSTS}	2		2		ns
t_{FSS}	2		5		ns
t_{BES}	2		5		ns
t_{SMPS}	2		5		ns
t_{SDS}	1.5		2		ns
t_{SENS}	1.5		2		ns
t_{FWS}	0		0		ns
t_{DH}	0.6		0.6		ns
t_{ENH}	0		0		ns
t_{RSTH}	0		0		ns
t_{FSH}	0		0		ns
t_{BEH}	0		0		ns
t_{SPMH}	0		0		ns
t_{SDH}	0		0		ns
t_{SENH}	0		0		ns
t_{SPH}	0		0		ns
t_{SKEW1}	2.5		5		ns
t_{SKEW2}	2.5		5		ns
t_A		3.5		4	ns
t_{WFF}		3		4	ns
t_{REF}		3		4	ns
t_{PAE}		3		4	ns
t_{PAF}		3		4	ns
t_{PMF}		3		4	ns
t_{PMR}		3.5		4	ns
t_{MDV}		3.5		4	ns
t_{RSF}		4		4	ns
t_{EN}		1.5		4	ns
t_{DIS}		1.5		4	ns
t_{PRT}	25		25		ns
t_{RTR}	45		45		ns