HD74HC651/HD74HC652

Octal Bus Transceivers/Registers (with inverted 3-state outputs)
Octal Bus Transceivers/Registers (with 3-state outputs)

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Description

This device consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{\text{GBA}}$ are provided to cotrol the transceiver functions. Select AB and Select BA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the HD74HC651 and HD74HC652.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to high transition at the appropriate clock pins (Clock AB or Clock BA) regardless of the select or enable control pins. When Select AB and Select BA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling Enable GAB and $\overline{\text{GBA}}$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.
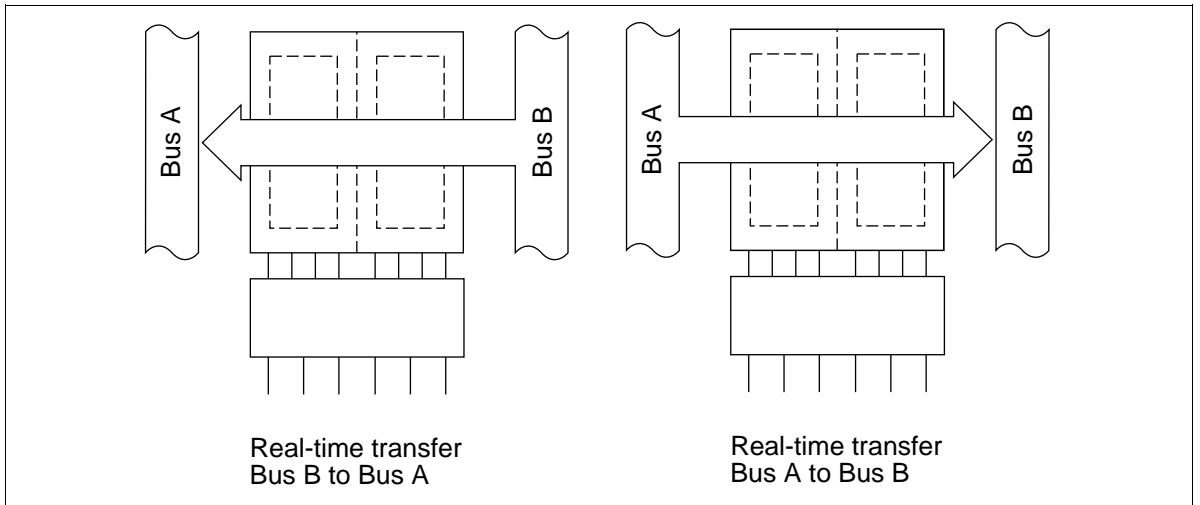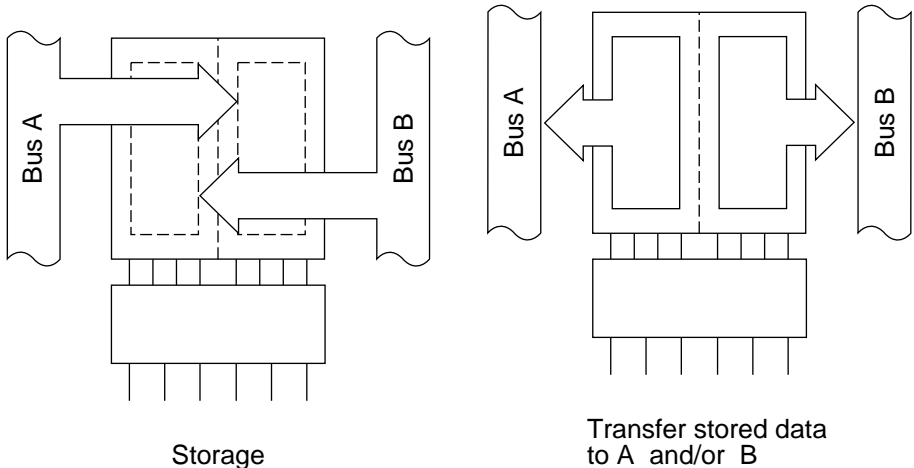
Features

- High Speed Operation: t_{pd} (Bus to Bus) = 16 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)

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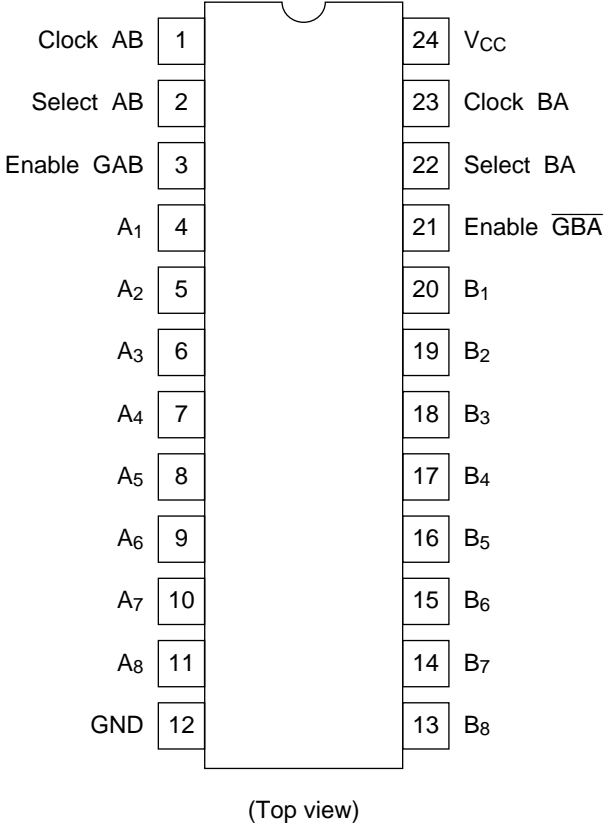
Function Table

	Real-Time Transfer Bus B to Bus A	Real-Time Transfer Bus A to Bus B	Storage	Transfer Stored Data to A and/or B
Clock AB	X	X		L or H
Select AB	X	L	X	H
Enable GAB	L	H	L	H
Clock BA	X	X		L or H
Select BA	L	X	X	H
Enable GBA	L	H	H	L

Real-time transfer
Bus B to Bus A

Real-time transfer
Bus A to Bus B

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Storage

Transfer stored data
to A and/or B

Pin Arrangement

Clock AB	1	24	V_{CC}
Select AB	2	23	Clock BA
Enable GAB	3	22	Select BA
A_1	4	21	Enable $\overline{GBA}$
A_2	5	20	B_1
A_3	6	19	B_2
A_4	7	18	B_3
A_5	8	17	B_4
A_6	9	16	B_5
A_7	10	15	B_6
A_8	11	14	B_7
GND	12	13	B_8

(Top view)

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Absolute Maximum Ratings

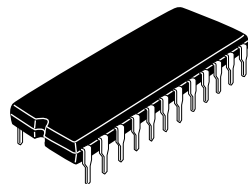| Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Output current	I_{OUT}	±35	mA
DC current drain per V_{CC} , GND	I_{CC}, I_{GND}	±75	mA
DC input diode current	I_{IK}	±20	mA
DC output diode current	I_{OK}	±20	mA
Power Dissipation per package	P_T	500	mW
Storage temperature	Tstg	−65 to +150	°C

Logic Diagram

HD74HC651
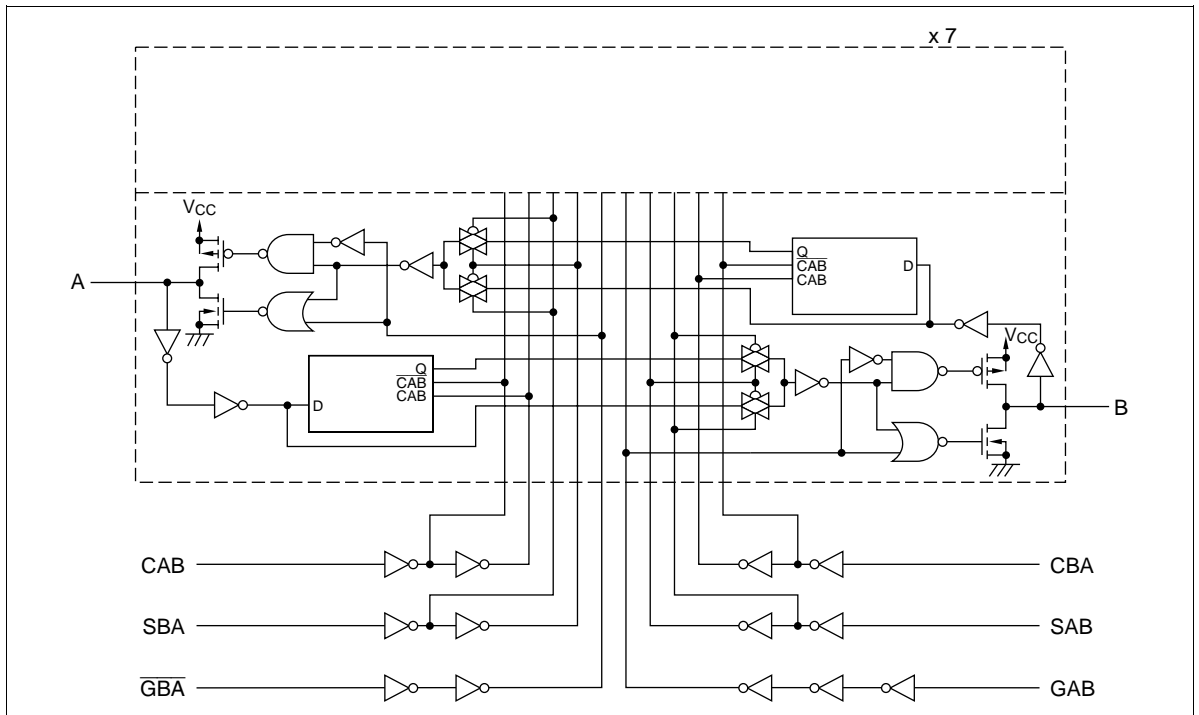
HD74HC652
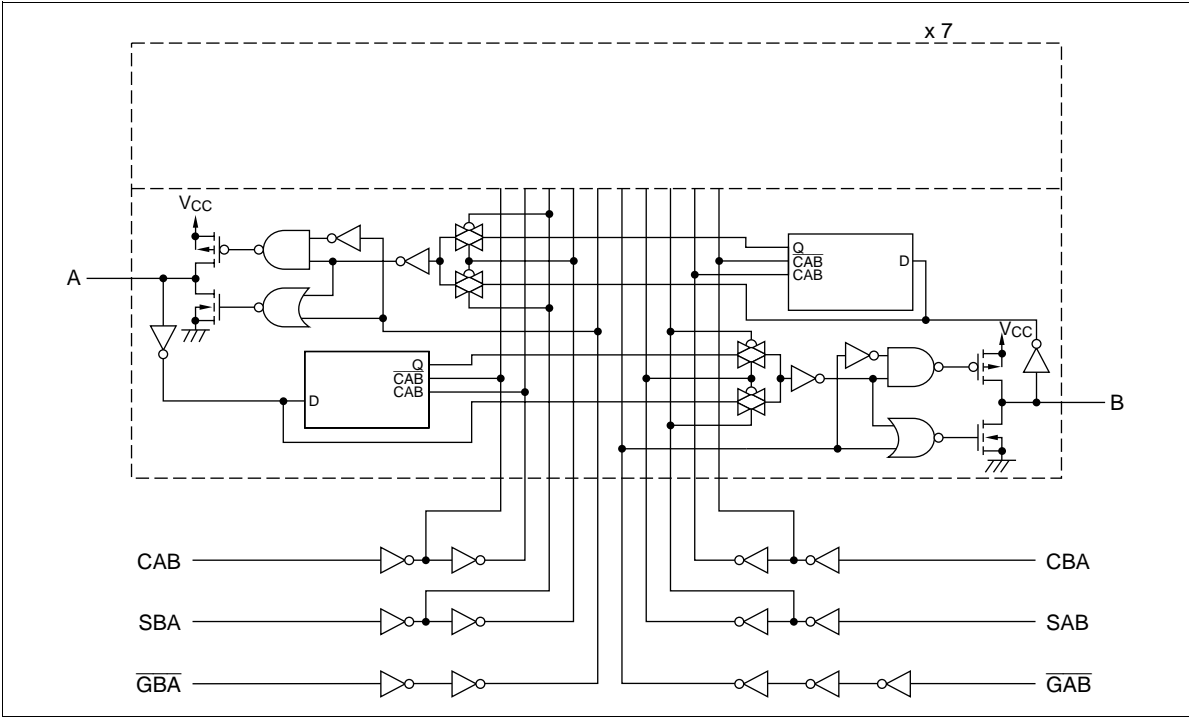
DC Characteristics

Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = −40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V_{IL}	2.0	—	—	0.5	—	0.5	V	
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL} I_{OH} = −20 μA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		I_{OH} = −6 mA
		6.0	5.68	—	—	5.63	—		I_{OH} = −7.8 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL} I_{OL} = 20 μA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		I_{OL} = 6 mA
		6.0	—	—	0.26	—	0.33		I_{OL} = 7.8 mA
Off-state output current	I_{OZ}	6.0	—	—	±0.5	—	±5.0	μA	Vin = V_{IH} or V_{IL}, Vout = V_{CC} or GND
Input current	Iin	6.0	—	—	±0.1	—	±1.0	μA	Vin = V_{CC} or GND
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	μA	Vin = V_{CC} or GND, Iout = 0 μA

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AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V_{cc} (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Propagation delay	t_{PLH}	2.0	—	—	170	—	215	ns	Clock to Bus
time	t_{PHL}	4.5	—	19	34	—	43		
		6.0	—	—	29	—	37		
		2.0	—	—	135	—	170	ns	Bus to Bus
		4.5	—	16	27	—	34		
		6.0	—	—	23	—	29		
		2.0	—	—	190	—	240	ns	Select to Bus
		4.5	—	18	38	—	48		
		6.0	—	—	32	—	41		
Output enable	t_{ZL}	2.0	—	—	150	—	190	ns	
time	t_{ZH}	4.5	—	14	30	—	38		
		6.0	—	—	26	—	33		
Output disable	t_{LZ}	2.0	—	—	150	—	190	ns	
time	t_{HZ}	4.5	—	18	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	7	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	
		4.5	20	4	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	
		4.5	5	–1	—	5	—		
		6.0	5	—	—	5	—		
Output rise/fall	t_{TLH}	2.0	—	—	60	—	75	ns	
time	t_{THL}	4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
Input capacitance	Cin	—	—	5	10	—	10	pF	

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Unit: mm
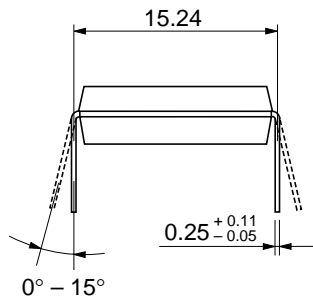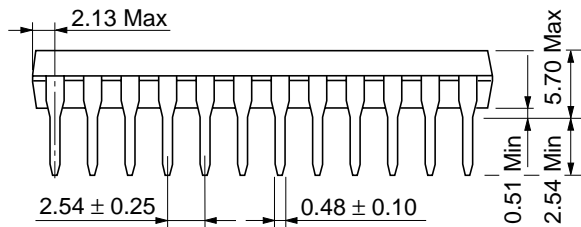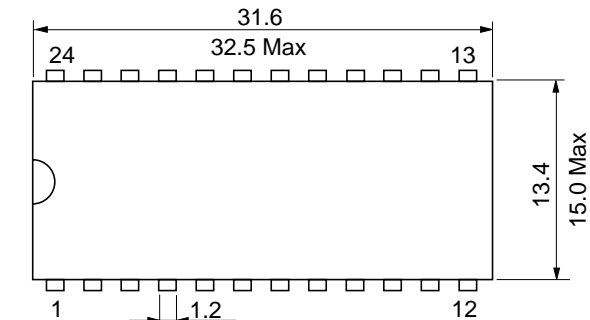
Hitachi Code	DP-24
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	3.1 g

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