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NIPPON PRECISION CIRCUITS INC.

OVERVIEW

The SM6453AB is a 3-wire serial data volume control for headphone amplifiers with built-in electronic volume control. Two switchable input systems are supported. It features bass boost function, auto gain control function (AGC), power-down function, and beep input, making it ideal for use in portable electronic products.

FEATURES

- 2 stereo system inputs, 1 output system
- 12mW + 12mW output (standard, 16Ω load, 2.0V supply voltage)
- Attenuation function
  - 1.0dB step width
  - 80-step
  - + 12 to – 68dB variable range
- Mute function
- Low current consumption (2.3mA total, 2.4V supply voltage)
- 12dB voltage gain
- Bass boost function (2 boost characteristics controlled by external RC network)
- Auto gain control function (AGC)
- Beep sound input/output circuit
- Power-down function
- 1.9 to 3.6V operating supply voltage range
- Silicon-gate CMOS process

ORDERING INFORMATION

Device	Package
SM6453AB	32-pin QFN

PINOUT

(Top view)

Top row pins (left to right): 32 DVDD1, 31 DVDD2, 30 DVSS, 29 LRMX0, 28 AGCTC, 27 BSTC, 26 BSTN

Left side pins (top to bottom):
- MLEN 1
- MCK 2
- MDT 3
- RSTN 4
- MUTEN 5
- PDN 6
- BEEPI 7
- VREF1 8
- VREF2 9

Right side pins (top to bottom):
- 25 BSTO
- 24 BEEPLO
- 23 LOUT
- 22 AVSS2
- 21 AVDD2
- 20 AVDD3
- 19 AVSS3
- 18 ROUT
- 17 BEEPRO

Bottom row pins (left to right): 10 AVDD1, 11 LIN1, 12 LIN2, 13 AVSS1, 14 RIN1, 15 RIN2, 16 VBIAS
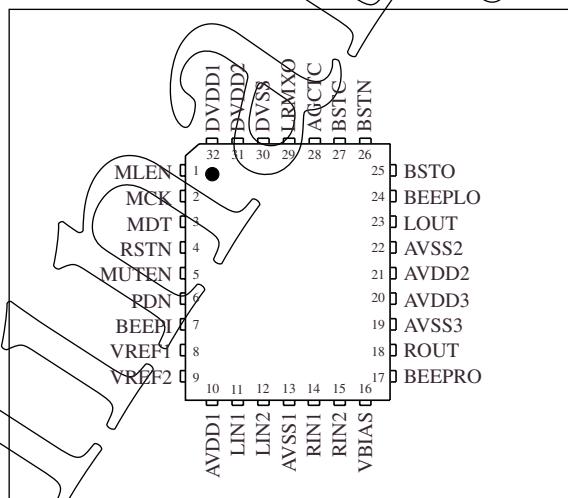
PACKAGE DIMENSIONS

(Unit: mm)

32-pin QFN

TBD

PIN DESCRIPTION

| Number	Name	I/O[1]	Description	V_{DD}
1	MLEN	Ip	Microcontroller latch enable input	V_{DD2}
2	MCK	Ip	Microcontroller clock input	
3	MDT	Ip	Microcontroller data input	
4	RSTN	Ip	System reset (LOW-level reset)	
5	MUTEN	I	Mute input (LOW-level mute)	
6	PDN	I	Power-down mode select (LOW-level power-down)	
7	BEEPI	I	Beep signal input	
8	VREF1	O	Reference voltage 1	V_{DD1}
9	VREF2	O	Reference voltage 2	
10	AVDD1	–	EVR-stage analog V_{DD}	
11	LIN1	I	Left-channel analog input 1	
12	LIN2	I	Left-channel analog input 2	
13	AVSS1	–	EVR-stage analog V_{SS}	
14	RIN1	I	Right-channel analog input 1	
15	RIN2	I	Right-channel analog input 2	
16	VBIAS	O	EVR-stage bias voltage	
17	BEEPRO	O	Right-channel beep signal output	
18	ROUT	O	Right-channel output	
19	AVSS3	–	Headphone amplifier right-channel analog V_{SS}	
20	AVDD3	–	Headphone amplifier right-channel analog V_{DD}	
21	AVDD2	–	Headphone amplifier left-channel analog V_{DD}	
22	AVSS2	–	Headphone amplifier left-channel analog V_{SS}	
23	LOUT	O	Left-channel output	
24	BEEPLO	O	Left-channel beep signal output	
25	BSTO	O	Bass boost auxiliary output	
26	BSTN	I	Bass boost auxiliary input	
27	BSTC	O	Bass boost capacitor connection	
28	AGCTC	O	AGC time constant capacitor connection	
29	LRMXO	O	Left + right-channel mix detector output	
30	DVSS	–	Digital V_{SS}	
31	DVDD2	–	Digital V_{DD2}	
32	DVDD1	–	Digital V_{DD1}	V_{DD2}

1. Ip = input with pull-up

V_{DD1}, V_{DD2}, V_{SS} definition:
V_{DD1} = DVDD2 = AVDD1 = AVDD2 = AVDD3
V_{DD2} = DVDD1
V_{SS} = DVSS = AVSS1 = AVSS2 = AVSS3

BLOCK DIAGRAM
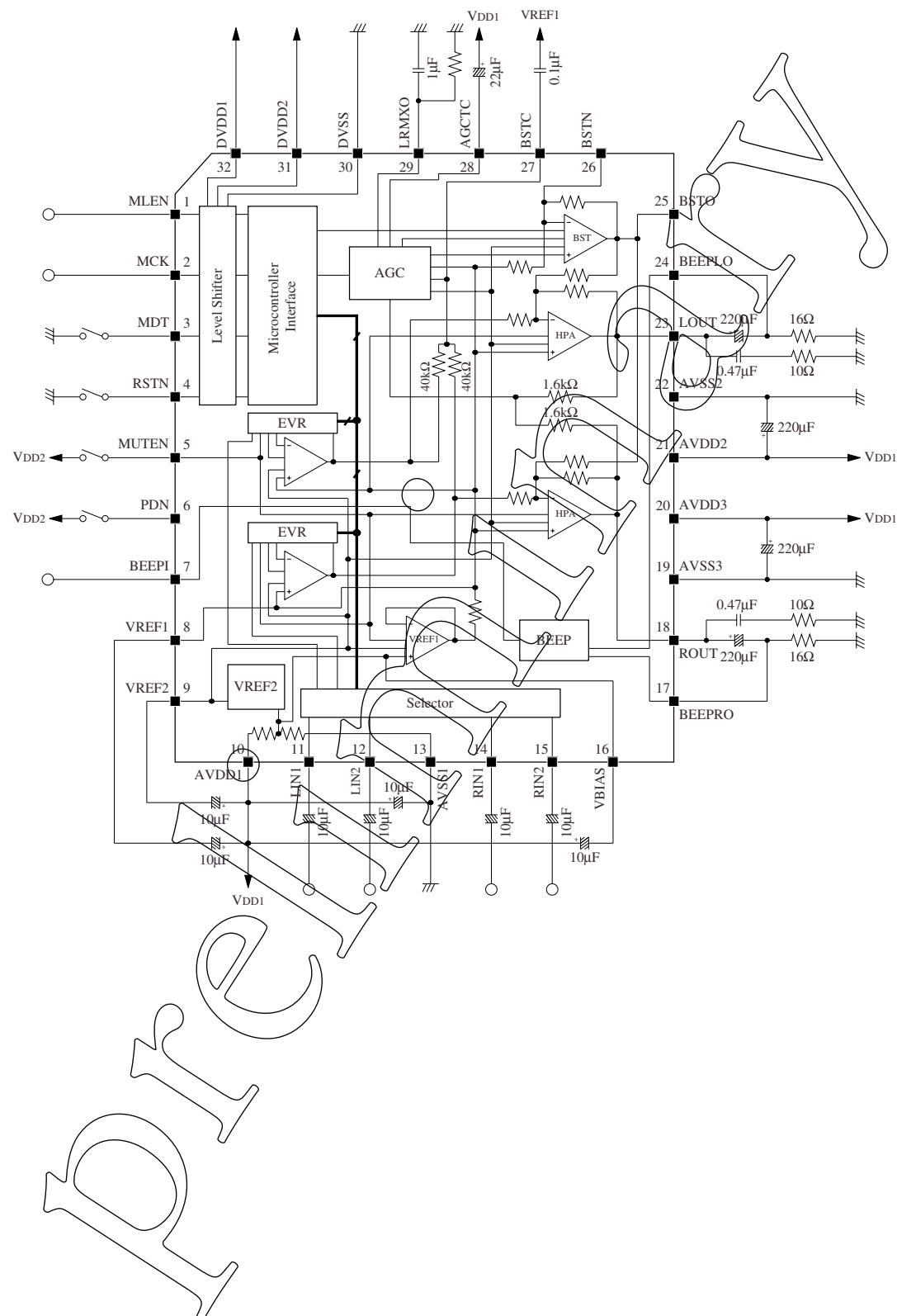
SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD1}, V_{DD2}	− 0.3 to 4.6	V
	V_{SS}	0	V
Digital system input voltage	V_{IND}	DVSS − 0.3 to V_{DD1} + 0.3	V
Analog system input voltage	V_{INA}	AVSS − 0.3 to V_{DD2} + 0.3	V
Storage temperature	T_{STG}	− 55 to 125	°C

Recommended Operating Conditions

$V_{SS} = DVSS = AVSS1 = AVSS2 = AVSS3 = 0V$, $V_{DD1} = DVDD2 = AVDD1 = AVDD2 = AVDD3$,
$V_{DD2} = DVDD1$

Parameter	Symbol	Conditions	Unit
Supply voltage 1	V_{DD1}	1.9 to 3.6	V
Supply voltage 2	V_{DD2}	1.9 to 3.6	V
Operating temperature	T_{OPR}	− 40 to 85	°C

Voltages between DVDD2, AVDD1, AVDD2, AVDD3 should be less ± 0.1V.

DC Characteristics

AVSS1 = AVSS2 = AVSS3 = DVSS = 0V, AVDD1 = AVDD2 = AVDD3 = DVDD2 = 1.9 to 3.6V,
DVDD1 = 1.9 to 3.6V

Parameter	Pins	Symbol		Condition	Rating			Unit
					min	typ	max	
Current consumption	DVDD1	I_{DDD1A}		(Note 1)		0.01	0.02	mA
		I_{DDD1S}		(Note 2)		0.2	1.0	µA
	DVDD2	I_{DDD2A}		(Note 1)		0.30	TBD	mA
		I_{DDD2S}		(Note 2)		0.2	1.0	µA
	AVDD1	I_{DDA1A}		(Note 1)		0.84	1.26	mA
		I_{DDA1S}		(Note 2)		TBD	25.0	µA
	AVDD2	I_{DDA2A}		(Note 1)		0.68	1.02	mA
		I_{DDA2S}		(Note 2)		TBD	25.0	µA
		I_{DDA2T}		(Note 3)	TBD			
	AVDD3	I_{DDA3A}		(Note 1)		0.68	1.02	mA
		I_{DDA3S}		(Note 2)		TBD	25.0	µA
		I_{DDA3T}		(Note 3)	TBD			
Input voltage 1	(*1)	H-level	V_{IH1}		0.7×DVDD1			V
		L-level	V_{IL1}				0.3×DVDD1	V
Input voltage 2	(*2)	H-level	V_{IH2}		1.0			V
		L-level	V_{IL2}				0.4	V
Input voltage 3	(*3)	H-level	V_{IH3}		1.5			V
		L-level	V_{IL3}				1.0	V
Input current 1	(*1)		I_{IL1}	$V_{IN} = 0V$		70	150	µA
Input current 2	(*3)		I_{IH1}	$V_{IN} = V_{DD1}$		280	420	µA
Input leakage current 1	(*1)		I_{IH2}	$V_{IN} = V_{DD1}$			1.0	µA
Input leakage current 2	(*2)		I_{IL2}	$V_{IN} = 0V$			1.0	µA
Input leakage current 3	(*2)		I_{IH3}	$V_{IN} = V_{DD1}$			1.0	µA
Input leakage current 4	(*3)		I_{IL3}	$V_{IN} = 0V$			1.0	µA

(Note 1) MUTEN = H-level, PDN = H-level, Analog input = – ∞ dBv, ATT = 0dB, Microcontroller clock frequency = 4MHz, data transfer from microcontroller
(Note 2) MUTEN = L-level, PDN = L-level, Analog input = – ∞ dBv, ATT = 0dB, data transfer from microcontroller stopped, Pins (*1) = V_{DD2}
(Note 3) MUTEN = H-level, PDN = H-level, reference voltage = Measurement circuit, Bass boost = OFF, AGC = OFF, Frequency = 1kHz, P_O = 0.5mW + 0.5mW

Pin types

(*1)	Function	Digital signal inputs (with pull-up)
	Name	MLEN, MDT, MCK, RSTN
(*2)	Function	Analog input 1
	Name	MUTEN, PDN
(*3)	Function	Analog input 2
	Name	BEEP

AC Characteristics

AVDD1 = AVDD2 = AVDD3 = DVDD1 = DVDD2 = 1.9 to 3.6V, V_{SS} = 0V, Ta = $-$ 40 to 85°C, unless otherwise noted.

Serial inputs (MDT, MCK, MLEN)

Parameter		Symbol	Rating			Unit
			min	typ	max	
MCK, MLEN rise time		t_r			100	ns
MCK, MLEN fall time		t_f			100	ns
MDT setup time		t_{MDS}	50			ns
MDT hold time		t_{MDH}	50			ns
MLEN	Setup time	t_{MCS}	50			ns
	Hold time	t_{MCH}	50			ns
	LOW-level pulsewidth	t_{MEWL}	50			ns
	HIGH-level pulsewidth	t_{MEWH}	50			ns
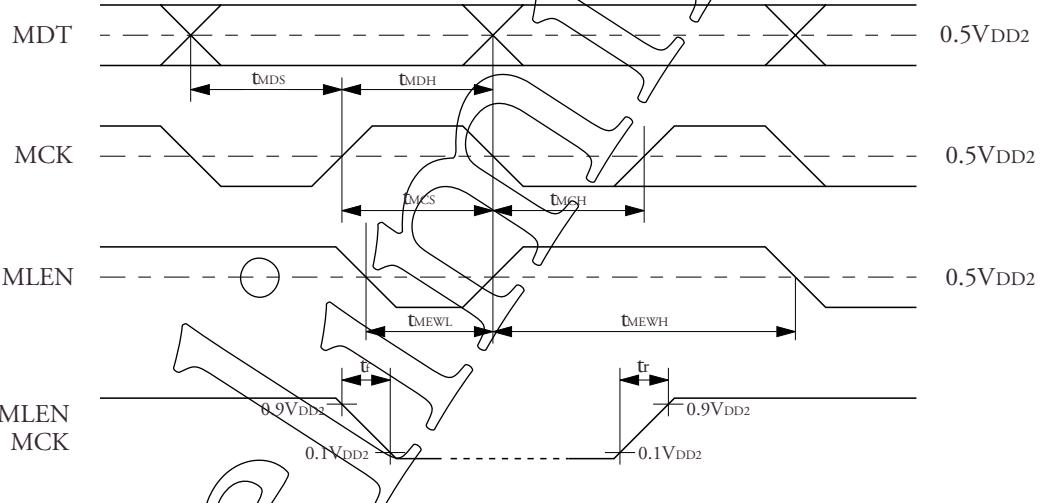
Reset input (RSTN)

Parameter	Symbol	Rating			Unit
		min	typ	max	
RSTN LOW-level pulsewidth	t_{RSTN}	100			ns

AC Analog Characteristics

$V_{DD1} = V_{DD2} = 2.0V$, analog input amplitude = 0.022Vrms, input frequency = 1kHz, Ta = 25°C, Measurement circuit, unless otherwise noted.

Analog input characteristics (LIN1, RIN1, LIN2, RIN2)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Reference input amplitude	V_{AI}	ATT = 0dB		0.022		Vrms
Input resistance	R_{IN}		45	51	57	kΩ
Input clipping voltage	V_{CLP}	ATT = 0dB	0.14	0.168		Vrms

Analog output characteristics (LOUT, ROUT)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Residual noise voltage	V_{NS}	ATT = 0dB		20	30	μVrms
Total harmonic distortion + noise	THD + N	P_O = 0.5mW + 0.5mW		0.3	0.8	%
Maximum output voltage	P_{OMAX}	ATT = 0dB, THD = 10%	15	20		mW
Bass boost response[1]	B_{BST}			+ 13.5		dB
AGC detection level	V_{AGC}			0.55+ 0.5V_{DD1}		V
Gain control range	R_{CNT}		− 68		12	dB
Step size	STEP		0.8	1.0	1.8	dB
Attenuation error (1kHz to 20kHz)	ERR1	@ 12dB to − 48dB	TBD	0.2	TBD	dB
	ERR2	@ − 49dB to − 68dB	TBD	0.5	TBD	dB
Absolute attenuation (1kHz)	AT_0	ATT = 0dB		+ 12.0		dB
	AT_2	ATT = − 20dB		− 8.0		dB
	AT_4	ATT = − 40dB		− 28.0		dB
	AT_6	ATT = − 60dB		− 48.1		dB
	AT_8	ATT = − 80dB		− 68.2		dB
Mute factor (1kHz)	MUTE	ATT = MUTE, MUTEN = LOW	− 84.0	− 90.0		dB
Channel crosstalk[2]	CT_1		− 84.0	− 90.0		dB
Channel crosstalk[3]	CT_2		− 24.0	− 40.0		dB
Ripple rejection	PSRR	Supply ripple on AVDD1, AVDD2, AVDD3	69.0	75.0		dB

1. Bass boost control bit D9 = HIGH, 55Hz, V_O = − 30dBv
2. ATT = 0dB, leakage output on one channel with analog input on the other channel only.
3. Bass boost control bit D9 = HIGH, ATT = 0dB, leakage output on one channel with analog input on the other channel only.

Analog output characteristics (BEEPLO, BEEPRO)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
BEEP output current	I_{BO}	400Hz rectangular wave, input level = 1.5V to V_{DD2}	0.3	0.36	0.4	mA
BEEP output voltage	V_{BO}		− 56	− 51.3	− 46	dBv

Reference voltage characteristics (VREF1, VREF2, VBIAS)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Reference voltage output 1	V_{REF1}		$0.45V_{DD1}$	$0.5V_{DD1}$	$0.55V_{DD1}$	V
Reference voltage output 2	V_{REF2}			$V_{DD1} - 0.815$		V
Bias voltage output	V_{BIAS}		$0.45V_{DD1}$	$0.5V_{DD1}$	$0.55V_{DD1}$	V

Measurement circuit
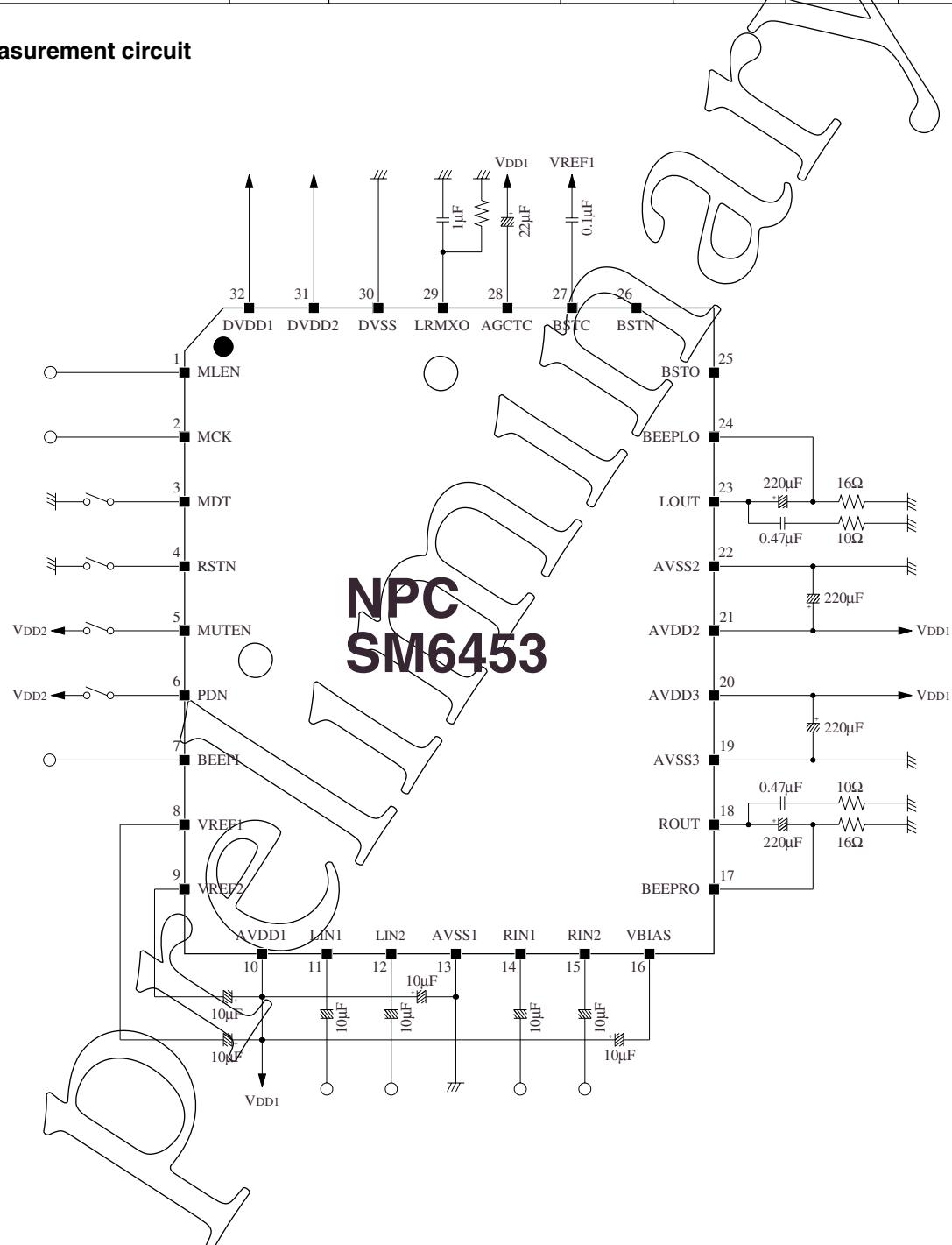
FUNCTIONAL DESCRIPTION

Microcontroller Interface

The SM6453AB uses a serial microcontroller interface comprising MDT (data), MCK (clock), MLEN (latch enable).

Data format

The data transfer format is shown in figure 1.
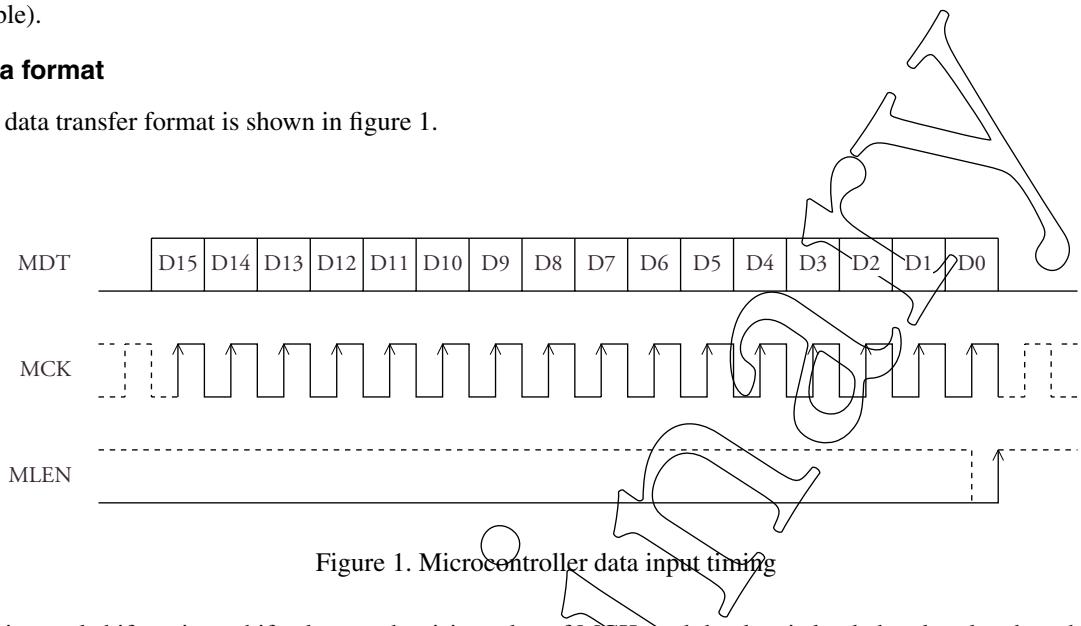
Figure 1. Microcontroller data input timing

The internal shift register shifts data on the rising edge of MCK, and the data is loaded and updated on the rising edge of MLEN (the dotted lines are all valid data timing). Each cycle is completed by 16 or more MCK input cycles, even if there are unused data bits.
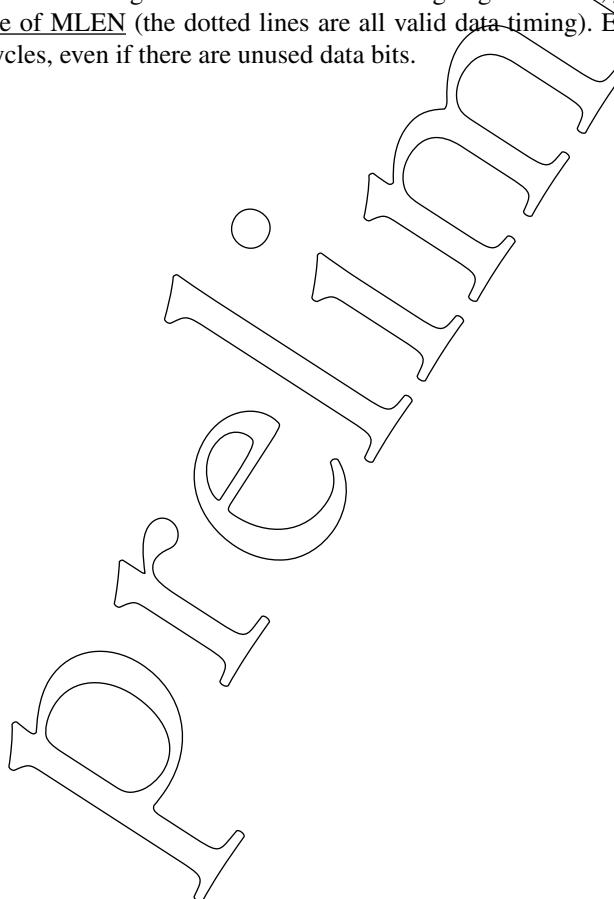
Microcontroller data description

"L" = V_{IL1} level, "H" = V_{IH1} level

■ D15 to D12: Not used (Don't Care) bits. Can be either "L" or "H".

■ D11: AGC bit. OFF when "L", and ON when "H".

D11	AGC function
L	OFF
H	ON

■ D10, D9: Bass boost control bit.

D9	D10	Bass boost characteristics
L	L	OFF
	H	
H	L	BB1
	H	BB2

■ D8: Input select bit. LIN1 and RIN1 when "L", and LIN2 and RIN2 when "H".

D8	Selected inputs
L	LIN1, RIN1
H	LIN2, RIN2

■ D7 to D0: Attenuation (ATT) bits.

| Amp gain	EVR ATT value	D7	D6	D5	D4	D3	D2	D1	D0	HEX
+ 12dB	0dB	L	L	L	L	L	L	L	L	00
+ 11dB	− 1dB	L	L	L	L	L	L	L	H	01
+ 10dB	− 2dB	L	L	L	L	L	L	H	L	02
:	:	:	:	:	:	:	:	:	:	:
− 3dB	− 15dB	L	L	L	L	H	H	H	H	0F
− 4dB	− 16dB	L	L	L	H	L	L	L	L	10
− 5dB	− 17dB	L	L	L	H	L	L	L	H	11
:	:	:	:	:	:	:	:	:	:	:
− 52dB	− 63dB	L	L	H	H	H	H	H	H	3F
− 53dB	− 64dB	L	H	L	L	L	L	L	L	40
− 54dB	− 65dB	L	H	L	L	L	L	L	H	41
:	:	:	:	:	:	:	:	:	:	:
− 67dB	− 79dB	L	H	L	L	H	H	H	H	4F
− 68dB	− 80dB	L	H	L	H	L	L	L	L	50
MUTE	MUTE	L	H	L	H	L	L	L	H	51
MUTE	MUTE	L	H	L	H	L	L	H	L	52
MUTE	MUTE	:	:	:	:	:	:	:	:	:
MUTE	MUTE	H	H	H	H	H	H	H	L	FE
MUTE	MUTE	H	H	H	H	H	H	H	H	FF

Note: At system reset, AGC = OFF, bass boost = OFF, LIN1 and RIN1 input, MUTE are selected.
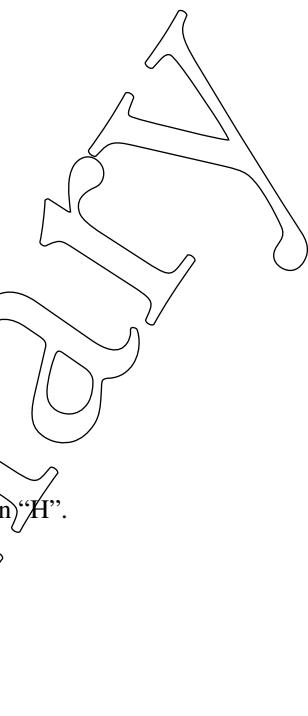
Bass Boost Function (BSTO, BSTN, BSTC)

Using the bass boost function, the left-channel and right-channel bass components are sampled and amplified, or boosted, and added to the headphone driver amplifier. The connection of 0.1μF (std) capacitor to BSTC forms a lowpass filter. The bass boost response can also be selected using bit D12.
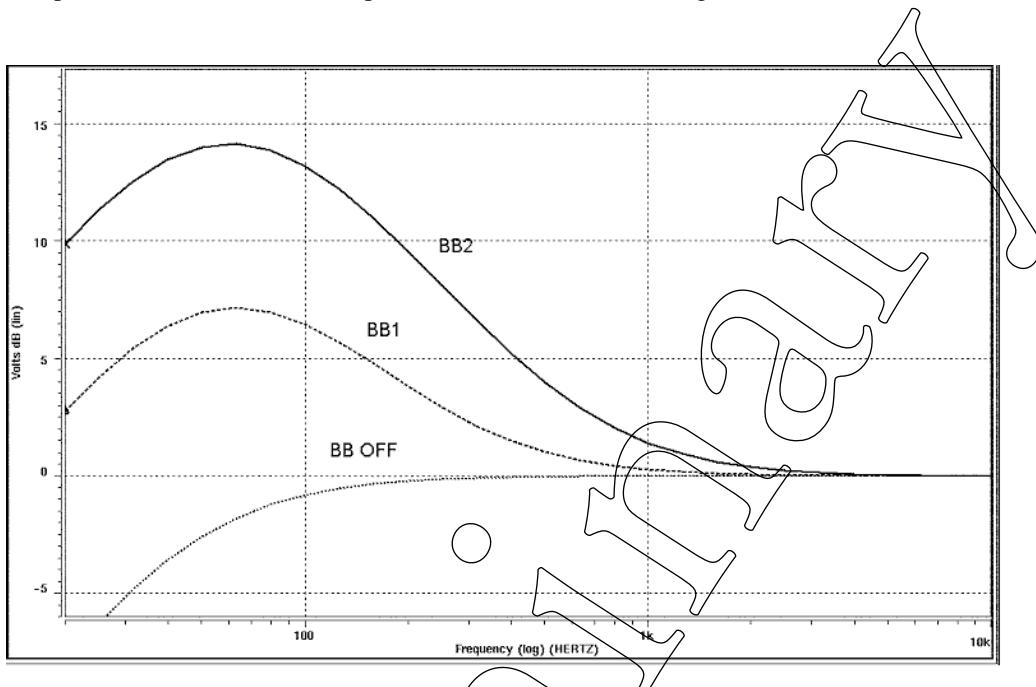
Usually there is no component connected to BSTO and BSTN, however, the boost response characteristic can be modified by connecting a resistor and capacitor between BSTO and BSTN.
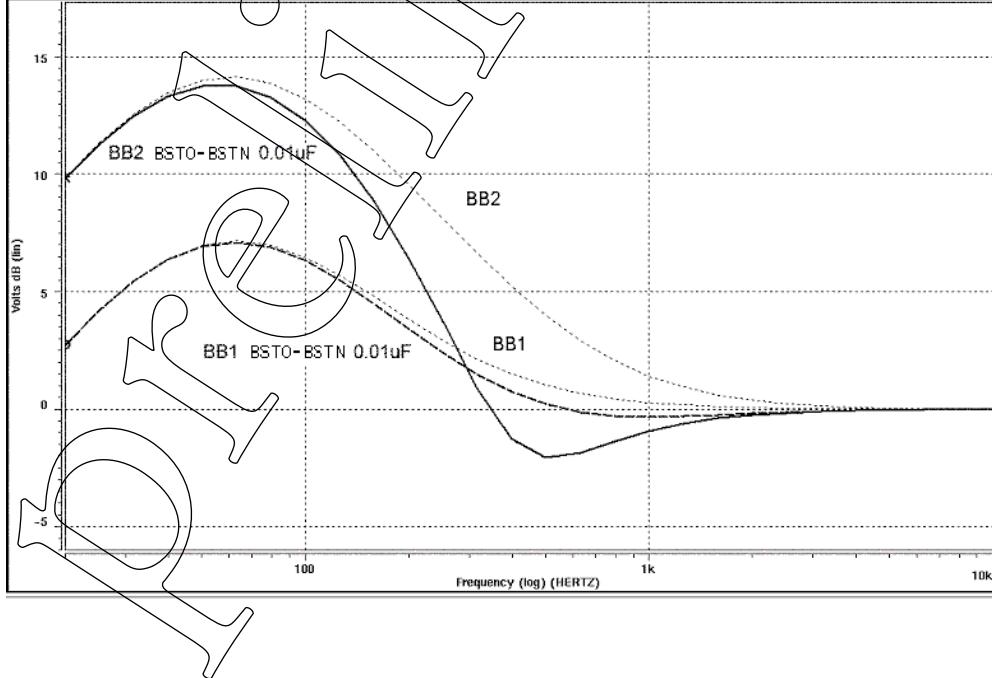
Auto-gain Control

The output level from the bass boost circuit can be controlled to prevent the output from exceeding a value VREF1 [V] + 0.55 [Vpeak].

The output clip level margin is increased when bass boost is ON.

Mute Function (MUTEN)

Mute is ON when MUTEN = "L". The mute setting is also controlled by microcontroller data. A pull-down resistor can be added to prevent malfunction.

Power-down Function (PDN)

Power-down function is ON when PDN="L". A pull-down resistor can be added to prevent malfunction.

Beep Signal Input/Output (BEEPI, BEEPLO, BEEPRO)

The beep output circuit operates when MUTEN = "L". The beep output is a fixed-current output on BEEPLO and BEEPRO.