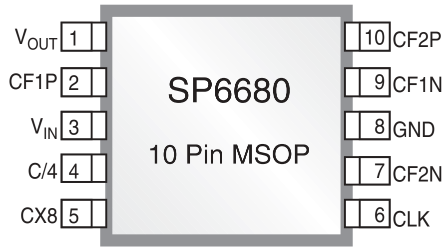
High Efficiency Buck/Boost Charge Pump Regulator

- Ideal For Sim Card Applications In Cellular Phones
- Low Profile, Inductorless Regulator
- Up To 96% Power Efficiency
- +2.7V to +6.3V Input Voltage Range
- 5.8V Output Voltage
- 60mA Output Current
- 75µA Quiescent Current
- 4µA Shutdown Current
- External 32.768kHz Clock Input
- Three Programmable Charge Pump Frequencies: 8.192kHz, 32.768kHz, and 262.14kHz
- Internal Oscillator At 16.7kHz, When CLK Pin Is Held High
- Space Saving 10-Pin µSOIC Package

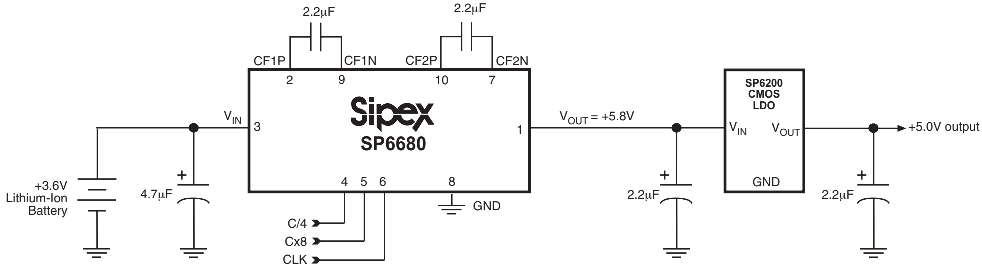


Now Available in Lead Free Packaging

DESCRIPTION

The SP6680 is a charge pump ideal for converting a +3.6V Li-Ion battery input to a +5.0V regulated output. An input voltage range of +2.7V to +6.3V is converted to a regulated output of 5.8V. The SP6680 device will operate at three different switching frequencies corresponding to three different output resistances and load current ranges. An external 32.768kHz nominal clock signal is used to produce three synchronized pump frequencies through the use an internal phase look loop of an to drive the charge pump. Two control inputs can adjust the internal pump frequency on the fly to 8.192kHz (f_{INPUT}/ 4), 32.768kHz (f_{INPUT} x 1), or 262.14kHz (f_{INPUT} x 8). The charge pump configuration dynamically changes to optimize power efficiency. At low input voltages the charge pump doubles the input while at higher inputs the output is 1.5 times the input. The SP6680 can deliver high power efficiencies up to 96% with low quiescent currents from 75µA to 800µA. The SP6680 is offered in a 10-Pin µSOIC package.

TYPICAL APPLICATION CIRCUIT



*All Capacitors Are Ceramic

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{IN}..-0.3V to +7.0V
V_{OUT}...-0.3V to +7.0V
I_{OUT}..100mA
Storage Temperature........................-65˚C to +150˚C

Power Dissipation Per Package
10-pin mSOIC
(derate 8.84mW/^{O}C above +70^{O}C)..................720mW
Junction Temperature.......................................125˚C

ELECTRICAL CHARA CTERISTICS

V_{IN} = +2.7 to +6.3V, f_{CLK} = 32.768kHz, C_{IN} = 4.7µF (ceramic), CF1 = CF2 = C_{OUT} = 2.2µF, (ESR = 0.03 Ω) and T_{AMB} = -40°C to +85°C unless otherwise noted.

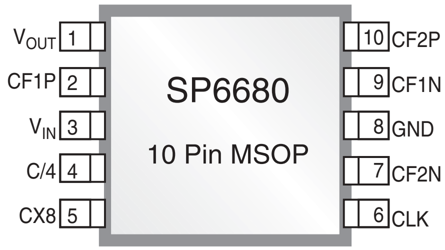
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Supply Voltage, V_{IN}	2.75	3.6	6.3	V	
Quiescent Current, I_Q		75 170 800	150 300 1500	µA	$f_{PUMP} = f_{CLK}/4$ $f_{CLK} = f_{PUMP}$ V_{IN} = 4.2V $f_{PUMP} = f_{CLK}$ x 8
In-Rush Current into V_{IN}, I_{INRUSH}		500		mA	2.7V<V_{IN}<6.3V, Note 1
Off Current, I_{OFF}		4.4	10	µA	V_{IN} = 4.2V, clock not present, -40˚ C to +70˚ C
Input Clock Frequency, f_{CLK}		32.768		kHz	Operational (supplied externally)
Pump Frequency, f_{PUMP} (Note 2)		 0 32.768 8.192 262.14 16.7		kHz	**f_{CLK}** / **C/4pin input** / **Cx8pin input** no input / X / X present / low / low present / high / low present / X / high high / low / low
Input Threshold Voltage V_{IL} V_{IH}	 1.3		 0.4	V	 Digital inputs = f_{CLK}, $f_{CLK}/4$, f_{CLK} x 8 Digital inputs = f_{CLK}, $f_{CLK}/4$, f_{CLK} x 8
Input Current $I_{IN(low)}$ $I_{IN(high)}$		 0.1 1.0	 10 10	µA	 Digital inputs = f_{CLK}, $f_{CLK}/4$, f_{CLK} x 8 Digital inputs = f_{CLK}, $f_{CLK}/4$, f_{CLK} x 8
Mode Transition Voltage, X1.5 to X2, V_{IN} falling	3.55 3.55	3.70 3.70	3.85 3.85	V	$f_{pump} = f_{CLK}/4$, I_{LOAD} = 1mA f_{pump}, $f_{CLK,}$ I_{LOAD} = 5mA
Hysteresis for Mode Transition Voltage		50		mVpp	V_{IN} rising to V_{IN} falling
Transient Response: Maximum Transient Amplitude		 1.5 1.5 1.5		%	**I_{LOAD}** / **Δt** / **f_{PUMP}** 100µA to 2mA / 5µs / 8.192kHz 2mA to 20mA / 5µs / 32.768kHz 20mA to 60mA / 5µs / 262.14kHz

V_{IN} = +2.7 to +6.3V, f_{CLK} = 32.768kHz, C_{IN} = 4.7µF (ceramic), CF1 = CF2 = C_{OUT} = 2.2µF, and T_{AMB} = -40°C to +85°C unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS			
Output Resistance, R_{OUT}					V_{IN}	I_{LOAD}	f_{PUMP}	mode
		60		Ω	3.85V	2mA	8.192kHz	X2
		20	30		3.85V	10mA	32.768kHz	X2
		12.5			3.85V	40mA	262.14kHz	X2
Average Output Voltage, V_{OUT}					V_{IN}	I_{LOAD}	f_{PUMP}	mode
	5.1	5.8	6.3	V	3.0V	2mA	8.192kHz	X2
	5.1	5.8	6.3		3.55V	2mA	8.192kHz	X2
	5.1	5.6	6.3		3.85V	2mA	8.192kHz	X1.5
	5.1	5.6	6.3		6.3V	2mA	8.192kHz	X1.5
	5.1	5.8	6.3		3.0V	10mA	32.768kHz	X2
	5.1	5.8	6.3		3.55V	10mA	32.768kHz	X2
	5.1	5.5	6.3		3.85V	10mA	32.768kHz	X1.5
	5.1	5.6	6.3		6.3V	10mA	32.768kHz	X1.5
	5.1	5.6	6.3		3.0V	40mA	262.14kHz	X2
	5.1	5.8	6.3		3.55V	40mA	262.14kHz	X2
	5.1	5.3	6.3		3.85V	40mA	262.14kHz	X1.5
	5.1	5.8	6.3		6.3V	40mA	262.14kHz	X1.5
Power Efficiency, P_{EFF}					V_{IN}	I_{LOAD}	f_{PUMP}	mode
		93		%	3.0V	2mA	8.192kHz	X2
		80			3.55V	2mA	8.192kHz	X2
		92			3.85V	2mA	8.192kHz	X1.5
		54			6.3V	2mA	8.192kHz	X1.5
		96			3.0V	10mA	32.768kHz	X2
		80			3.55V	10mA	32.768kHz	X2
		92			3.85V	10mA	32.768kHz	X1.5
		57			6.3V	10mA	32.768kHz	X1.5
		92			3.0V	40mA	262.14kHz	X2
		81			3.55V	40mA	262.14kHz	X2
		91			3.85V	40mA	262.14kHz	X1.5
		60			6.3V	40mA	262.14kHz	X1.5

Note 1: f_{CLK} applied 10ms after V_{IN} is present.

PINOUT



PIN ASSIGNMENTS

Pin 1— V_{OUT} — Regulated charge pump output from +5.2V to +6.3V. The output voltage is regulated to 5.8V nominal output.

Pin 2 — CF1P — Positive terminal to the charge pump flying capacitor, CF1.

Pin 3 — V_{IN} — Input pin for the +2.7V to +6.3V supply voltage.

Pin 4 — C/4 — This is a control line for the internal charge pump frequency. When this control line is forced to a logic high, the internal charge pump frequency is set to $^1/_4$ of the CLK frequency, provided that Cx8 is low.

Pin 5 — Cx8 — This is a control line for the internal charge pump frequency. When this control line is forced to a logic high, the internal charge pump frequency is set to x8 of the CLK frequency.

Pin 6 — CLK — 32.768kHz Clock. Connect this input pin to an external 32.768kHz clock to drive the frequency of the charge pump. Logic low inputs on the C/4 and Cx8 pins sets the internal charge pump frequency according to *Table 1*. Shutdown mode for the device is set when there is no clock signal present on this input pin, or when it is pulled to ground.

Pin 7 — CF2N — Negative terminal to the charge pump flying capacitor, CF2.

Pin 8 — GND — Ground reference.

Pin 9 — CF2P — Positive terminal to the charge pump flying capacitor, CF2.

Pin 10 — CF1N — Negative terminal to the charge pump flying capacitor, CF2.

DESCRIPTION

The SP6680 device is a regulated CMOS charge pump voltage converter that can be used to convert a +2.7V to +6.3V input voltage to a nominal +5.2V to +6.3V output. These devices are ideal for cellular phone designs involving battery-powered and/or board level voltage conversion applications.

An external clock signal with a frequency of 32.768kHz nominal is required for device operation. A designer can set the SP6680 device to operate at 3 different charge pump frequencies: 8.192kHz (f_{INPUT} / 4), 32.768kHz (f_{INPUT} x 1), and 262.14kHz (f_{INPUT} x 8). The three frequencies correspond to three nominal load current ranges: 2mA, 20mA, and 60mA, respectively. The SP6680 device optimizes for high power efficiency with a low quiescent current of 100µA at 8.198kHz, 200µA at 32.768kHz, and 1.0mA at 262.14kHz. When there is no external clock signal input, the device is in a low-power shutdown mode drawing 4.4µA (typical) current.

The SP6680 device is ideal for designs using +3.6V lithium ion batteries such as cell phones, PDAs, medical instruments, and other portable equipment. For designs involving power sources above +2.7V up to +6.3V, the internal charge pump switch architecture dynamically selects an operational mode that optimizes efficiency. The SP6680 device regulates the maximum output voltage in steady state to +6.3V.

THEORY OF OPERATION

There are seven major circuit blocks for the SP6680 device. Refer to *Figure 1*.

1) The Voltage Reference contains a band gap and other circuits that provide the proper current biases and voltage references used in the other blocks.

2) The Clock Manager accepts the digital input voltage levels (including the input clock) and translates them to V_{CC} and 0V. It also determines if a clock is present in which case the device is powered up. If the CLK input is left floating or pulled near ground, the device shuts down and V_{IN} is shorted to V_{OUT}. The worst case digital low is 0.4V and the worst case digital high is 1.3V. This block contains a synthesizer that generates the internal pump clock which runs at the frequency controlled with the C/4 and Cx8 logic pins.

3) The Charge Pump Switch Configuration Control determines the pump configuration depending upon V_{IN} as described earlier and programs the Clock Phase Control. For an input supply voltage from +2.7V to +3.7V, an X2 doubling architecture is enabled. This mode requires one flying capacitor and one output capacitor. For an input supply voltage greater than +3.7V up to +6.3V, an X1.5 multiplier architecture is enabled. This mode requires two flying capacitors and one output capacitor.

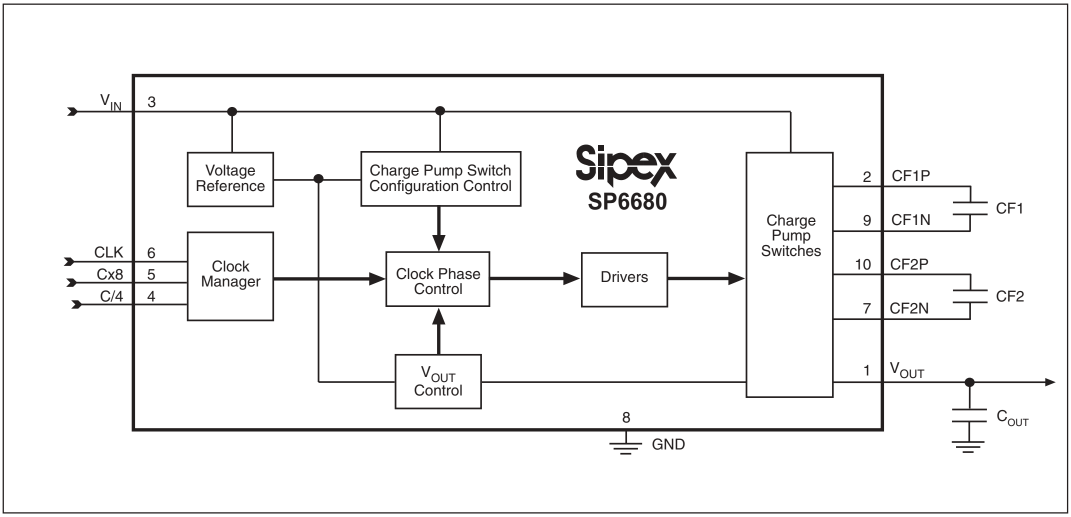


Figure 1. Internal Block Diagram of the SP6680

4) The Clock Phase Control accepts the clock and mode control generated by the Clock Manager and the Charge Pump Switch Configuration Control. This block then provides several clock phases going to the Drivers block.

5) The V_{OUT} Control regulates the Clock Phase Control to ensure V_{OUT} does not exceed +6.0V.

6) The Drivers block drives the clock phase information to the gates of the large pump transistors.

7) The Charge Pump Switch block contains the large transistors that transfer charge to the fly and load capacitors.

In normal operation of the device V_{IN} is connected between +2.7 and 6.3V. Refer to Figure 2 for a typical application circuit. When no clock is present (CLK is floating or near ground) the device is in shutdown and the output is connected to the input. This shutdown feature will work either in start up or after the device is pumping. Once a clock is present, the band gap is activated, but only if V_{IN} > 2.3V. Otherwise the device remains in shutdown mode. Once the reference voltage is stable, the device begins the pumping operation.

If V_{IN} < 3.70V, the device is configured as a doubler. However, if the output approaches 5.8V, the doubler action is truncated.

If V_{IN} is above 3.70V, the device is reconfigured and multiplies the input by a factor of 1.5. This mode reduces the current drawn from the supply and hence increases the power efficiency. If the output approaches 5.8V again, the charge transfer to the load capacitor is truncated.

APPLICATION INFORMATION

Refer to Figure 3 for a typical SIM card application circuit with the SP6680.

Oscillator Control

The external clock frequency required to drive the internal charge pump oscillator is 32.768kHz (nominal) at the CLK pin. When there is no clock signal present at the CLK pin, the SP6680 device is in a low-power shutdown mode.

C/4 and Cx8 are two control lines for the internal charge pump oscillator. When the C/4 control line is forced to a logic high and the Cx8 control line is at a low, the internal charge pump oscillator is set to 8.192kHz. When both the C/4 and Cx8 control lines are at a logic low, the internal charge pump oscillator is set to the input clock signal, 32.768kHz. When the C/4 control line is forced to a logic high, the internal charge pump oscillator is set to 262.14kHz.

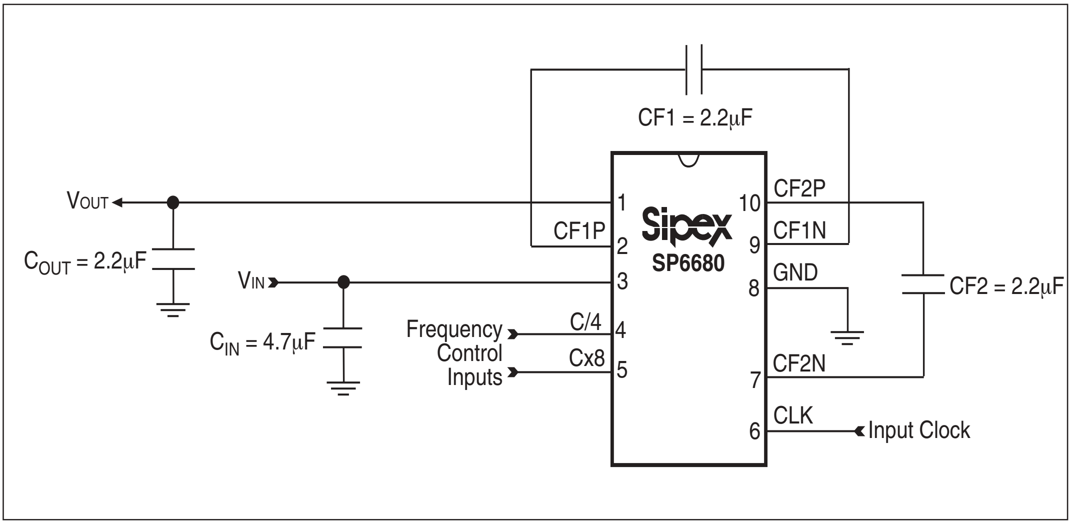


Figure 2. Typical Application for the SP6680

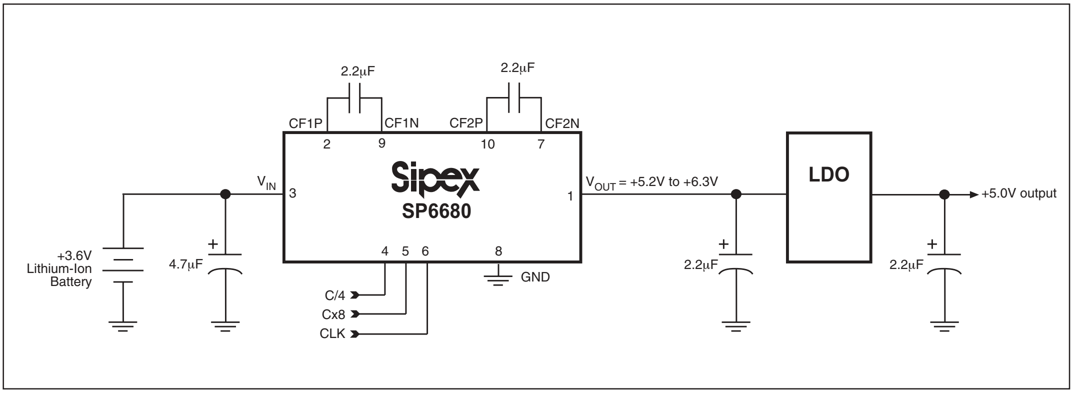


Figure 3. Typical SIM Card Application Circuit for the SP6680

Any standard CMOS logic output is suitable for driving the C/4 or Cx8 control lines as long as logic low is less than 0.4V and logic high is greater than 1.3V.

CLK pin	C/4 pin	Cx8 pin	f_{PUMP}
not present	X	X	0
32.768kHz	low	low	32.768kHz
32.768kHz	low	high	262.14kHz
32.768kHz	high	low	8.192kHz
32.768kHz	high	high	262.14kHz

Table 1. Control Line Logic for the Internal Charge Pump Oscillator

Efficiency

Power efficiency with the SP6680 charge pump regulator is improved over standard charge pumps doubler circuits by the inclusion of an 1.5X output mode, as described in the Theory of Operation section. The net result is an increase in efficiency at battery inputs greater than 3.7 to 3.8V where the SP6680 switches to the 1.5X mode. This is illustrated in figure 4 Efficiency vs Input Voltage.

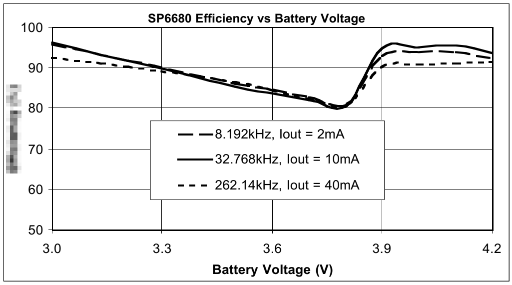


Figure 4. Efficiency vs Battery Voltage

Capacitor Selection

In order to maintain the lowest output resistance, input ripple voltage and output ripple voltage, multi-layer ceramic capacitors with inherently low ESR are recommended. Refer to Table 2 for some suggested low ESR capacitors. Tables of output resistance and ripple voltages for a variety of input, output and pump capacitors are included here to use as a guide in capacitor selection. Measured conditions are with CLK = 32kHz, 5mA output load and all capacitors are 2.2uF except when stated otherwise. A DC power supply with added 0.25ohm output ESR was used to simulate a Lithium Ion Battery as shown in figure 5.

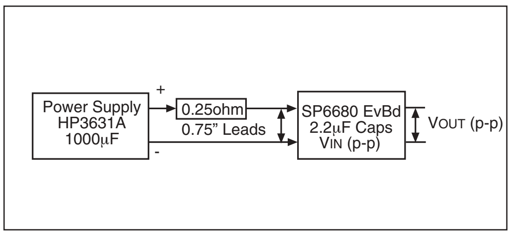


Figure 5. Capacitor Selection Test Circuit

MANUFACTURER / TELEPHONE #	PART NUMBER	CAPACITANCE / VOLTAGE	MAX ESR @ 100kHz	CAPACITOR SIZE / TYPE
TDK / 847-803-6100	C2012X5R1A225K	2.2µF / 10V	0.030Ω	0805 / X5R
TDK / 847-803-6100	C3216X5R1C475K	4.7µF / 10V	0.020Ω	1206 / X5R
AVX / 843-448-9411	1206ZC225K	2.2µF / 10V	0.030Ω	1206 / X7R
Taiyo Yuden / 847-925-0888	LMK212BJ225MG	2.2µF / 10V	0.030Ω	0805 / X5R
Taiyo Yuden / 847-925-0888	LMK316BJ475ML	4.7µF / 10V	0.020Ω	1206 / X7R

Figure 2. Suggested Low ESR Cermic Surface Mount Capacitors.

Board Layout

PC board layout is an important design consideration to mitigate switching current effects. High frequency operation makes PC layout important for minimizing ground bounc and noise. Components should be place as close to the IC as possible with connections made through short, low impedance traces. To maximize output ripple voltage, use a ground plane and solder the IC's GND pin directly to the ground plane.

Output Resistance with Various Output and Pump Capacitors

From Tables 3 & 4 it can be seen that increasing output capacitance alone reduces the output resistance more than increasing pump capacitance. This offers the advantage of increasing one capacitor versus two capacitors in the case for the pump capacitance.

Table 3. Output Resistance vs Output Capacitance
All Ceramic Capacitors ESR < 0.05ohm
Cin, CF1, CF2 = 2.2uF, Vin = 3.85V, Iout = 5mA, CLK = 32kHz

Cout (uF)	SP6680 Rout (ohms)
0.47	57
1	28
2.2	18
4.7	13
10	11
22	10

Table 4. Output Resistance vs Pump Capacitance
All Ceramic Capacitors ESR < 0.05ohm
Cin, Cout = 2.2uF, Vin = 3.85V, Iout = 5mA, CLK = 32kHz

CF1, CF2 (uF)	SP6680 Rout (ohms)
0.47	39
1	24
2.2	18
4.7	15
10	14
22	13

Input Voltage Ripple with Various Input, Output and Pump Capacitors

Looking at Tables 5, 6 & 7 it can be seen that increasing the value of the input capacitor (Table 5) reduces the input voltage ripple the most. Note that placement of this input bypass capacitor as close to the SP6680 input is recommended. Also note that Table 7 shows that increasing the pump capacitor beyond the values of the other capacitors (2.2uF) actually increases the input ripple voltage and is not recommended.

Table 5. Input Voltage Ripple vs Input Capacitance
All Ceramic Capacitors ESR < 0.05ohm
Cout, CF1, CF2 = 2.2uF, Iout = 5mA, CLK = 32kHz

	Vin = 3.55V (In Regulation)	Vin = 3.85V (Not in Regulation)
Cin (uF)	Vin Ripple mV (pp)	Vin Ripple mV (pp)
0.47	296	30
1	140	24
2.2	80	18
4.7	36	12
10	24	10
22	14	6

Table 6. Input Voltage Ripple vs Output Capacitance
All Ceramic Capacitors ESR < 0.05ohm
Cin, CF1, CF2 = 2.2uF, Iout = 5mA, CLK = 32kHz

	Vin = 3.55V (In Regulation)	Vin = 3.85V (Not in Regulation)
Cout (uF)	Vin Ripple mV (pp)	Vin Ripple mV (pp)
0.47	90	30
1	74	24
2.2	80	18
4.7	74	14
10	72	12
22	78	12

Table 7. Input Voltage Ripple vs Pump Capacitance
All Ceramic Capacitors ESR < 0.05ohm
Cin, Cout = 2.2uF, Iout = 5mA, CLK = 32kHz

	Vin = 3.55V (In Regulation)	Vin = 3.85V (Not in Regulation)
CF1, CF2 (uF)	Vin Ripple mV (pp)	Vin Ripple mV (pp)
0.47	76	26
1	76	20
2.2	80	18
4.7	154	16
10	162	16
22	162	14

Output Voltage Ripple with Various Input, Output and Pump Capacitors

From Tables 8, 9 & 10 it appears that increasing pump capacitance will reduce output voltage ripple the most. But, as we saw previously in Table 7, input voltage ripple increases with increasing pump capacitance and it is not recommended to use pump capacitors greater than the other capacitor values. It is therefore recommended to use an output capacitor value equal to or slightly above the pump capacitor value. Note that for most designs the SP6680 output will be followed by a Low Dropout Regulator that will greatly reduce the output ripple.

Table 8. Output Voltage Ripple vs Input Capacitance
All Ceramic Capacitors ESR < 0.05ohm
Cout, CF1, CF2 = 2.2uF, Iout = 5mA, CLK = 32kHz

	Vin = 3.55V (In Regulation)	Vin = 3.85V (Not in Regulation)
Cin (uF)	Vout Ripple mV (pp)	Vout Ripple mV (pp)
0.47	90	52
1	92	52
2.2	104	52
4.7	102	52
10	106	52
22	108	52

Table 9. Output Voltage Ripple vs Output Capacitance
All Ceramic Capacitors ESR < 0.05ohm
Cin, CF1, CF2 = 2.2uF, Iout = 5mA, CLK = 32kHz

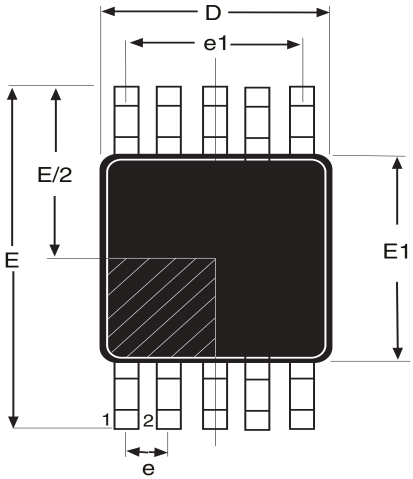
	Vin = 3.55V (In Regulation)	Vin = 3.85V (Not in Regulation)
Cout (uF)	Vout Ripple mV (pp)	Vout Ripple mV (pp)
0.47	102	64
1	102	58
2.2	104	52
4.7	102	46
10	104	44
22	102	44

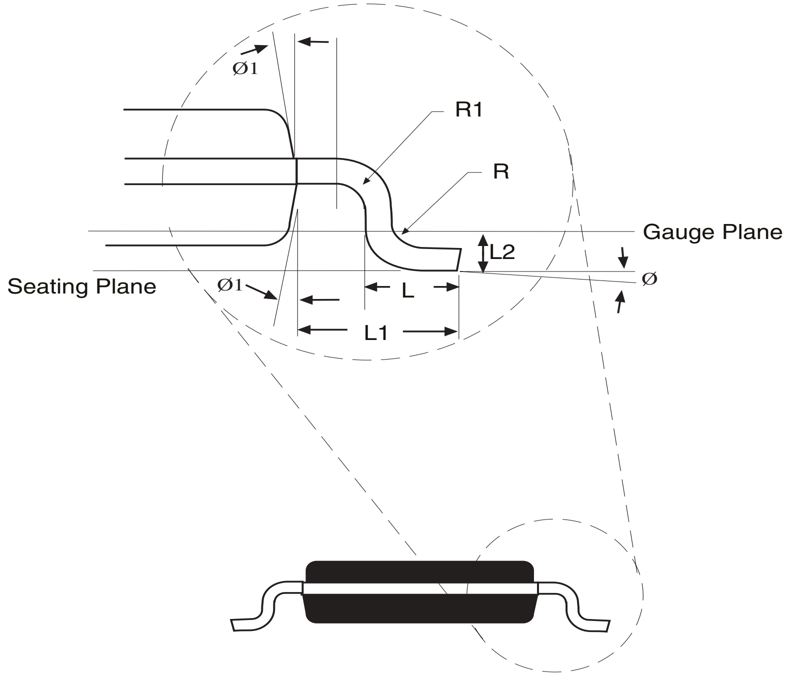
Table 10. Output Voltage Ripple vs Pump Capacitance
All Ceramic Capacitors ESR < 0.05ohm
Cin, Cout = 2.2uF, Iout = 5mA, CLK = 32kHz

	Vin = 3.55V (In Regulation)	Vin = 3.85V (Not in Regulation)
CF1, CF2 (uF)	Vout Ripple mV (pp)	Vout Ripple mV (pp)
0.47	365	200
1	172	108
2.2	108	52
4.7	90	24
10	76	14
22	40	8

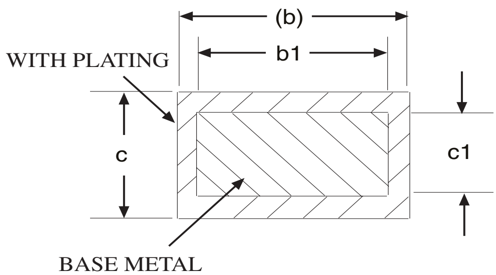
PACKAGE: 10-PIN MSOP

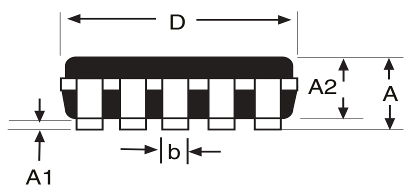
(ALL DIMENSIONS IN MILLIMETERS)





Dimensions in (mm)	10-PIN MSOP JEDEC MO-187 (BA) Variation		
	MIN	TYP	MAX
A	0		1.1
A1	0		0.015
A2	0.75	0.85	0.95
b	0.17		0.27
c	0.08		0.23
D	3.00 BSC.		
E	4.90 BSC.		
E1	3.00 BSC.		
e	0.50 BSC.		
e1	2.00 BSC.		
L	0.4	0.60	0.80
L1		0.95	
L2		0.25	
N		10	
R	0.07		
R1	0.07		
Ø	0º		8º
Ø1	0º		15º





ORDERING INFORMATION

Part Number	Temperature Range	Package Type
SP6680EU	-40˚C to +85˚C	10-pin MSOP
SP6680EU/TR	-40˚C to +85˚C	10-pin MSOP

Available in lead free packaging. To order add "-L" suffix to part number.
Example: SP6680EU/TR = standard; SP6680EU-L/TR = lead free

/TR = Tape and Reel
Pack quantity is 2500 for MSOP.

ANALOG EXCELLENCE

Sipex Corporation

Headquarters:
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600