NEC

MOS FIELD EFFECT TRANSISTOR
2SJ601

SWITCHING
P-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SJ601 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

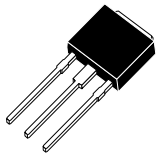
ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ601	TO-251
2SJ601-Z	TO-252

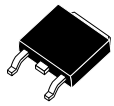
FEATURES

- Low on-state resistance:
  $R_{DS(on)1}$ = 31 mΩ MAX. (V_{GS} = –10 V, I_D = –18 A)
  $R_{DS(on)2}$ = 46 mΩ MAX. (V_{GS} = –4.0 V, I_D = –18 A)
- Low C_{iss}: C_{iss} = 3300 pF TYP.
- Built-in gate protection diode
- TO-251/TO-252 package

(TO-251)



(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–60	V
Gate to Source Voltage (V_{GS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	∓36	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	∓120	A
Total Power Dissipation (T_C = 25°C)	P_T	65	W
Total Power Dissipation (T_A = 25°C)	P_T	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	–35	A
Single Avalanche Energy Note2	E_{AS}	123	mJ

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1%

2. Starting T_{ch} = 25°C, R_G = 25 Ω, V_{GS} = –20 V → 0 V

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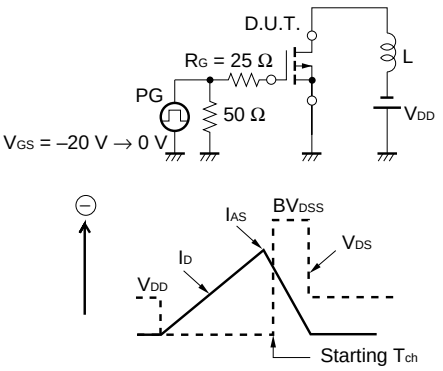
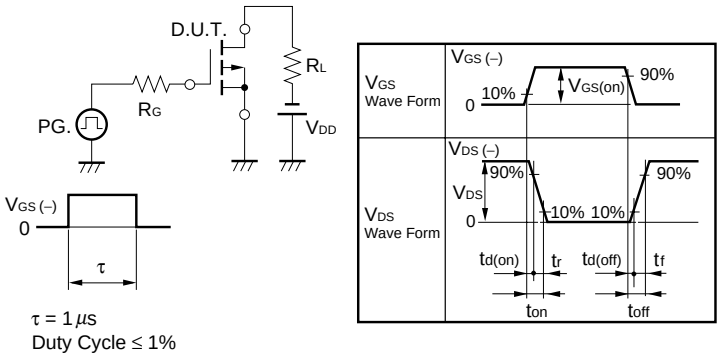
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –60 V, V_{GS} = 0 V			–10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓20 V, V_{DS} = 0 V			∓10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –18 A	15	30		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –18 A		25	31	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.0 V, I_D = –18 A		32	46	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		3300		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		580		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		230		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –30 V, I_D = –18 A		11		ns
Rise Time	t_r	$V_{GS(on)}$ = –10 V		12		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		80		ns
Fall Time	t_f			53		ns
Total Gate Charge	Q_G	V_{DD}= –48 V		63		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –10 V		10		nC
Gate to Drain Charge	Q_{GD}	I_D = –36 A		16		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = –36 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = –36 A, V_{GS} = 0 V		52		ns
Reverse Recovery Charge	Q_{rr}	di/dt = –100 A/μs		108		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

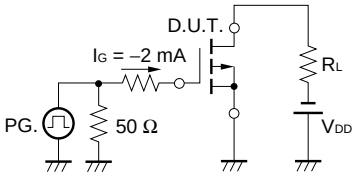


TEST CIRCUIT 2 SWITCHING TIME



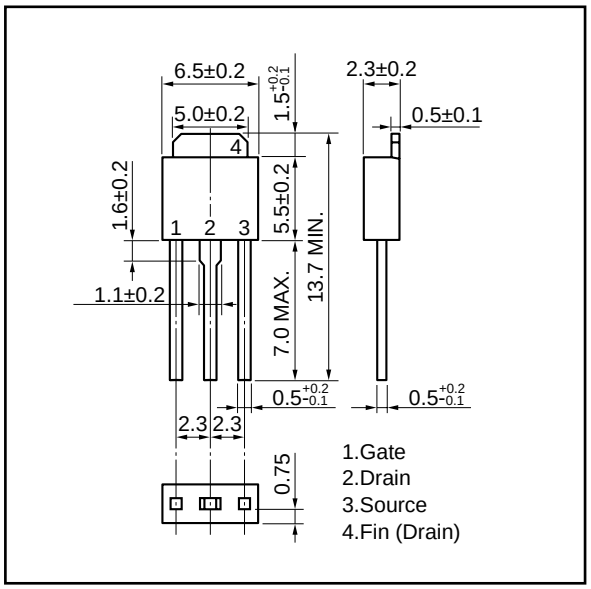
τ = 1 μs
Duty Cycle ≤ 1%

TEST CIRCUIT 3 GATE CHARGE

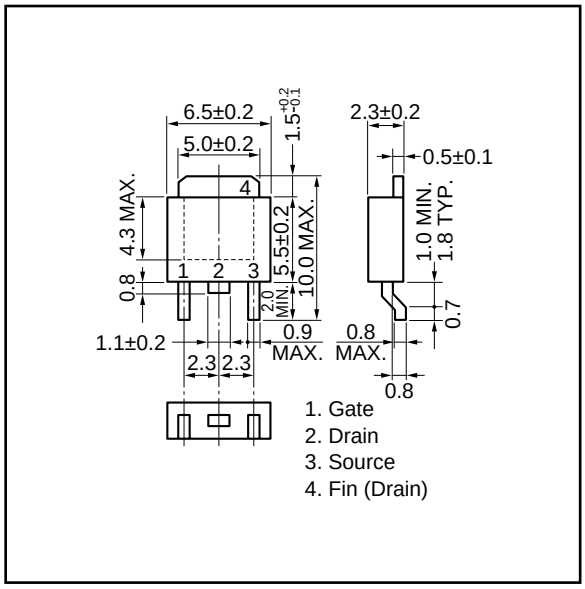


PACKAGE DRAWINGS (Unit : mm)

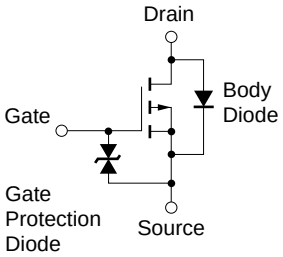
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.