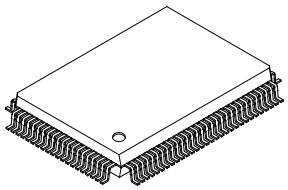
SONY

CXD2412AQ

Timing Generator for LCD Panels

100 pin QFP (Plastic)



Description

The CXD2412AQ is a timing signal generator for LCD panel drivers.

Features

- Generates the LCX007 drive pulse.
- Supports NTSC/PAL.
  (With PAL, a video signal on which scanning line conversion has been performed is used.)
- Supports WIDE.
- Supports HD (20 MHz band).
- Supports Muse-NTSC conversion signal (MNDC).
- Supports up/down and/or right/left inversion.
- Supports three-panel projector.
- Generates timing signal of external sample-and-hold circuit.
- Generates line inversion and field inversion signals.
- AC drive for LCD panel during no signal.
- AFC circuit supporting static and dynamic fluctuations.

Applications

LCD projectors

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25 °C)

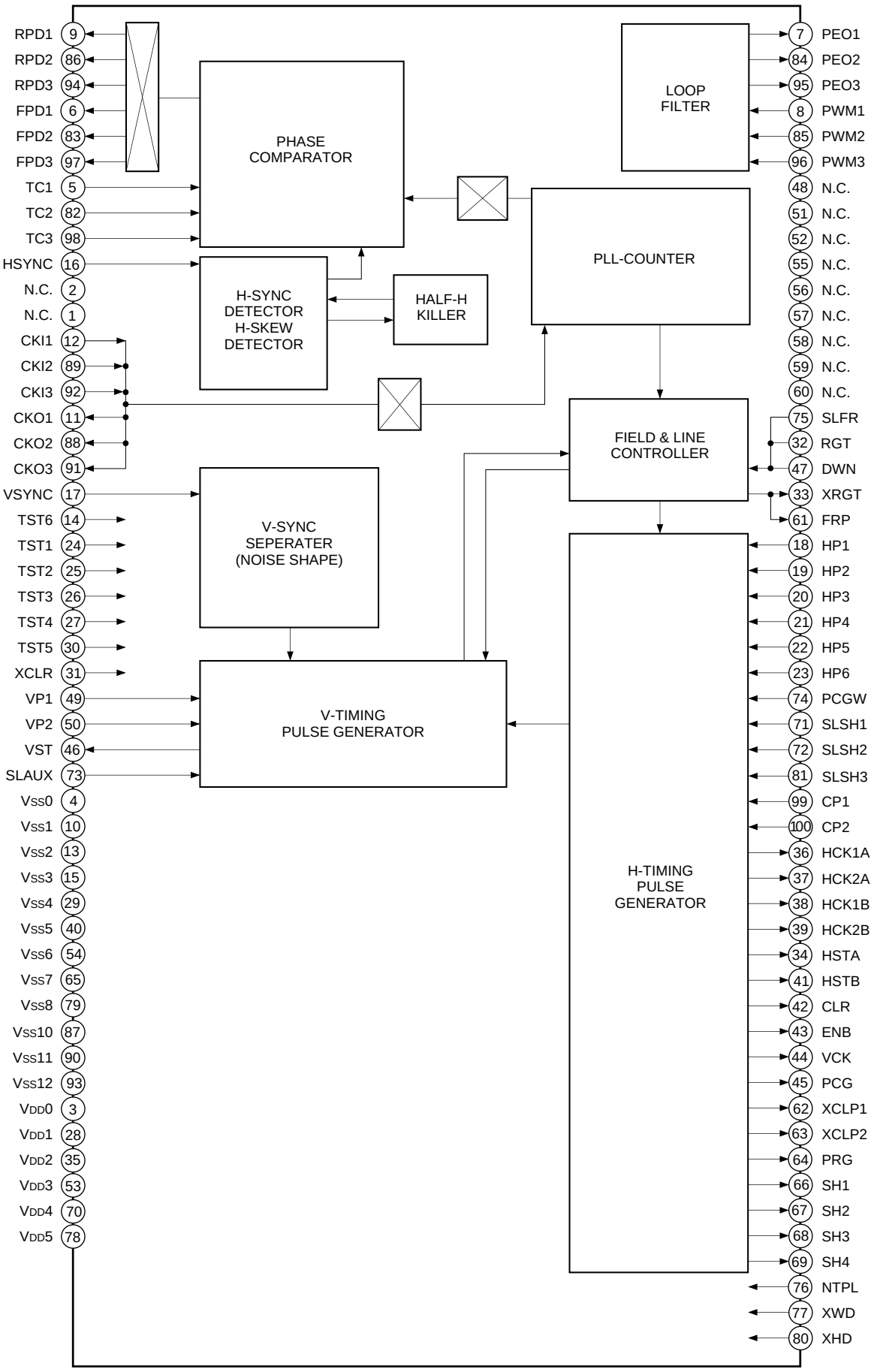
• Supply voltage	V_{DD}	V_{SS}–0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	5.0 ± 0.5	V
• Operating temperature	Topr	–20 to +75	°C

E94Y04-ST

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description	Input pin for open status
1	N.C.	—	Not connected	
2	N.C.	—	Not connected	
3	$V_{DD}0$	—	Power supply	
4	$V_{SS}0$	—	GND	
5	TC1	I	FPD1 pin pulse width adjustment	
6	FPD1	O	Phase comparator output B-1 (for NTSC/PAL)	
7	PEO1	O	Loop filter integrator output 1	
8	PWM1	I	Loop filter integrator input 1	
9	RPD1	O	Phase comparator output A-1 (for NTSC/PAL)	
10	$V_{SS}1$	—	GND	
11	CKO1	O	NTSC/PAL oscillation cell output	
12	CKI1	I	NTSC/PAL oscillation cell input	
13	$V_{SS}2$	—	GND	
14	TST6	I	Test	L
15	$V_{SS}3$	—	GND	
16	HSYNC	I	Hsync input (negative polarity)	
17	VSYNC	I	Vsync input (negative polarity)	
18	HP1	I	Switches for the horizontal display start position	L
19	HP2	I	Switches for the horizontal display start position	L
20	HP3	I	Switches for the horizontal display start position	L
21	HP4	I	Switches for the horizontal display start position	L
22	HP5	I	Switches for the horizontal display start position	L
23	HP6	I	Switches for the horizontal display start position	H
24	TST1	I	Test	L
25	TST2	I	Test	L
26	TST3	I	Test	L
27	TST4	I	Test	L
28	$V_{DD}1$	—	Power supply	
29	$V_{SS}4$	—	GND	
30	TST5	I	Test	H
31	XCLR	I	Cleared at 0 V	H
32	RGT	I	Right/left inversion identification signal input	H
33	XRGT	O	Right/left inversion identification signal output	
34	HSTA	O	H start pulse A	
35	$V_{DD}2$	—	Power supply	
36	HCK1A	O	H clock pulse 1A	
37	HCK2A	O	H clock pulse 2A	

Pin No.	Symbol	I/O	Description	Input pin for open status
38	HCK1B	O	H clock pulse 1B	
39	HCK2B	O	H clock pulse 2B	
40	$V_{SS}5$	—	GND	
41	HSTB	O	H start pulse B	
42	CLR	O	Clear pulse	
43	ENB	O	Enable pulse	
44	VCK	O	V clock pulse	
45	PCG	O	Precharge pulse	
46	VST	O	V start pulse	
47	DWN	I	Up/down inversion identification signal input	H
48	N.C.	—	Not connected	
49	VP1	I	Switches for the vertical display start position	L
50	VP2	I	Switches for the vertical display start position	H
51	N.C.	—	Not connected	
52	N.C.	—	Not connected	
53	$V_{DD}3$	—	Power supply	
54	$V_{SS}6$	—	GND	
55	N.C.	—	Not connected	
56	N.C.	—	Not connected	
57	N.C.	—	Not connected	
58	N.C.	—	Not connected	
59	N.C.	—	Not connected	
60	N.C.	—	Not connected	
61	FRP	O	AC drive inversion timing output	
62	XCLP1	O	Video signal pedestal clamp pulse 1	
63	XCLP2	O	Video signal pedestal clamp pulse 2	
64	PRG	O	Precharge signal pulse	
65	$V_{SS}7$	—	GND	
66	SH1	O	Sample-and-hold pulse 1	
67	SH2	O	Sample-and-hold pulse 2	
68	SH3	O	Sample-and-hold pulse 3	
69	SH4	O	Resample-and-hold pulse	
70	$V_{DD}4$	—	Power supply	
71	SLSH1	I	Switches SH	L
72	SLSH2	I	Switches SH	L
73	SLAUX	I	Switches free-running identification line number	H
74	PCGW	I	Switches PCG	H

Pin No.	Symbol	I/O	Description	Input pin for open status
75	SLFR	I	Switches between H inversion and F inversion (H: H inversion / L: F inversion)	H
76	NTPL	I	Switches mode	H
77	XWD	I	Switches mode	H
78	$V_{DD}5$	—	Power supply	
79	$V_{SS}8$	—	GND	
80	XHD	I	Switches mode	H
81	SLSH3	I	Switches SH	L
82	TC2	I	FPD2 pin pulse width adjustment	
83	FPD2	O	Phase comparator output B-2 (for WIDE)	
84	PEO2	O	Loop filter integrator output 2	
85	PWM2	I	Loop filter integrator input 2	
86	RPD2	O	Phase comparator output A-2 (for WIDE)	
87	$V_{SS}10$	—	GND	
88	CKO2	O	WIDE oscillation cell output	
89	CKI2	I	WIDE oscillation cell input	
90	$V_{SS}11$	—	GND	
91	CKO3	O	HD/MNDC oscillation cell output	
92	CKI3	I	HD/MNDC oscillation cell input	
93	$V_{SS}12$	—	GND	
94	RPD3	O	Phase comparator output A-3 (for HD/MNDC)	
95	PEO3	O	Loop filter integrator output 3	
96	PWM3	I	Loop filter integrator input 3	
97	FPD3	O	Phase comparator output B-3 (for HD/MNDC)	
98	TC3	I	FPD3 pin pulse width adjustment	
99	CP1	I	Switches pedestal clamp position	H
100	CP2	I	Switches pedestal clamp position	L

Electrical Characteristics

1. DC characteristics

(Temperature = 25°C, Vss = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.5		5.5	V
Input voltage	V_{IH}	TTL input cell	2.2			V
Input voltage	V_{IL}	TTL input cell			0.8	V
Input voltage	V_{IH}	CMOS input cell	$0.7V_{DD}$			V
Input voltage	V_{IL}	CMOS input cell			$0.3V_{DD}$	V
Output voltage	V_{OH}	I_{OH} = –4mA (HCKl, SHm)	V_{DD} – 0.8			V
Output voltage	V_{OL}	I_{OL} = 8mA (HCKI, SHm)			0.4	V
Output voltage	V_{OH}	I_{OH} = –3mA (CKOn, CKIn)	$V_{DD}/2$			V
Output voltage	V_{OL}	I_{OL} = 3mA (CKOn, CKIn)			$V_{DD}/2$	V
Output voltage	V_{OH}	I_{OH} = –2mA (other than the above)	V_{DD} – 0.8			V
Output voltage	V_{OL}	I_{OL} = 4mA (other than the above)			0.4	V
Input leak current	I_{IL}	Pull-up resistor connected	–40	–100	–240	µA
Input leak current	I_{IH}	Pull-down resistor connected	–40	100	240	µA
Output leak current	I_{LZ}	RPDn, FPDn (at high impedance state)	–40		40	µA
Current consumption	IDD	HD mode, V_{DD} = 5.0V (at no load)		75		mA

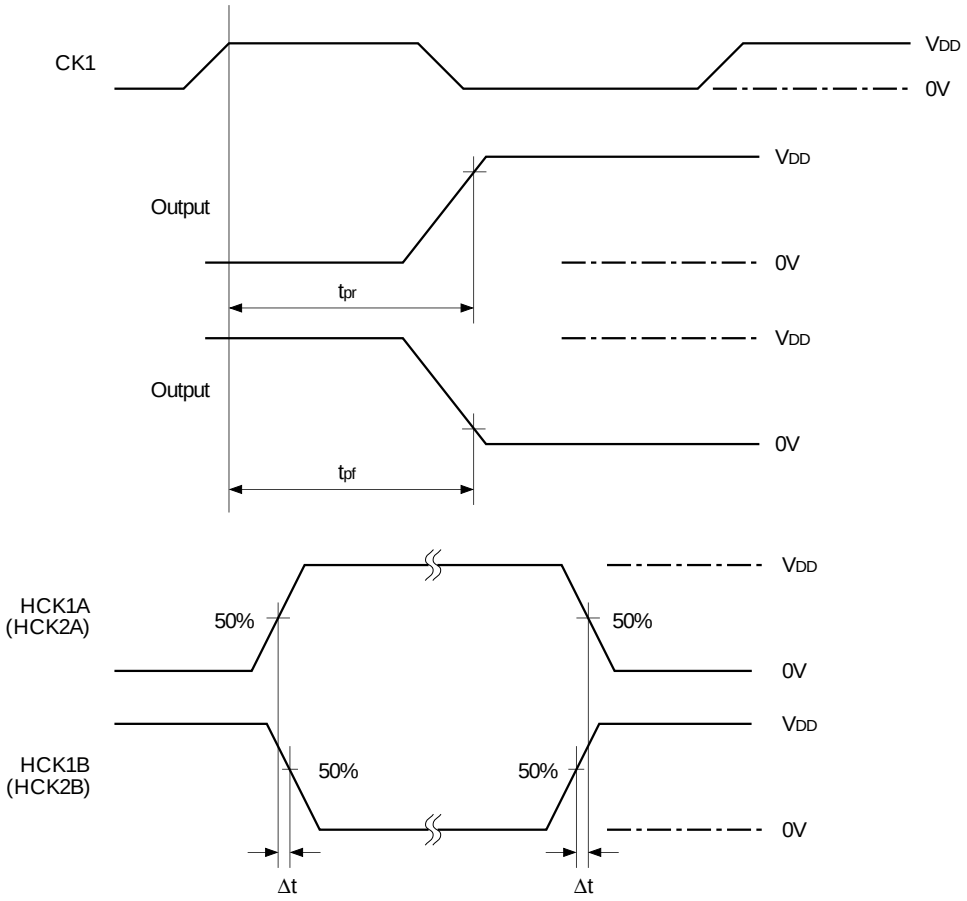
2. AC characteristics

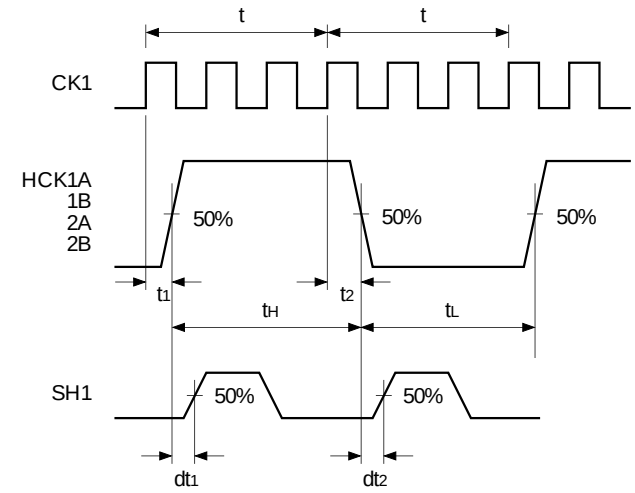
(V_{DD} = 5.0 ± 10%)

Item	Applicable pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock input cycle	CKIn			22			ns
Cross point time difference	HCK1A, HCK2A	Δt	CL = 30pF			10	ns
Cross point time difference	HCK1B, HCK2B	Δt	CL = 30pF			10	ns
Output rise delay	HCKI, SHm	tpr	CL = 30pF			20	ns
Output fall delay	HCKI, SHm	tpf	CL = 30pF			15	ns
Output rise delay	Other than HCK1 and SHm	tpr	CL = 30pF			25	ns
Output fall delay	Other than HCK1 and SHm	tpf	CL = 30pF			15	ns
HCK1, SH1 delay time difference	HCK1A, HCK1B, SH1	dt1	CL = 30pF	0.05		0.25	ns
HCK1, SH1 delay time difference	HCK1A, HCK1B, SH1	dt2	CL = 30pF	1		5	ns
HCK2, SH1 delay time difference	HCK2A, HCK2B, SH1	dt1	CL = 30pF	0.1		0.5	ns
HCK2, SH1 delay time difference	HCK2A, HCK2B, SH1	dt2	CL = 30pF	1		5	ns
HCK1 Duty	HCK1A, HCK1B	tH/tH + tL	CL = 30pF	45		52	%
HCK2 Duty	HCK2A, HCK1B	tH/tH + tL	CL = 30pF	45		52	%

Note) l = 1A, 1B, 2A, 2B
n = 1, 2, 3
m = 1, 2, 3, 4

Timing Definition





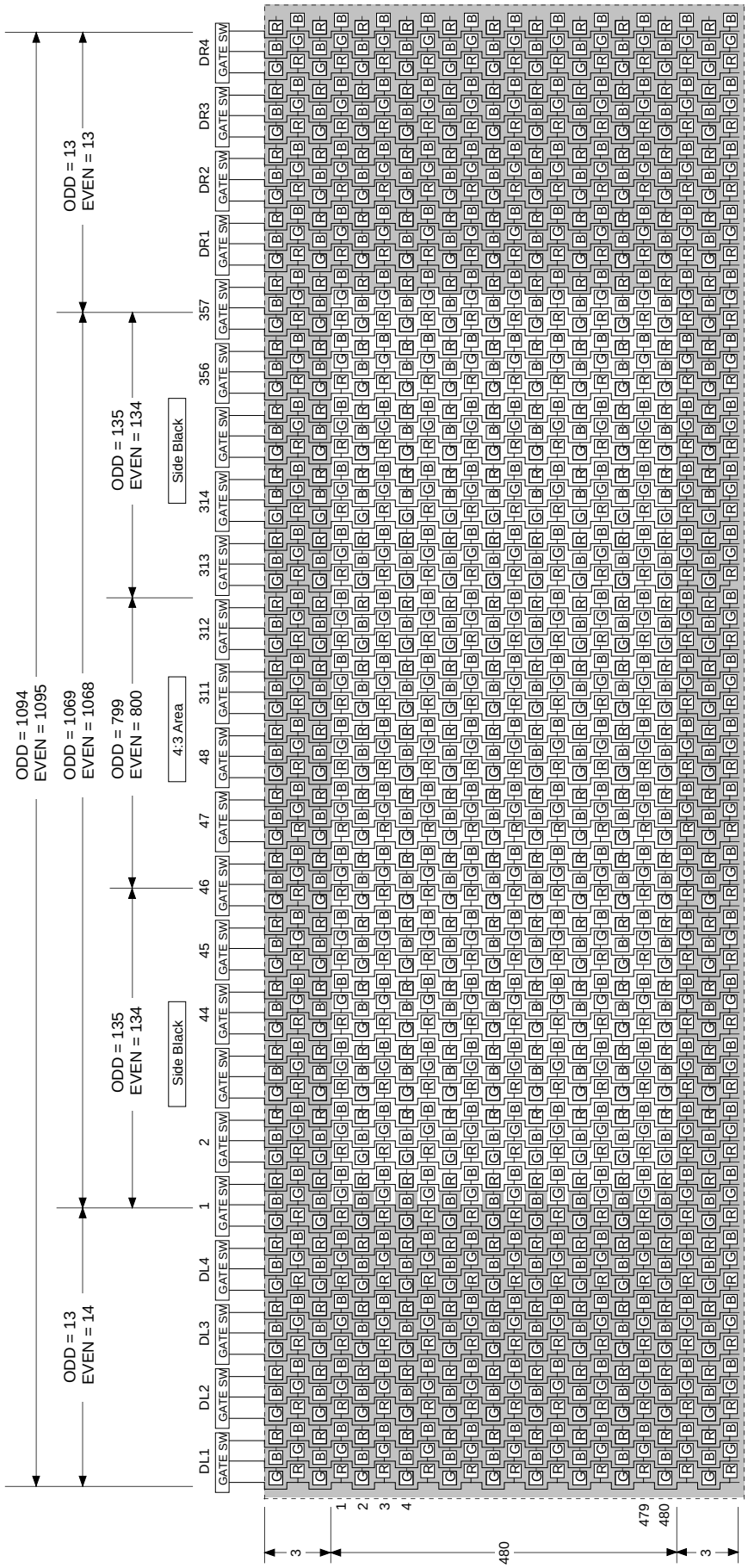
LCD Panel Structure

The structure of LCD panels driven by this IC is shown below.

Dot Arrangement (1) (16 : 9 display)

The dots are arranged in a delta pattern. The shaded area is used for the dark border around the display.

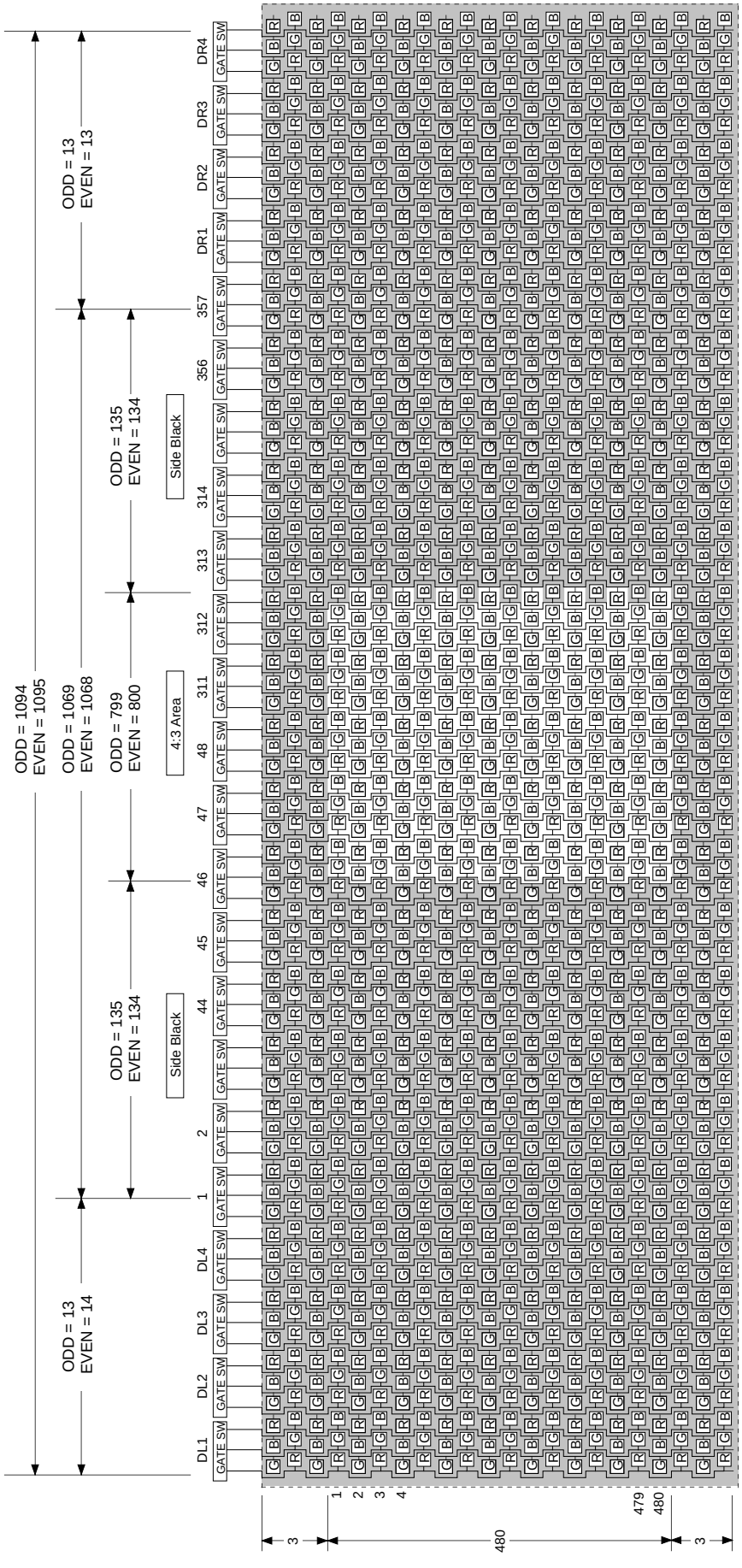
The R corresponds to SIG2, G to SIG1, and B to SIG3, respectively.



Dot Arrangement (2) (4 : 3 display)

The dots are arranged in a delta pattern. The shaded area is used for the dark border around the display.

The R corresponds to SIG2, G to SIG1, and B to SIG3, respectively.



Input Signal Specifications

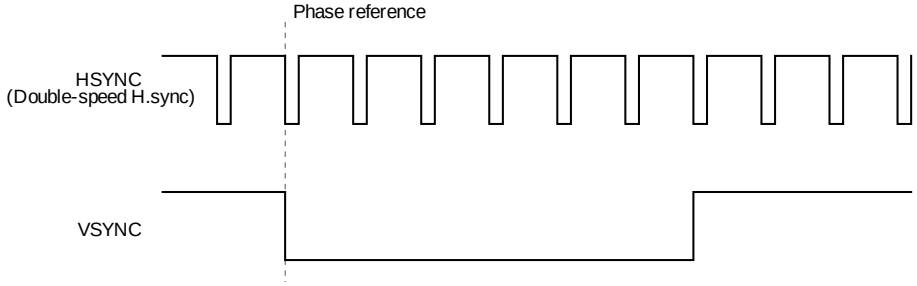
1. Horizontal sync signal

- With NTSC, NTSC WIDE, PAL, PAL+, and MNDC, the standard signal is doubled in speed, and a 1/2 cycle, 1/2 width horizontal sync signal (H.SYNC) is input.
- With HD, a signal derived by cutting off the lower part of 3-value sync is input.
- Negative polarity input is used.

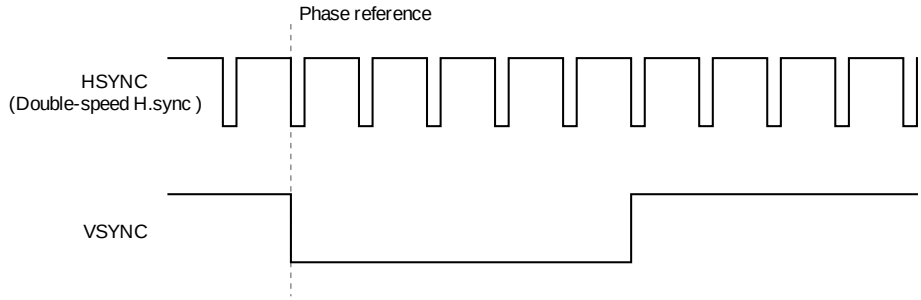
2. Vertical sync signal

- V.sync separated by synchronizing separation circuit and not doubled in speed is input as the vertical sync signal.
- Negative polarity input is used.
- With this TG, the phase relationship between VSYNC and HSYNC is as follows;

(1) NTSC/NTSC WIDE/MNDC

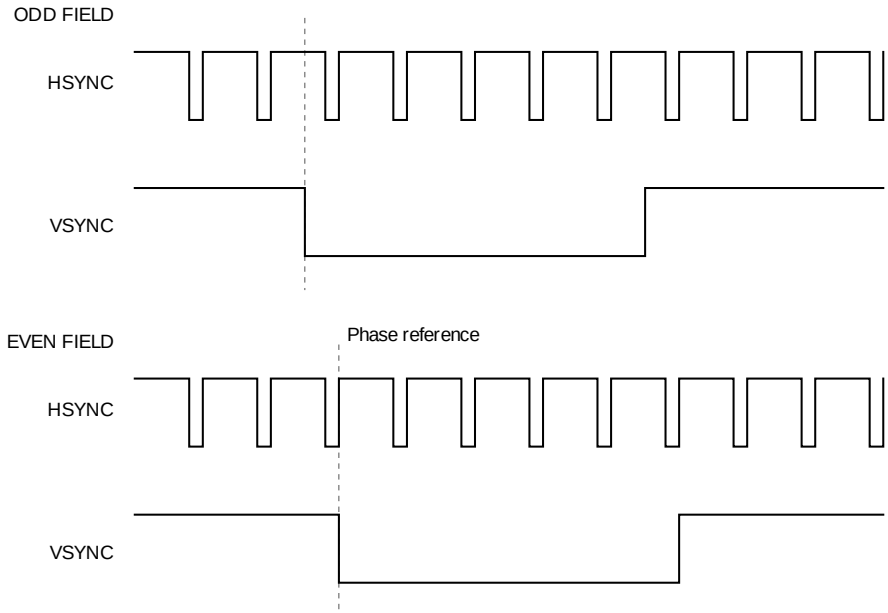


(2) PAL/PAL+



The video signal has a 487-line effective period due to scanning line conversion.

(3) HD



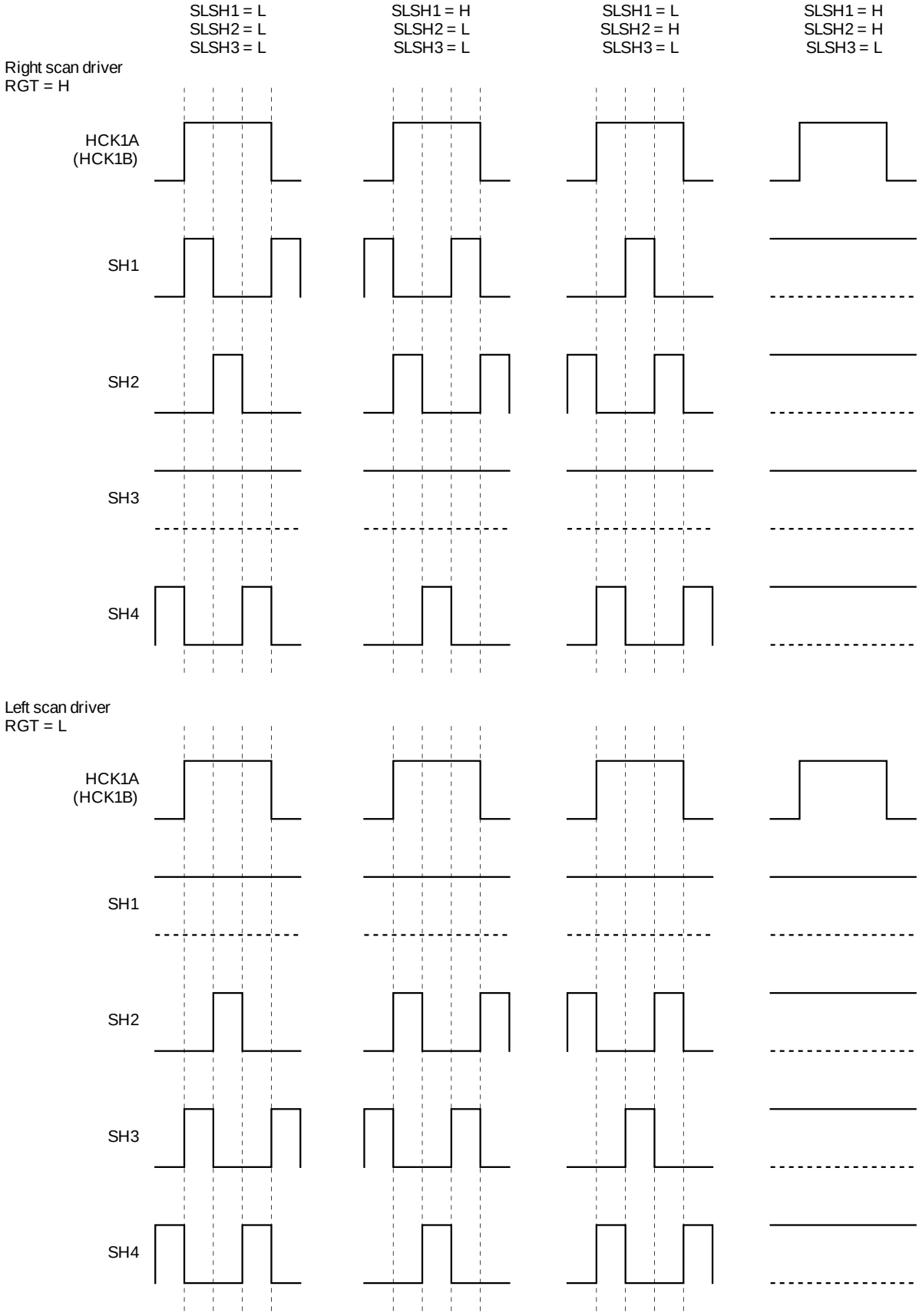
Mode Selection

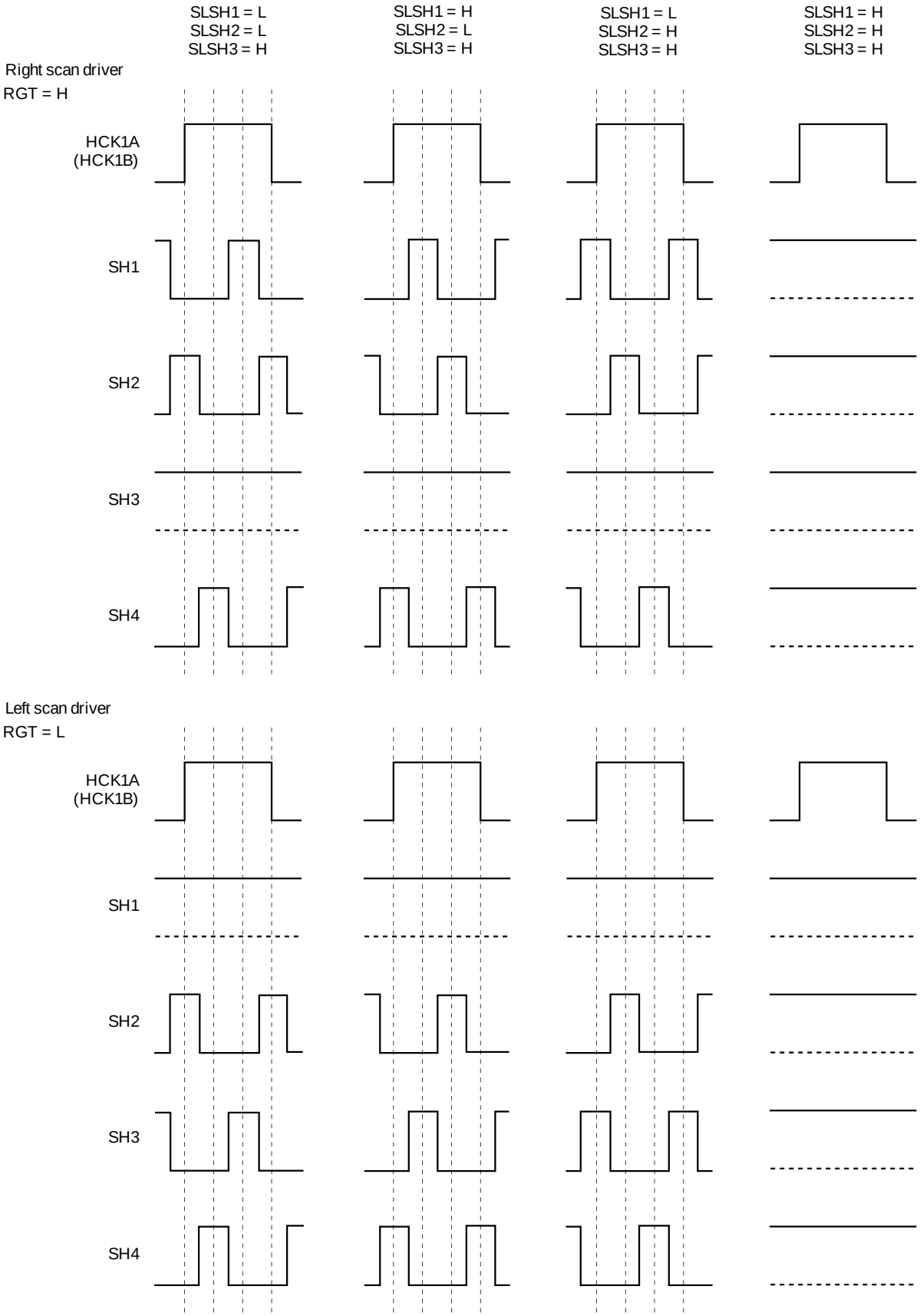
Mode selection is performed by means of three pins, as shown in the table.

NTPL	XWD	XHD	Mode
H	H	H	NTSC
L	H	H	PAL
H	L	H	NTSC WIDE
L	L	H	PAL+
L	X	L	HD
H	X	L	MNDC

SH Pulse Switching

The phase relationship between HCK1A, HCK1B and SH1, SH2, SH3, SH4 is switched by SLSH1, SLSH2, SLSH3.




SLSH1 = L
SLSH2 = L
SLSH3 = H
SLSH1 = H
SLSH2 = L
SLSH3 = H
SLSH1 = L
SLSH2 = H
SLSH3 = H
SLSH1 = H
SLSH2 = H
SLSH3 = H
Right scan driver
RGT = H
HCK1A
(HCK1B)
SH1
SH2
SH3
SH4
Left scan driver
RGT = L
HCK1A
(HCK1B)
SH1
SH2
SH3
SH4

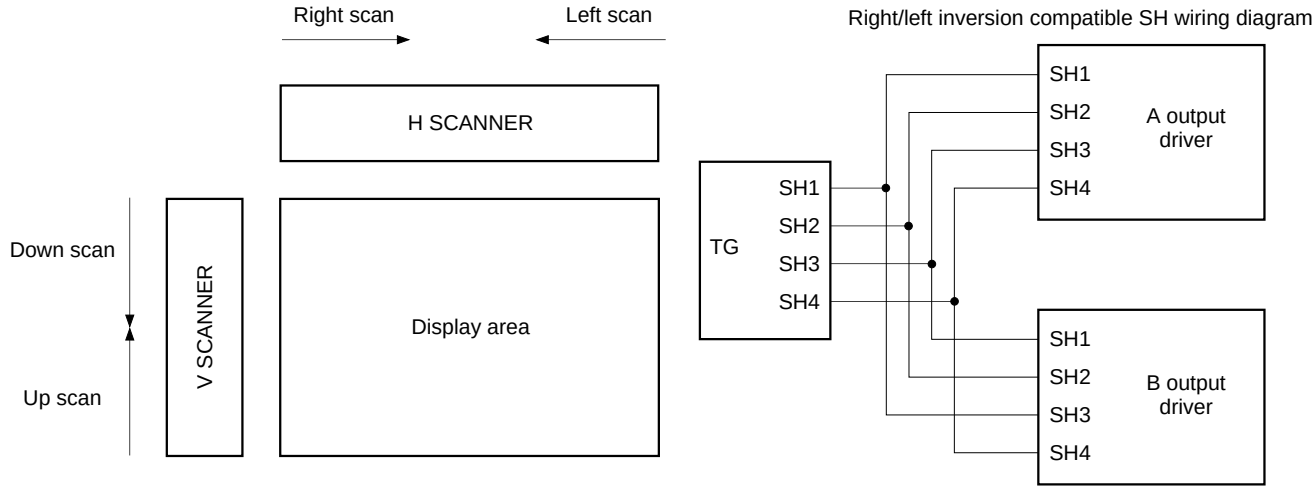
Right/Left Inversion and Up/Down Inversion

The LCD panel is arranged in a delta pattern, where an identical signal line is 1.5-dot offset for every horizontal line. For this reason, a 1.5-bit offset is made to the horizontal start pulse HST of the LCD between lines. HCK and S/H (sample and hold) are also 1.5-bit offset in a similar manner.
When the panel is driven with right/left inversion or up/down inversion, this offset relationship becomes inverted for even and odd lines. Moreover, since the dot arrangement is asymmetrical, the HST position is also offset. Right/left inversion and up/down inversion are supported by the TG as follows.

(1) Two types of output pulses for right scan (A output) and left scan (B output) are prepared for HST, HCK to allow right/left inversion present/absent mixed three-panel LCDs to be driven simultaneously. In addition, XRGT (RGT inverse output) is prepared for the left scan panel. SH1 and SH3 connections to the driver are reversed for sample-and-hold.

(2) Left scan pulses are output to the A output by setting the right/left inversion input pin RGT to low. Also, XRGT is driven high by setting RGT to low.

(3) The A and B outputs output up scan pulses by setting the up/down inversion input pin DWN to low.

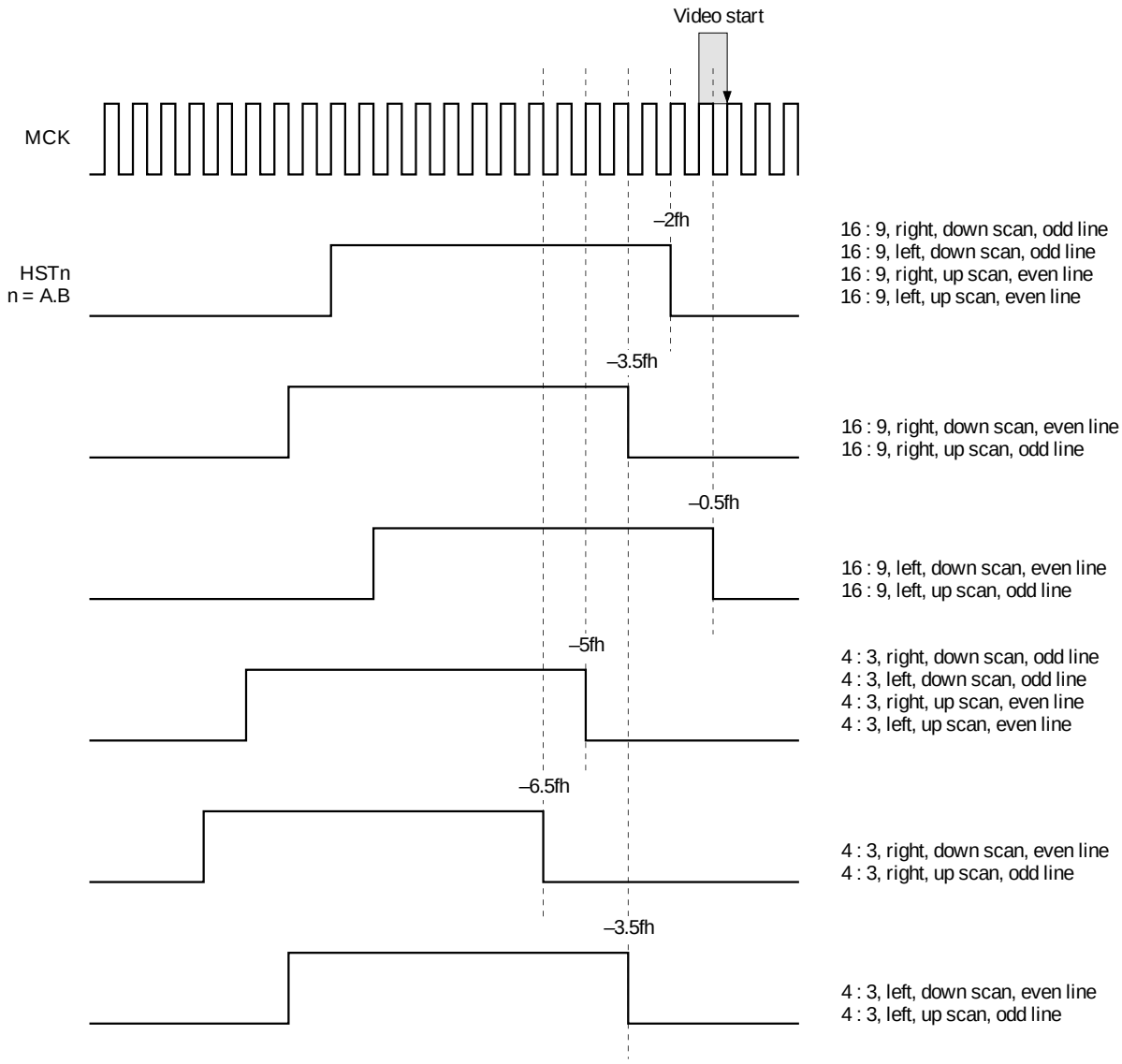


The relationship between the output pins and switches is summarized below.

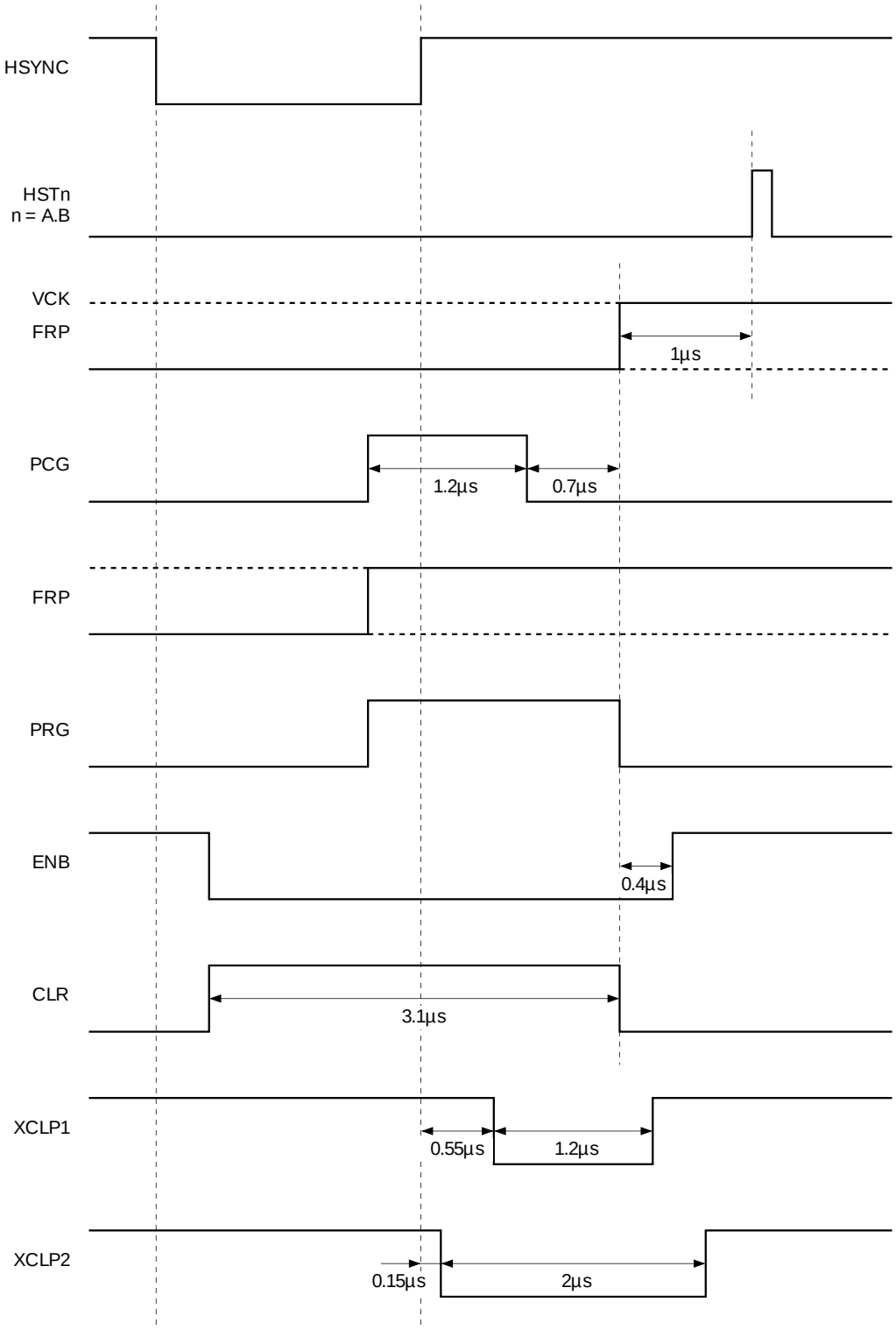
TG input pin		A output HST, HCK	B output HST, HCK (Three-panel LCD auxiliary output)
DWN	RGT		
H	H	For right scan, down scan	For left scan, down scan
H	L	For left scan, down scan	For right scan, down scan
L	H	For right scan, up scan	For left scan, up scan
L	L	For left scan, up scan	For right scan, up scan

Horizontal Output Pulses

The HST pulses are offset for each line in accordance with the dot arrangement.

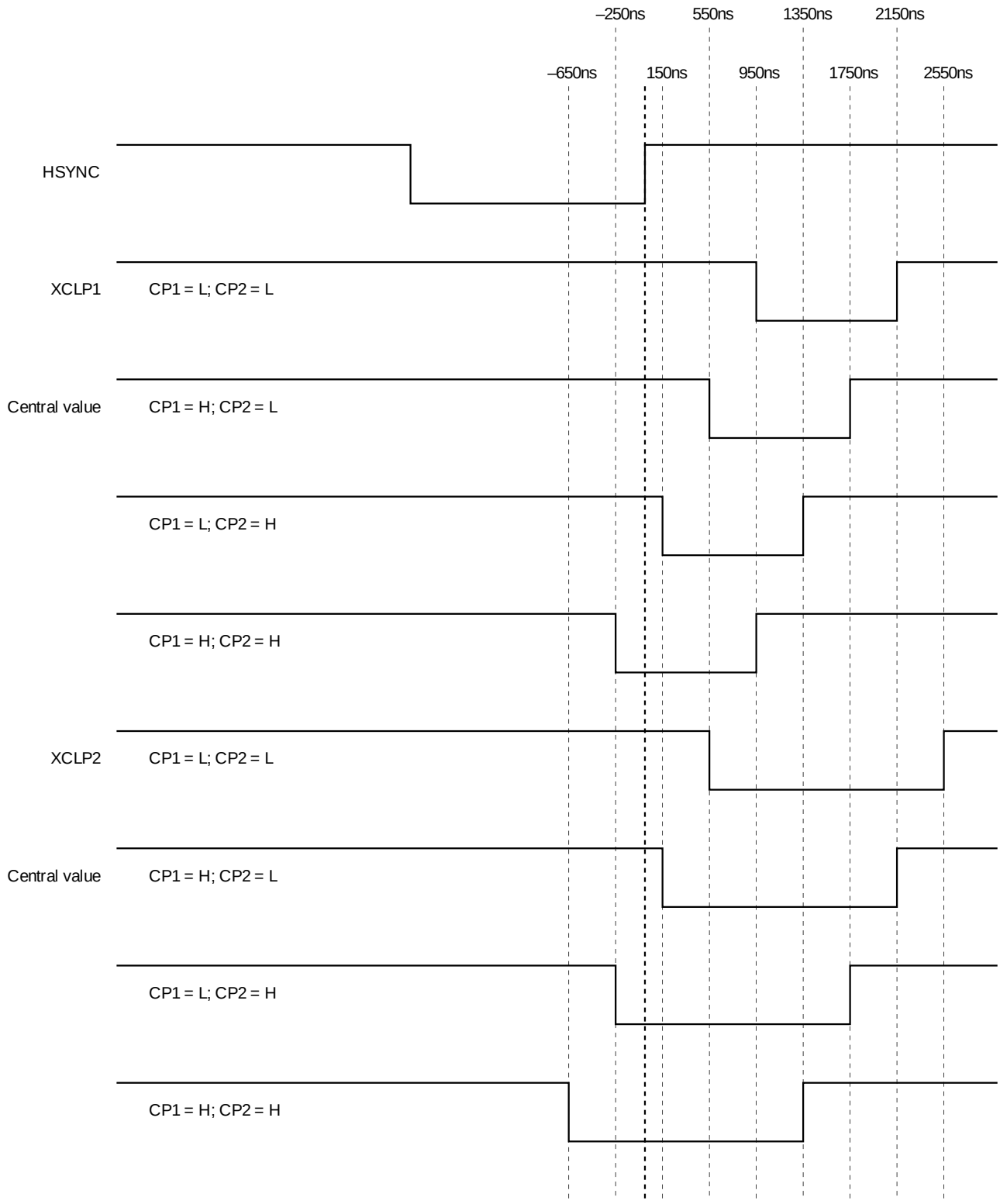


The phase relationship between the horizontal pulses is shown in the figure below.
The display start position can be changed by means of the HP pin while maintaining this relationship.



XCLP Pulse Switching

The phase relationship between HSYNC and XCLP1, XCLP2 is switched by means of CP1 and CP2.



Vertical Output

The vertical display position is varied as shown below.

VP1	VP2	
L	L	After 2H
H	L	After 1H
L	H	Central value
H	H	1H before

LCD Panel AC Driving for No Signal

With no signal, also, provision is made as follows for AC driving of the LCD panel.

Horizontal pulses The PLL is set to the free-running state.
Therefore, the horizontal pulse frequency depends on the PLL free-running frequency.

Vertical pulses The number of lines is counted by an internal counter, and VST and FRP are output in a specific cycle.

VST Cycle with No Signal

SLAUX = L

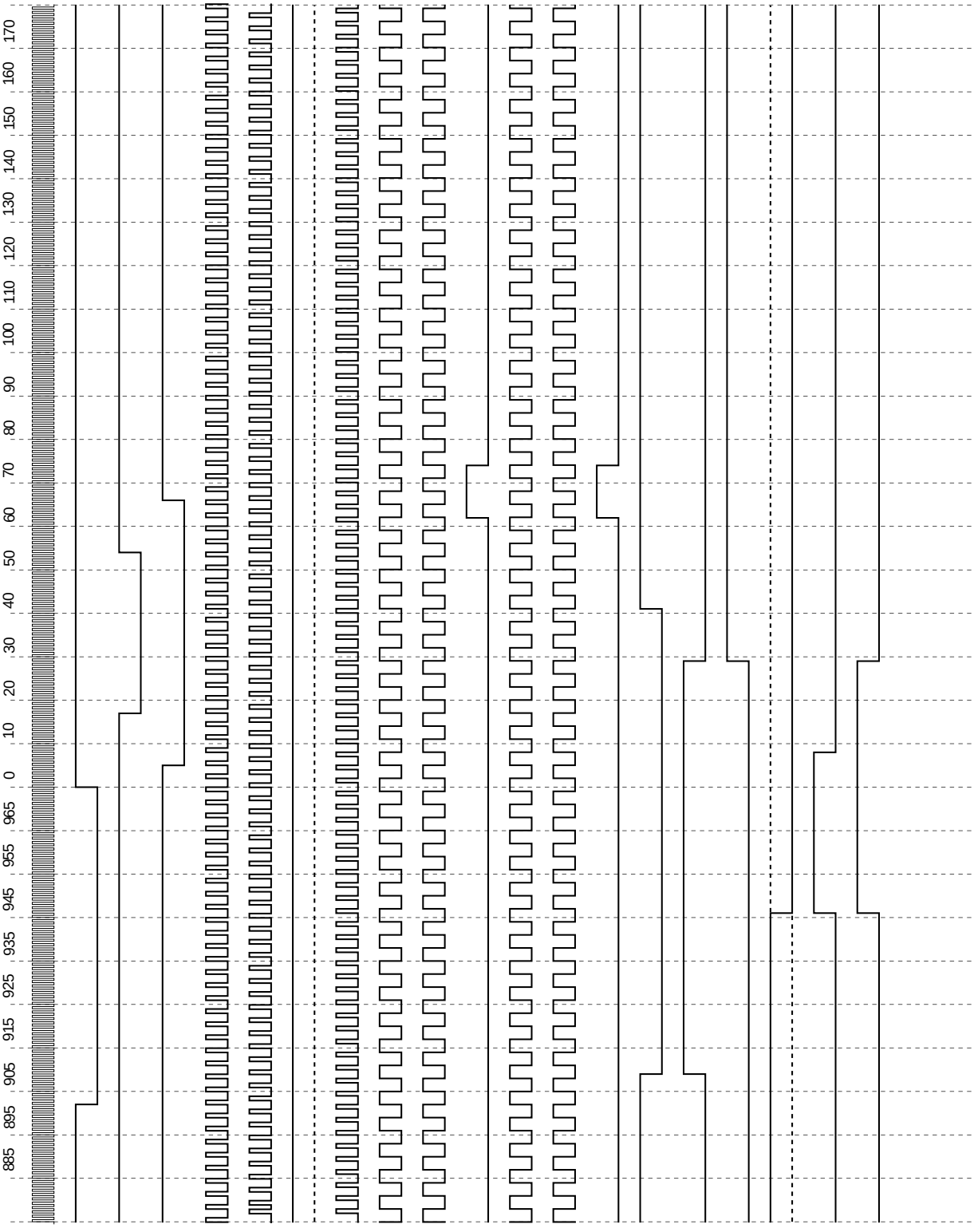
NTSC NTSC-WIDE MNDC	545H
PAL PAL+	641H
HD	577H

SLAUX = H

All modes	769H

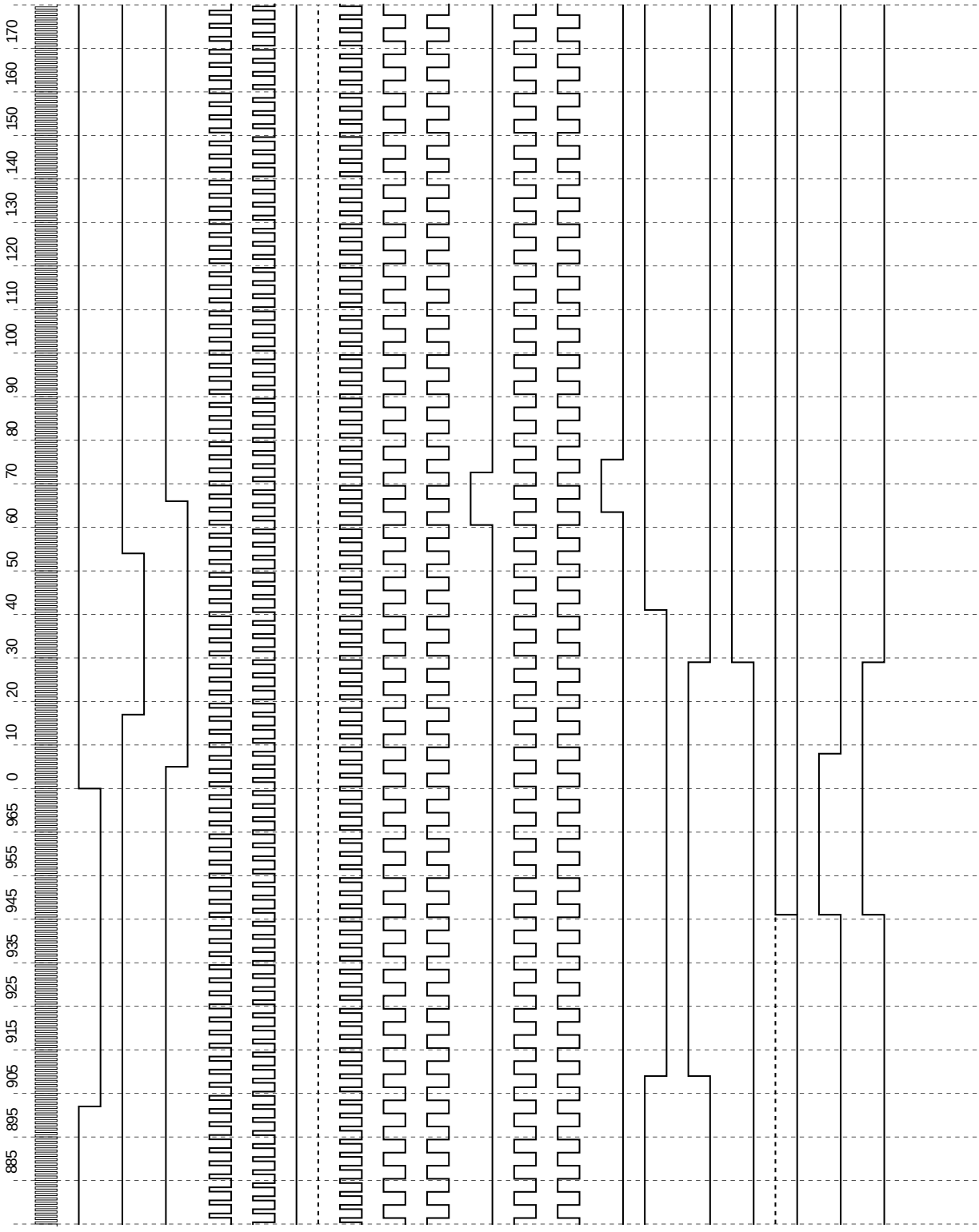
Note) This TG determines there to be no signal if there is no VSYNC input during the above cycle.

NTSC-ODD LINE Horizontal Direction Timing Chart



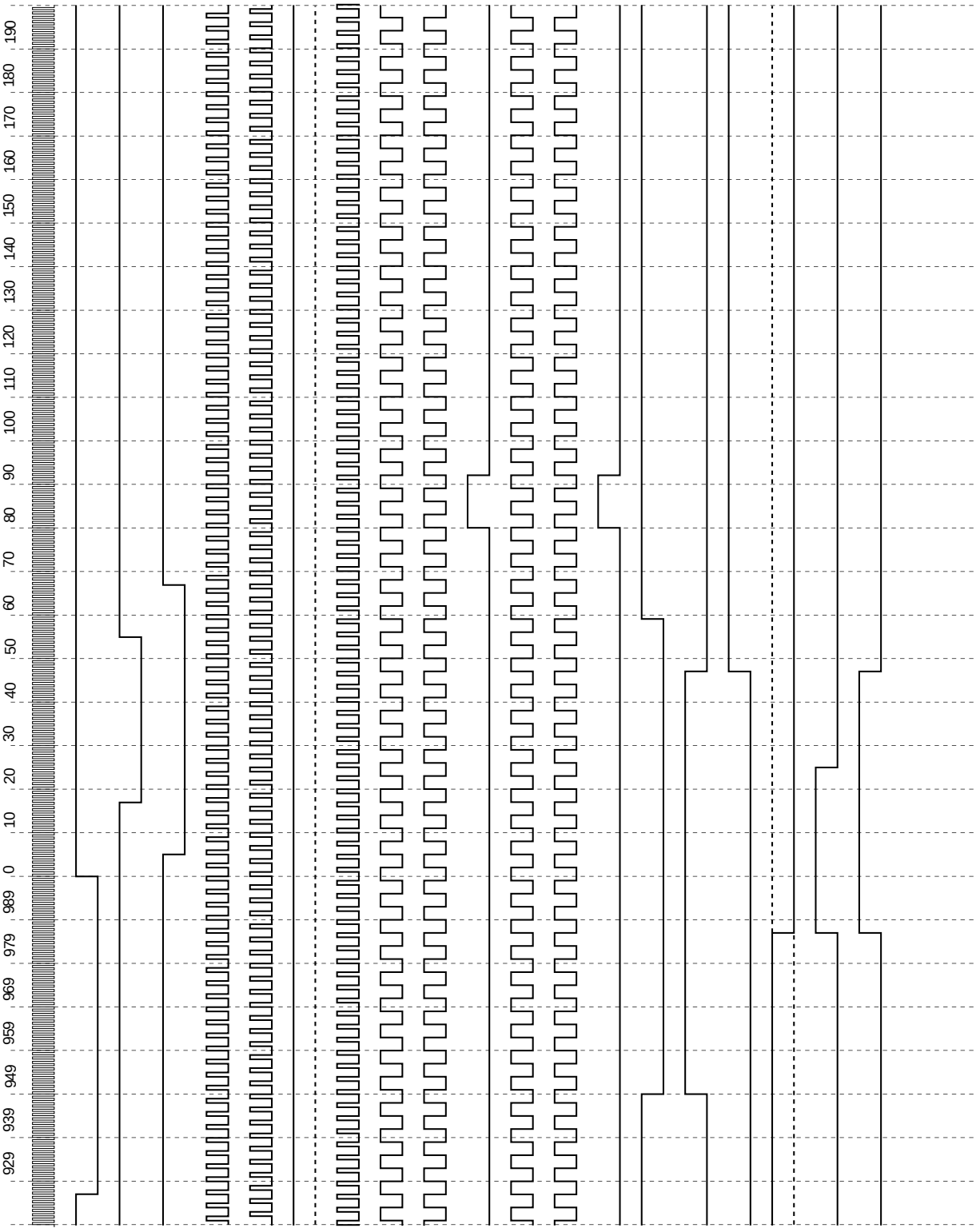
Note) Input pins in default state.

NTSC-EVEN LINE **Horizontal Direction Timing Chart**



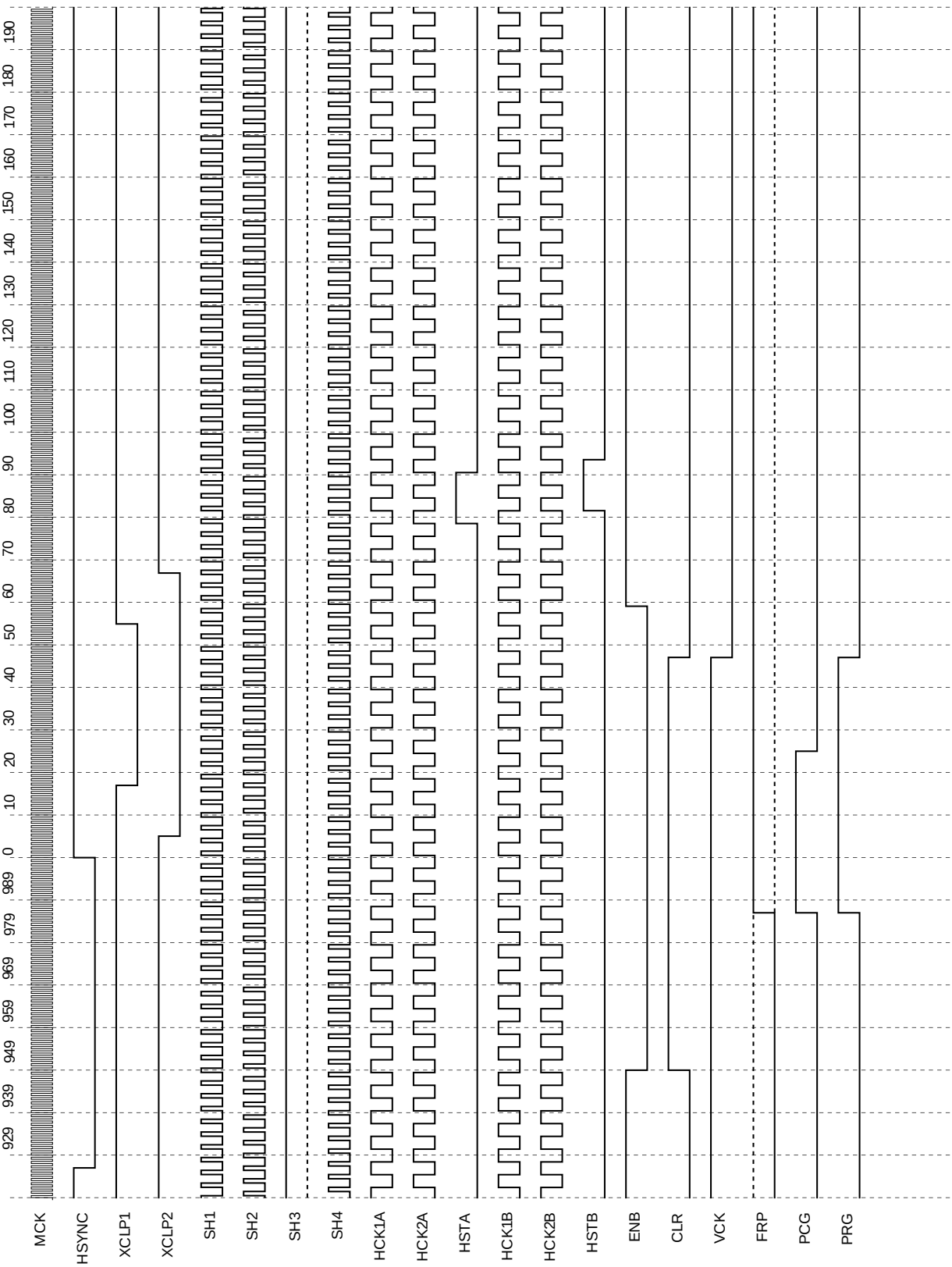
Note) Input pins in default state.

PAL-ODD LINE **Horizontal Direction Timing Chart**

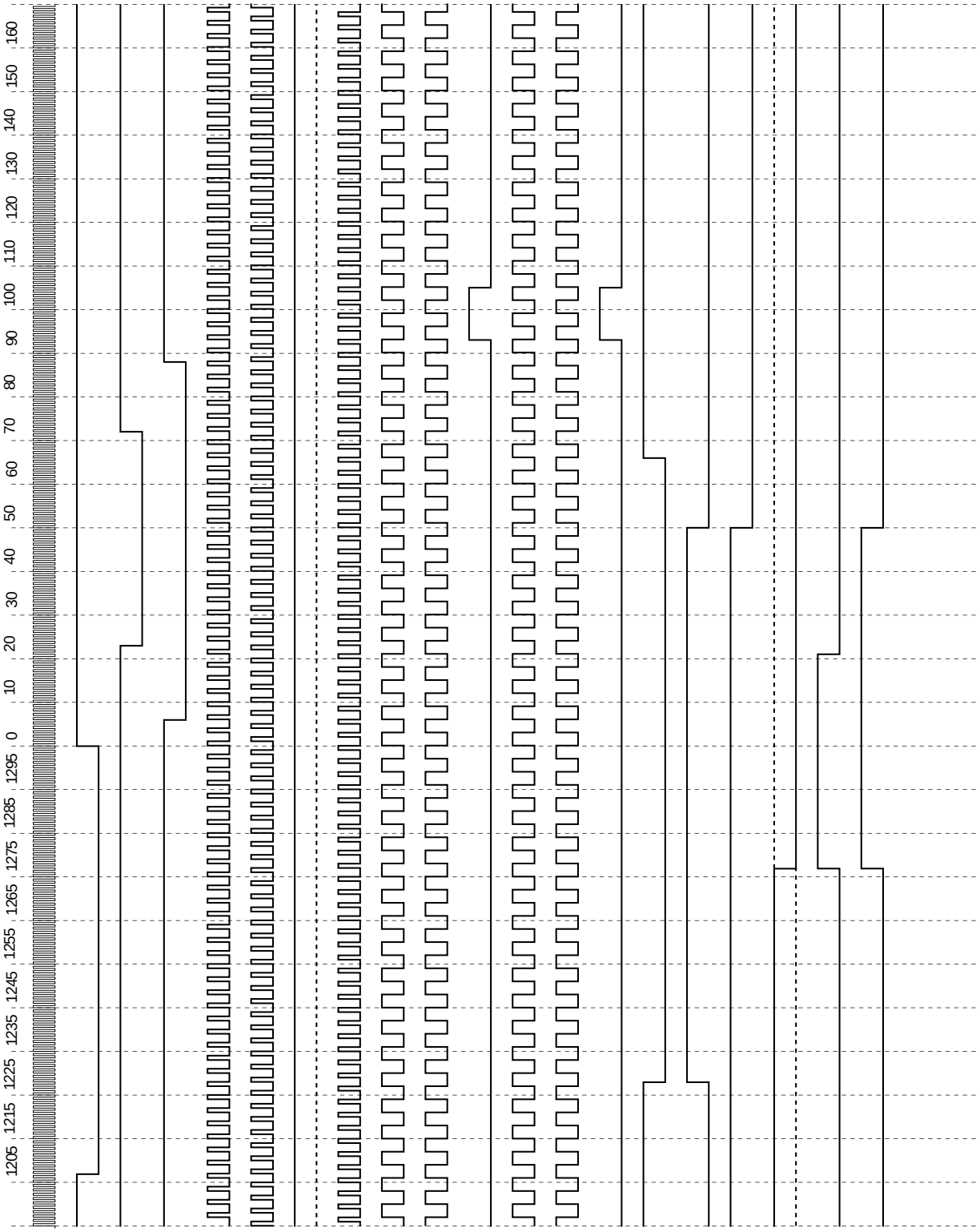


Note) Input pins in default state.

PAL-EVEN LINE **Horizontal Direction Timing Chart**

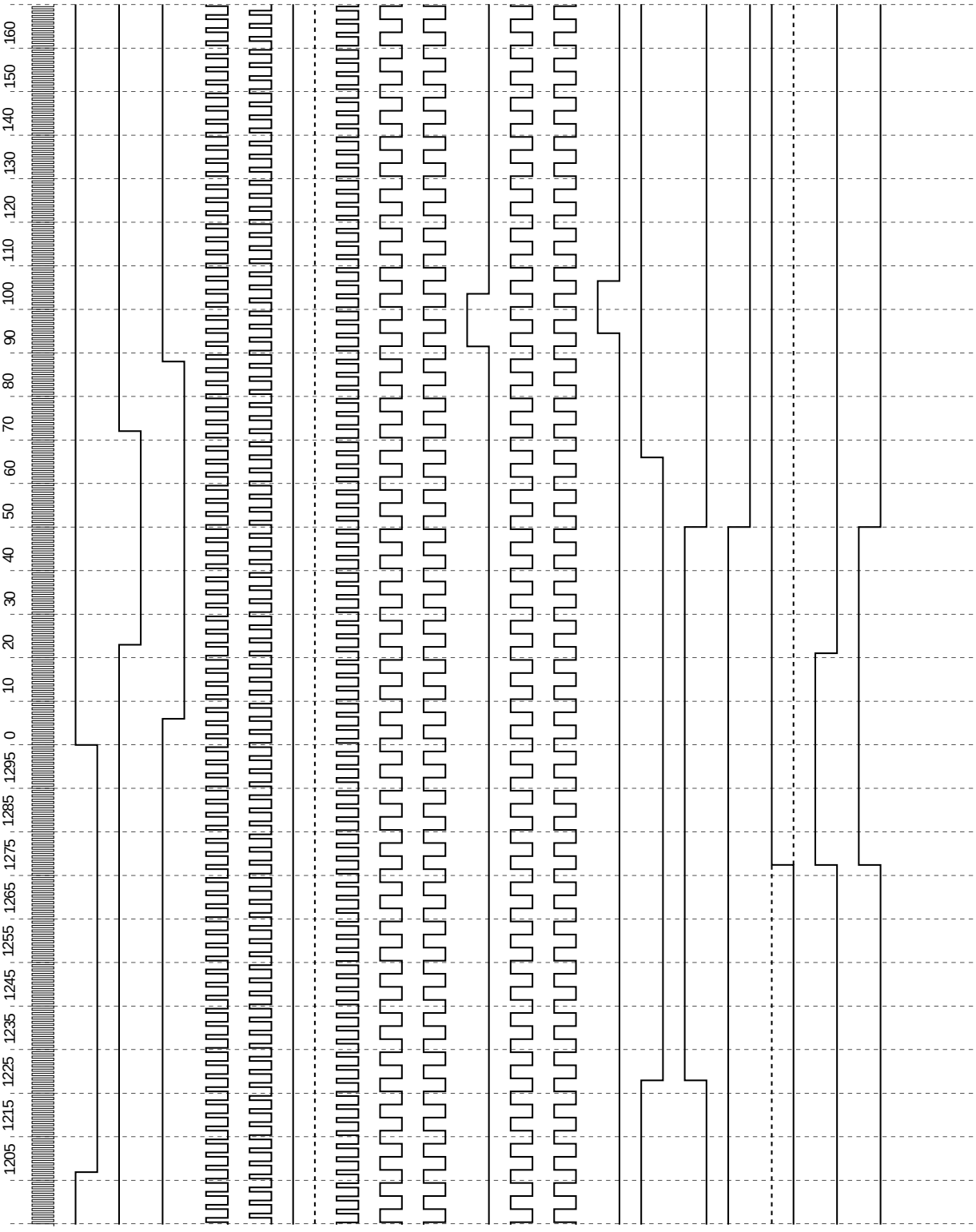


NT-WIDE-ODD LINE **Horizontal Direction Timing Chart**

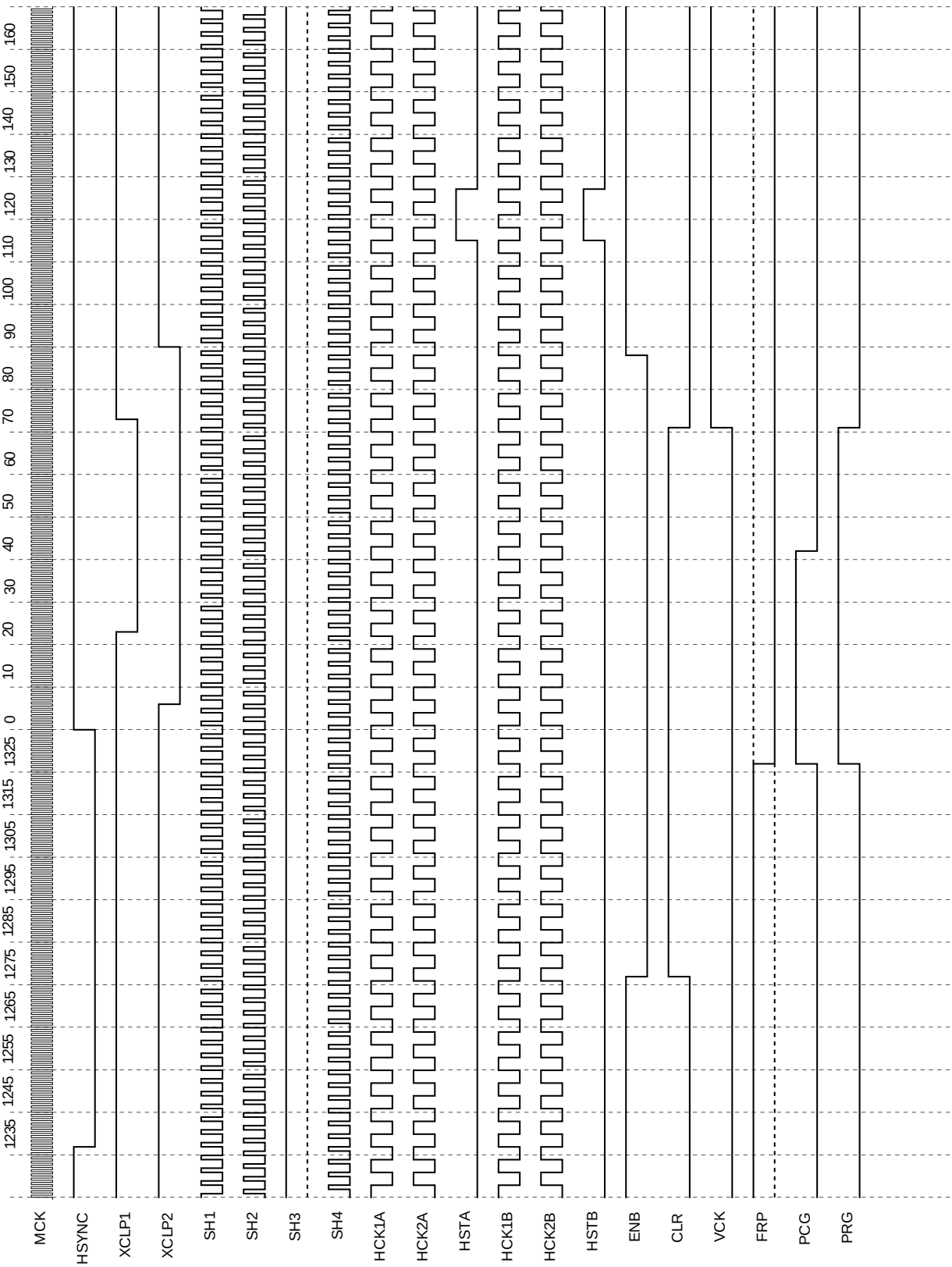


Note) Input pins in default state.

NT-WIDE-EVEN LINE Horizontal Direction Timing Chart

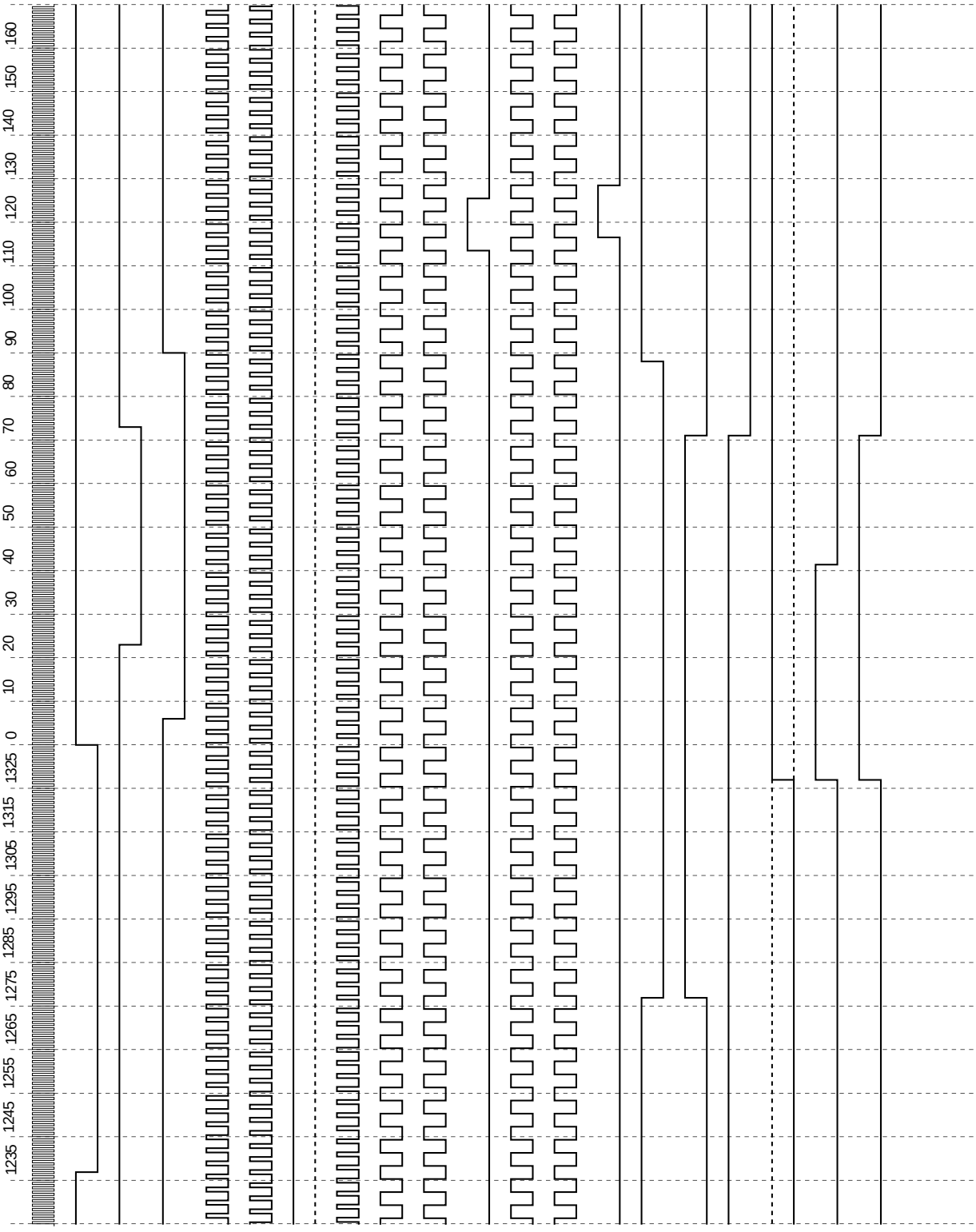


PAL+ -ODD LINE **Horizontal Direction Timing Chart**



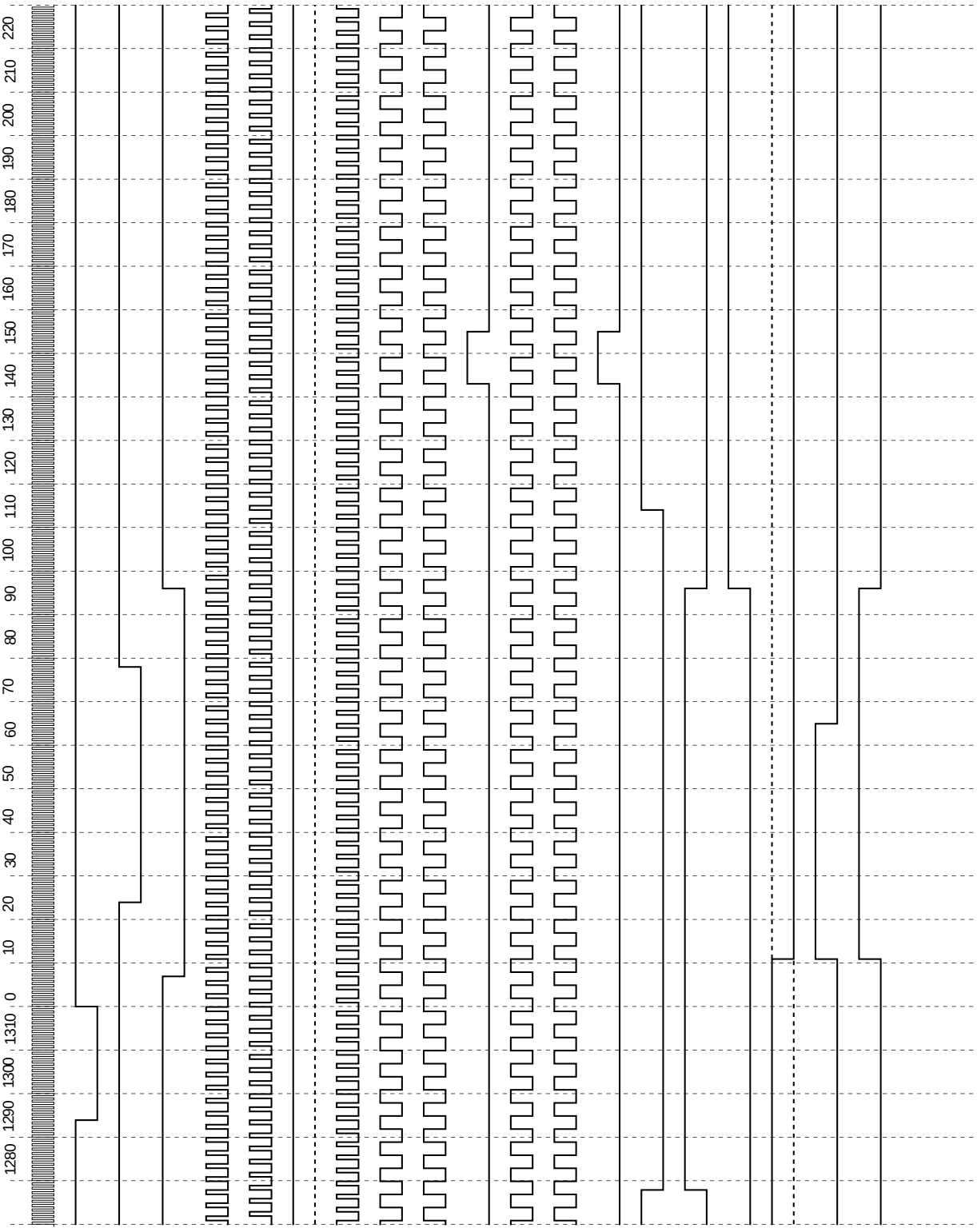
Note) Input pins in default state.

PAL+ -EVEN LINE Horizontal Direction Timing Chart



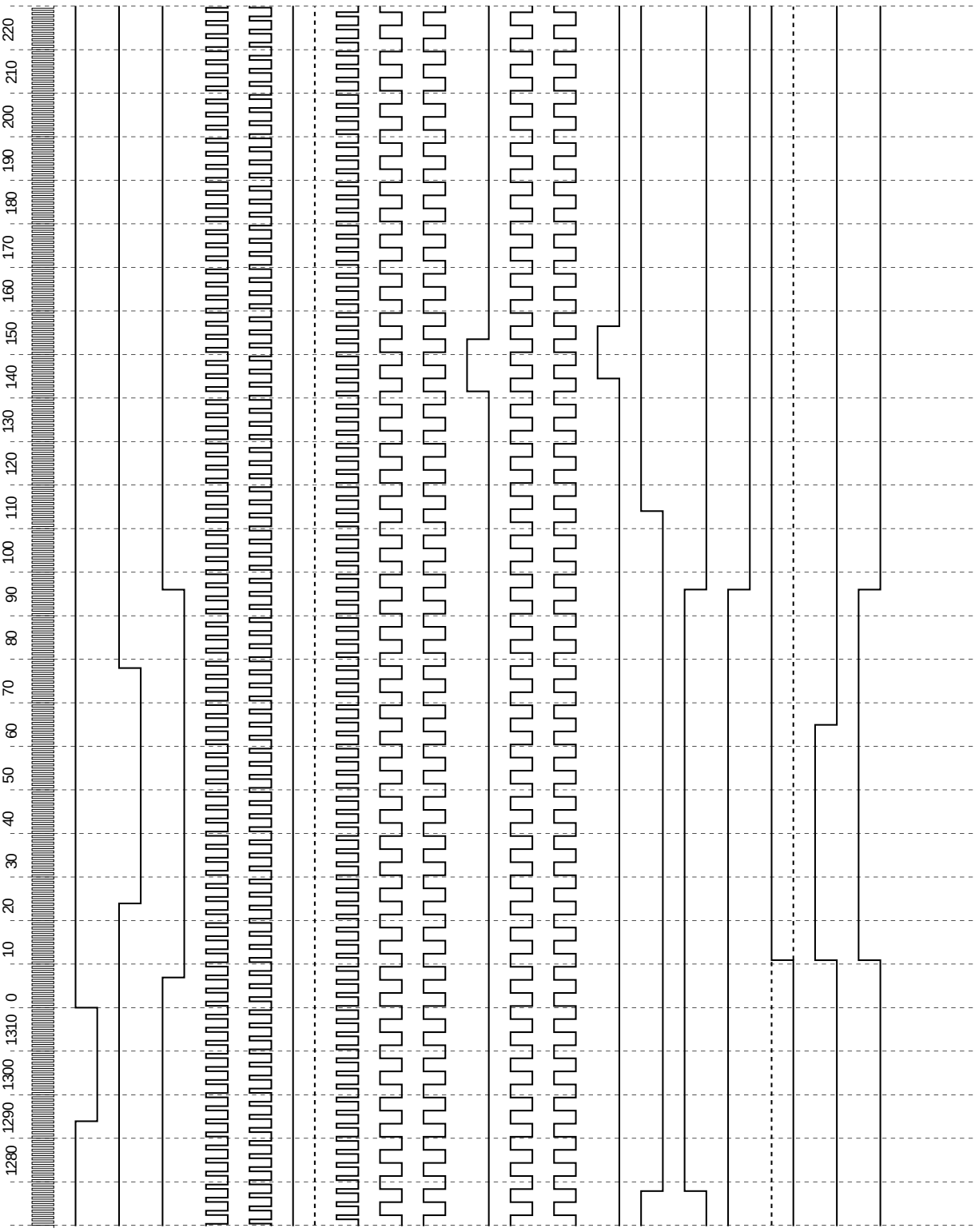
Note) Input pins in default state.

HD-ODD LINE **Horizontal Direction Timing Chart**



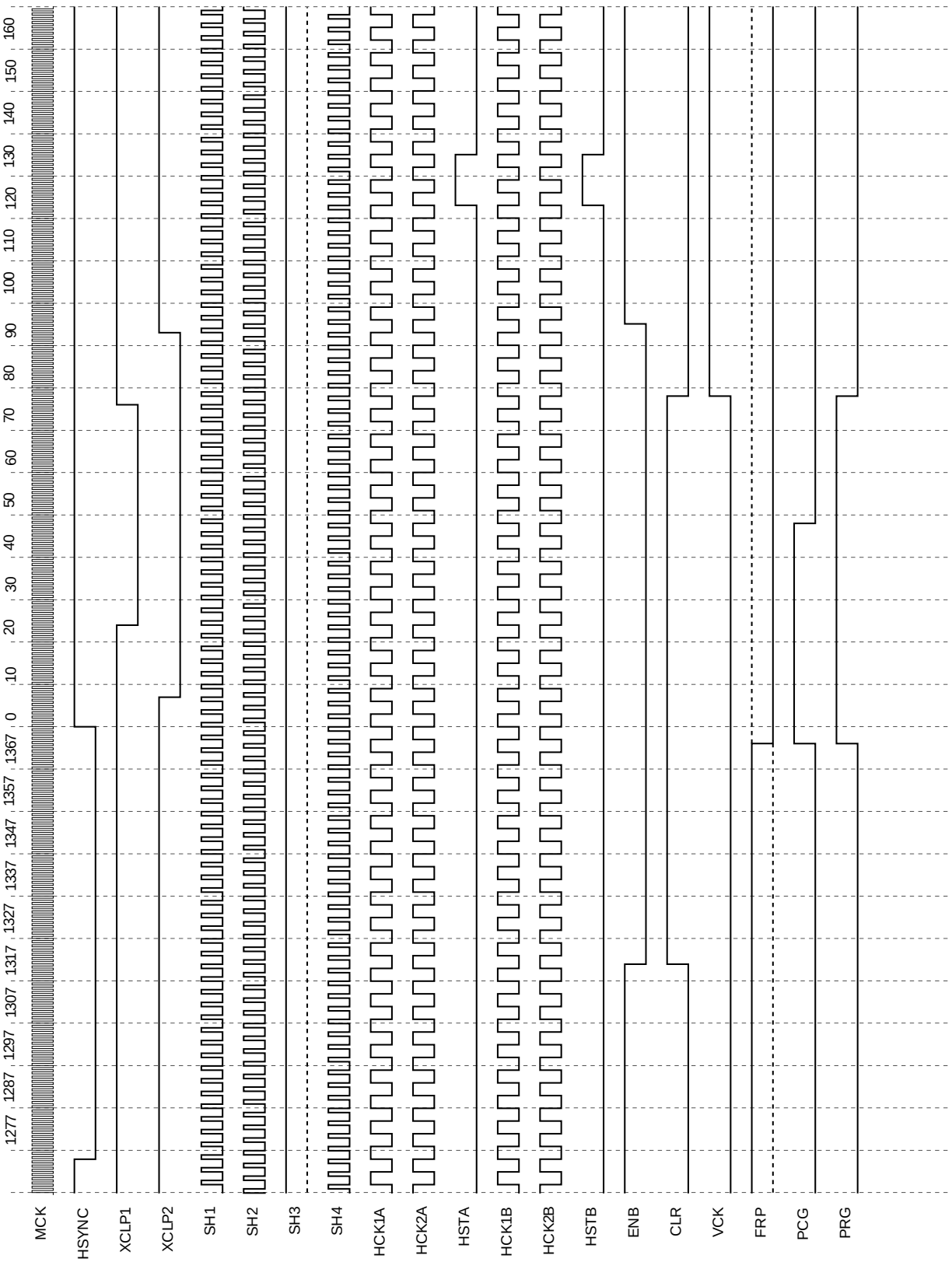
Note) Input pins in default state.

HD-EVEN LINE **Horizontal Direction Timing Chart**



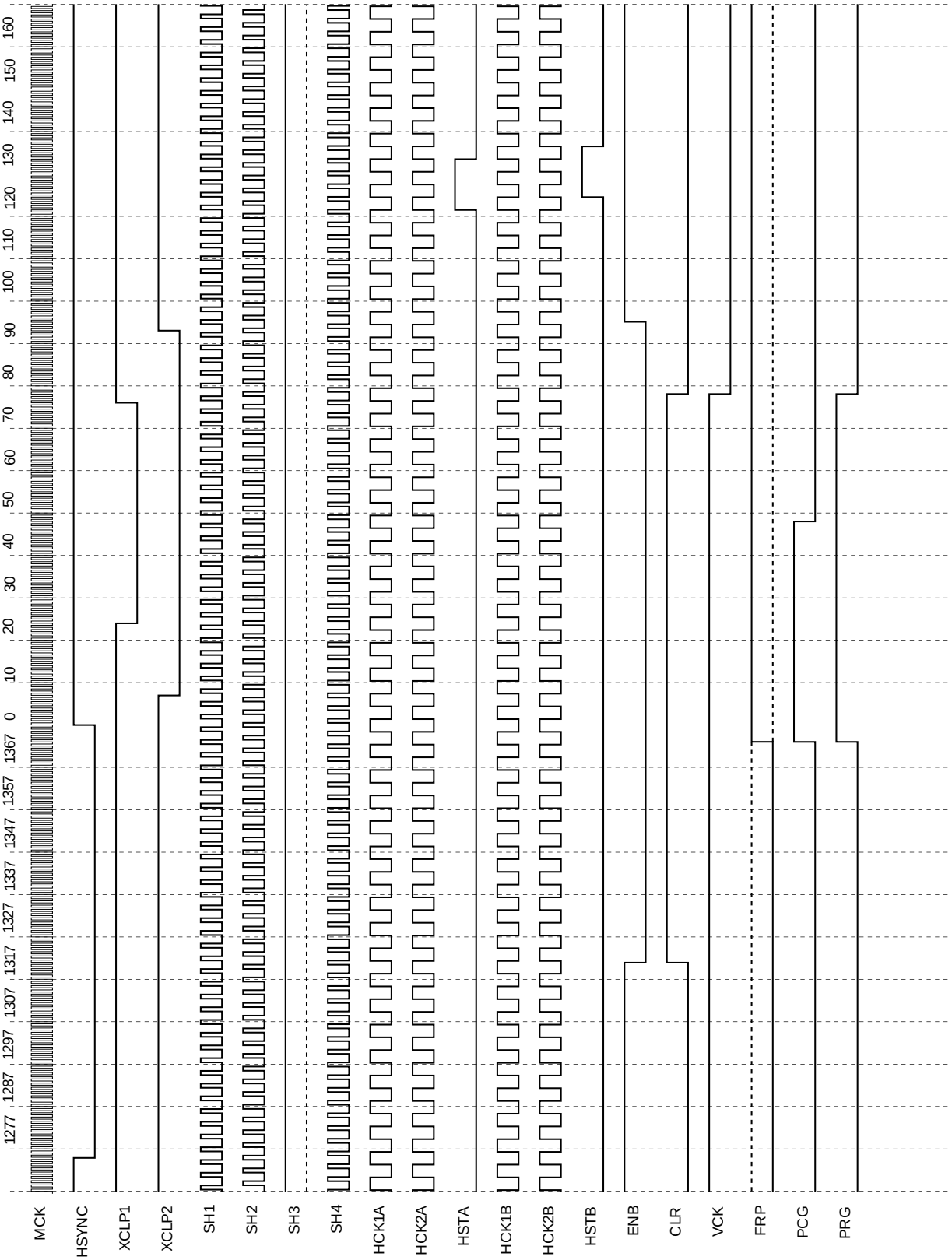
Note) Input pins in default state.

MNDC-ODD LINE Horizontal Direction Timing Chart

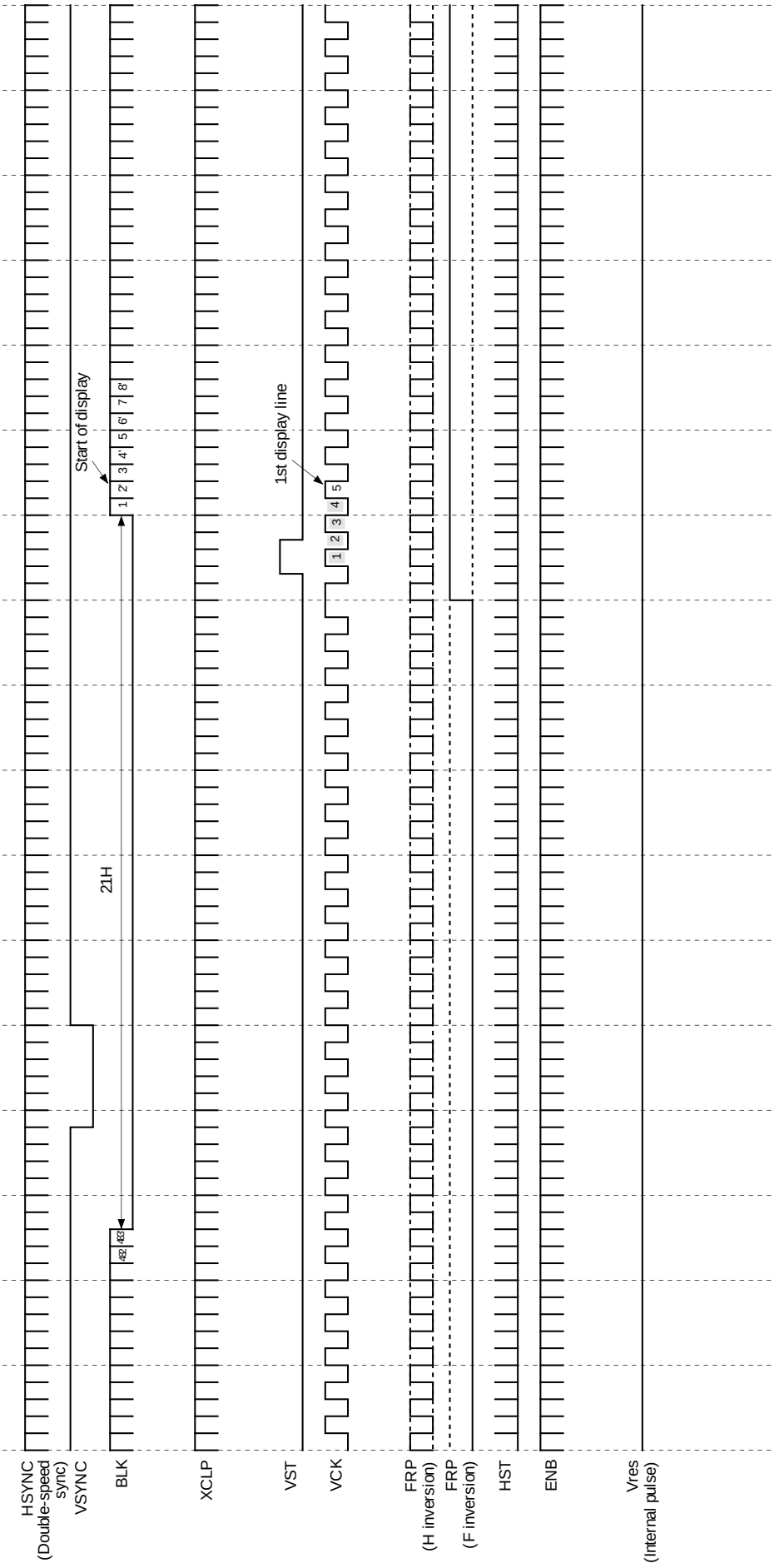


Note) Input pins in default state.

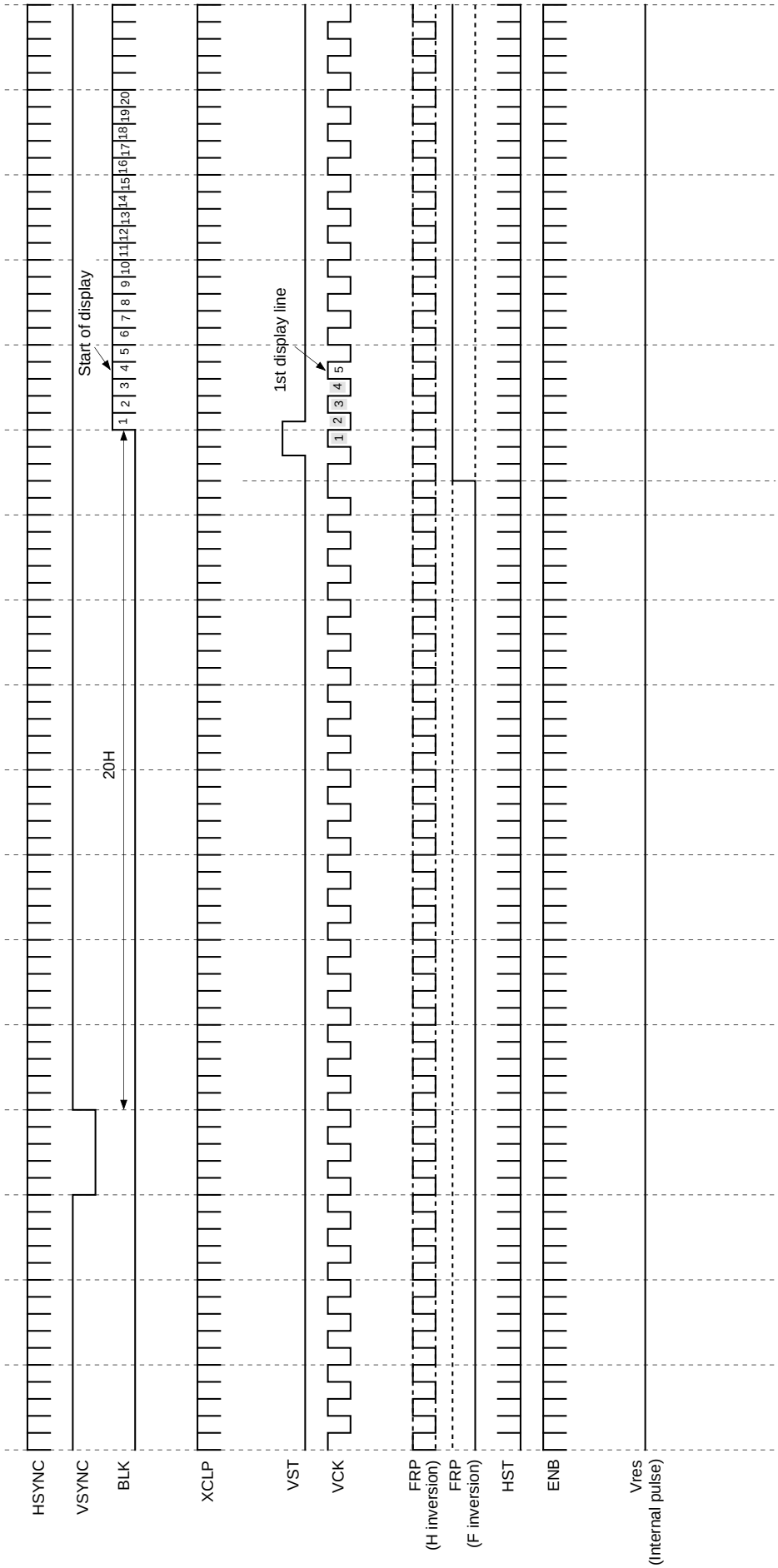
MNDC-EVEN LINE Horizontal Direction Timing Chart



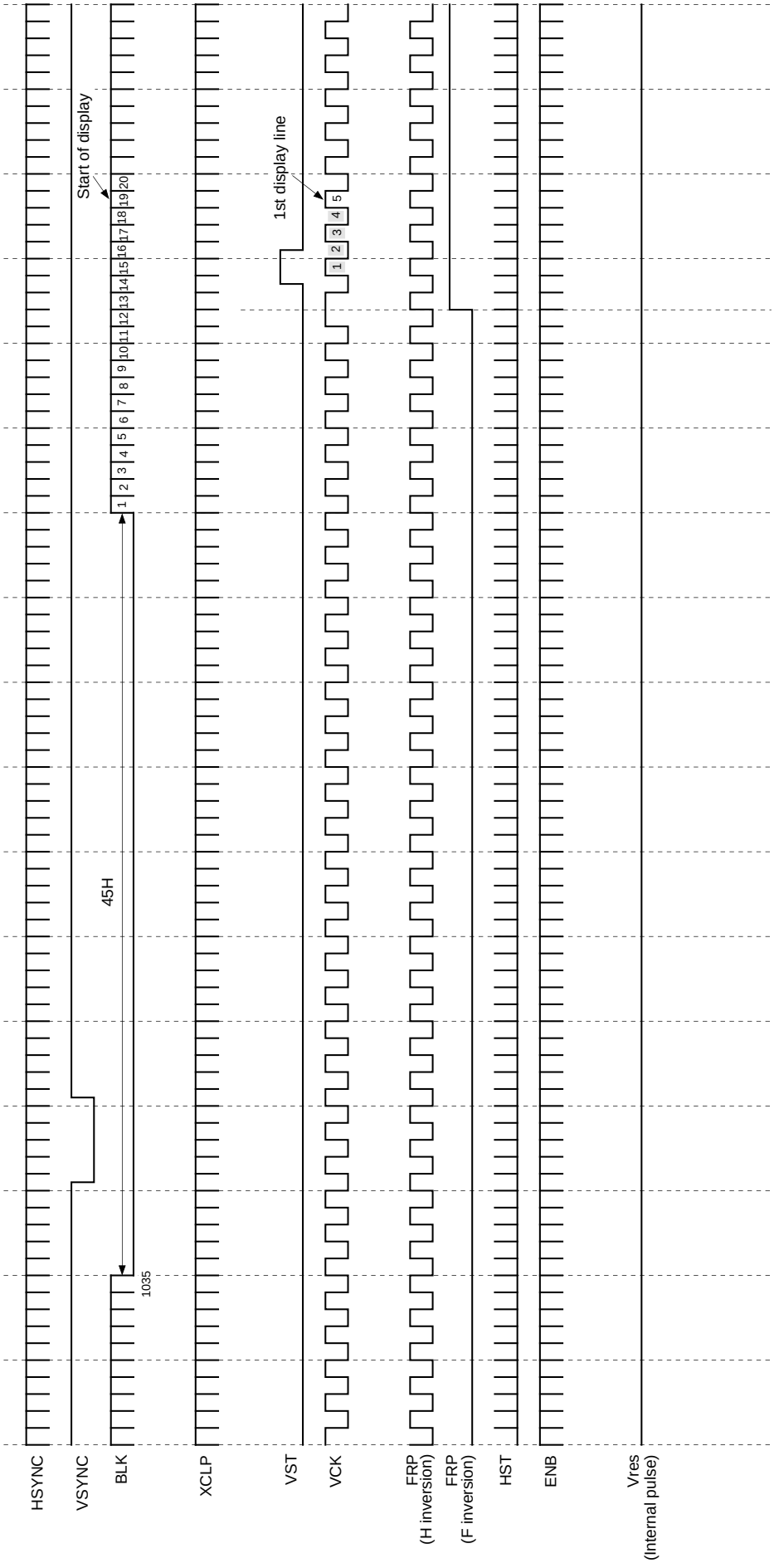
NTSC/NTSC WIDE/MNDC Vertical Direction Timing Chart



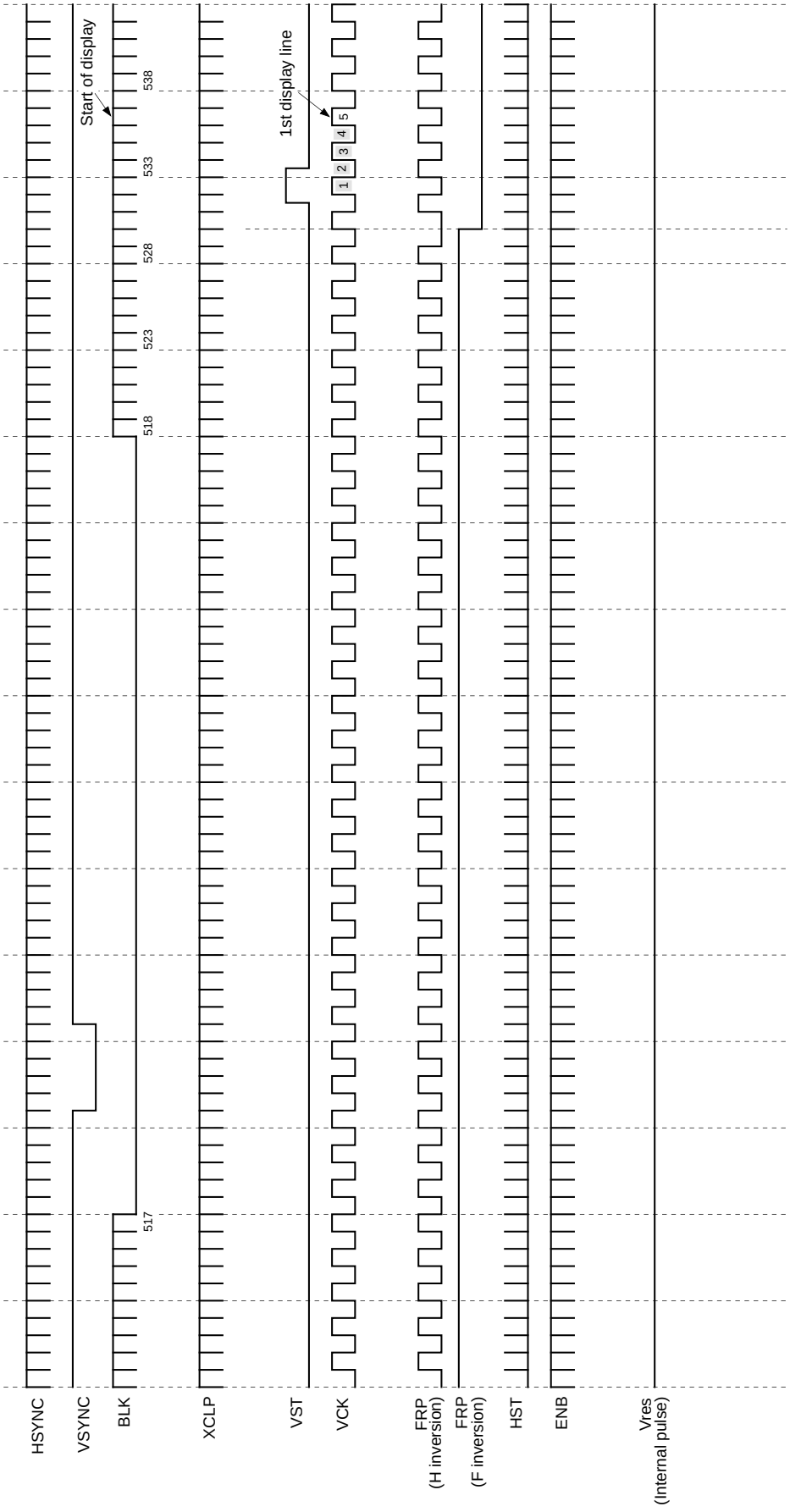
PAL/PAL+ Vertical Direction Timing Chart



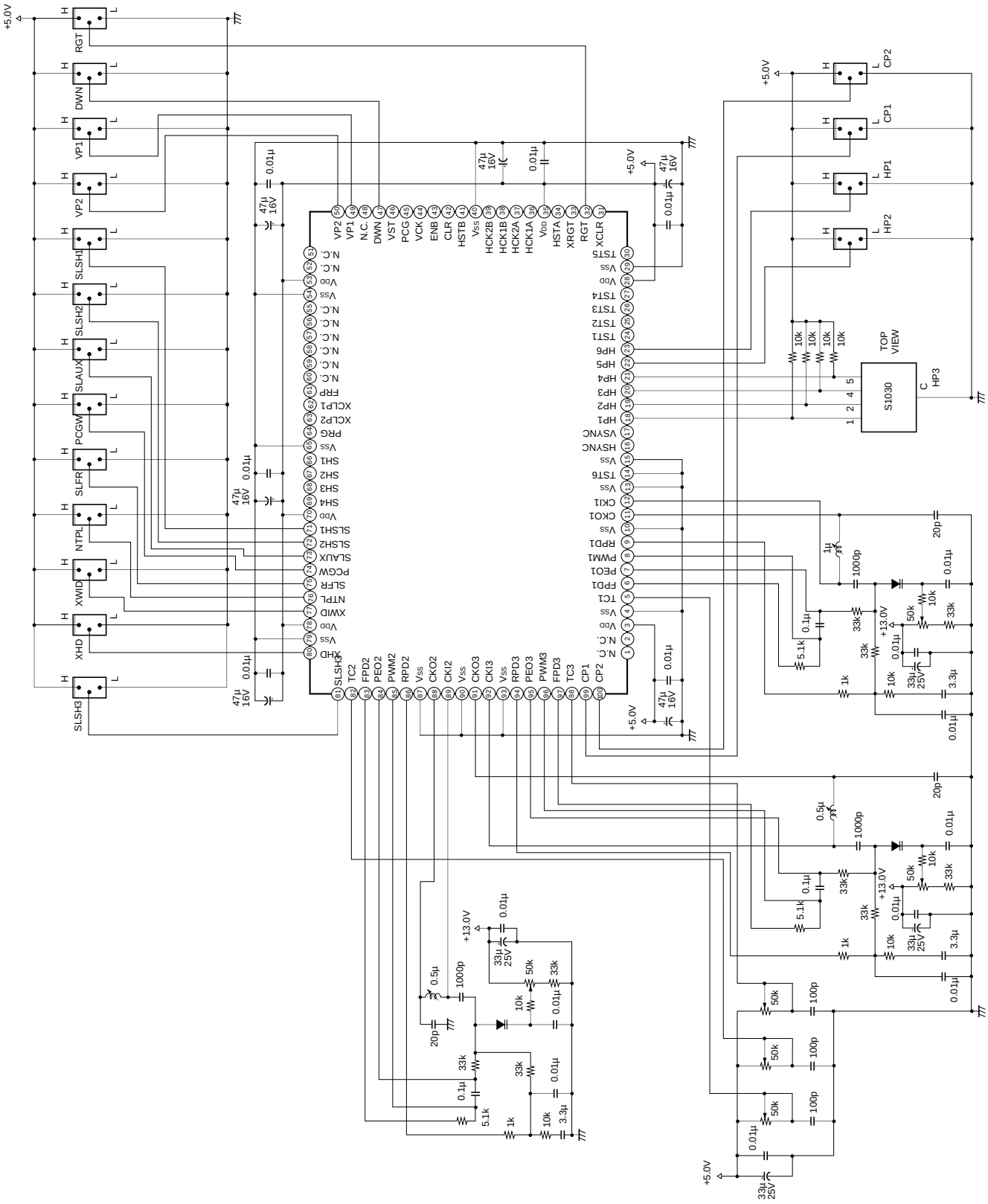
HD-ODD FIELD Vertical Direction Timing Chart



HD-EVEN FIELD Vertical Direction Timing Chart



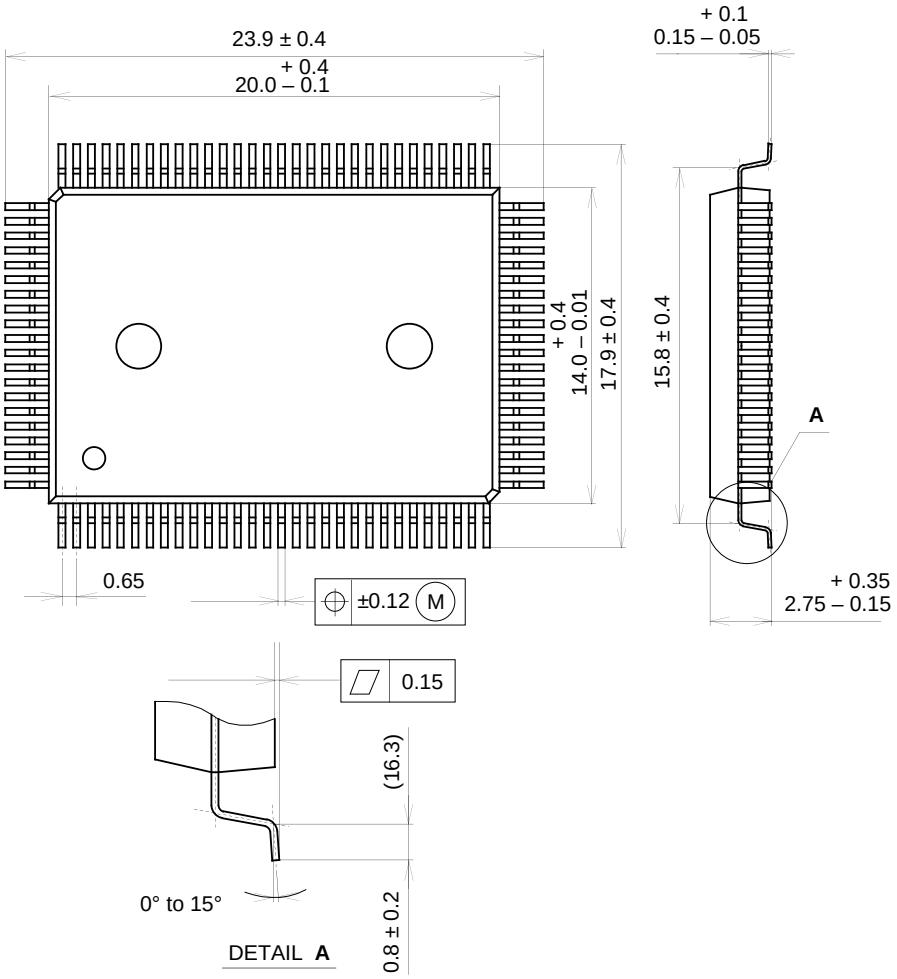
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	∗QFP100-P-1420-A
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g