SONY

CXD2443Q

Timing Generator for LCD Panels

Description

The CXD2443Q is a timing generator for the LCD panel LCX011 and LCX019 driver. This chip has a built-in serial interface circuit which allows various settings to be performed through external control from a microcomputer, etc.

Features

- Generates the LCD panel LCX011/LCX019 drive pulse
- Supports NTSC/PAL
  (PAL supported by scanning line conversion of video signal to 525H or pulse eliminate.)
- Supports WIDE mode (when driving the LCX011)
- Supports HD mode (when driving the LCX011)
- Supports up/down and/or right/left inversion
- Supports 3-panel projectors
- Generates timing signal of external sample-and-hold circuit
- Generates line inversion and field inversion signals
- AC drive of LCD panels during no signal
- Line double-speed display realized with a built-in double-speed controller (NTSC/PAL) (4:3 mode only)
  (Line memory µPD485505: NEC)

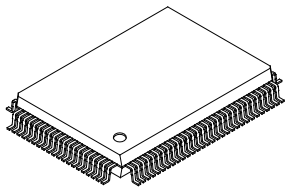
Applications

LCD projectors, etc.

Structure

Silicon CMOS IC

100 pin QFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

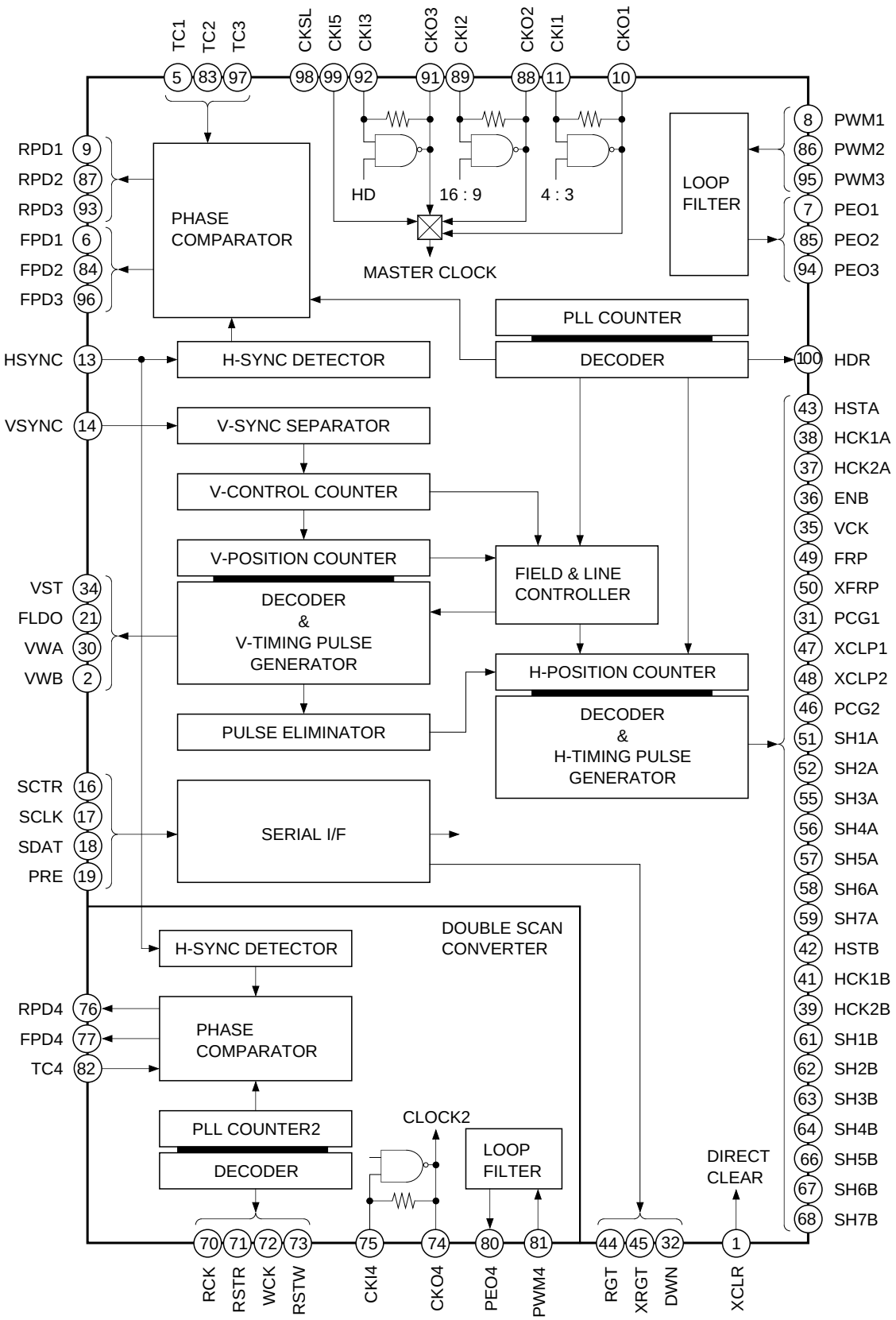
• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	–20 to +75	°C

E96X31-PS

Block Diagram



TEST: 12, 20, 22, 23, 24, 25, 26, 27, 33, 60, 69
V_{DD}: 3, 28, 53, 78
V_{SS}: 4, 15, 29, 40, 54, 65, 79, 90

Pin Description

Pin No.	Symbol	I/O	Description	Input pin for open status
1	XCLR	I	System clear (Low: All clear)	H
2	VWB	O	V window pulse B output	—
3	V_{DD}	—	Power supply	—
4	V_{SS}	—	GND	—
5	TC1	I/O	FPD1 output pulse width adjustment (NTSC/PAL 4:3)	—
6	FPD1	O	Phase comparator 1 output (NTSC/PAL 4:3)	—
7	PEO1	I/O	Loop filter integrator 1 output (NTSC/PAL 4:3)	—
8	PWM1	O	Loop filter integrator 1 input (NTSC/PAL 4:3)	—
9	RPD1	O	Phase comparator 1 output (NTSC/PAL 4:3)	—
10	CKO1	I/O	Oscillation cell 1 output (NTSC/PAL 4:3)	—
11	CKI1	I	Oscillation cell 1 input (NTSC/PAL 4:3)	—
12	TEST2	I	Test (Not connected.)	—
13	HSYNC	I	Horizontal sync signal input (Polarity set by serial data HPOL.)	—
14	VSYNC	I	Vertical sync signal input (Polarity set by serial data VPOL.)	—
15	V_{SS}	—	GND	—
16	SCTR	I	Chip select input (serial transfer block)	—
17	SCLK	I	Serial clock input (serial transfer block)	—
18	SDAT	I	Serial data input (serial transfer block)	—
19	PRE	I	Preset setting (Set to NTSC 4:3 mode when Low.)	H
20	TEST11	—	Test (Not connected.)	—
21	FLDO	O	Field discrimination signal output	—
22	TEST1	—	Test (Not connected.)	—
23	TEST3	—	Test (Not connected.)	—
24	TEST4	—	Test (Not connected.)	—
25	TEST5	—	Test (Not connected.)	—
26	TEST6	—	Test (Not connected.)	—
27	TEST7	—	Test (Connect to GND.)	—
28	V_{DD}	—	Power supply	—
29	V_{SS}	—	GND	—
30	VWA	O	V window pulse A output	—
31	PCG1	O	PCG1 pulse output (positive polarity)	—
32	DWN	O	Up/down inversion identification signal output (High: Down, Low: Up)	—
33	TEST8	—	Test (Not connected.)	—
34	VST	O	V start pulse output (positive polarity)	—
35	VCK	O	V clock pulse output	—

Pin No.	Symbol	I/O	Description	Input pin for open status
36	ENB	O	ENB pulse output (negative polarity)	—
37	HCK2A	O	H clock 2A pulse output	—
38	HCK1A	O	H clock 1A pulse output	—
39	HCK2B	O	H clock 2B pulse output	—
40	V_{SS}	—	GND	—
41	HCK1B	O	H clock 1B pulse output	—
42	HSTB	O	H start B pulse output (positive polarity)	—
43	HSTA	O	H start A pulse output (positive polarity)	—
44	RGT	O	Right/left inversion identification signal output (High: Right, Low: Left)	—
45	XRGT	O	Right/left inversion identification signal output (Low: Left, High: Right)	—
46	PCG2	O	PCG2 pulse output (positive polarity)	—
47	XCLP1	O	Pedestal clamp pulse 1 output (negative polarity)	—
48	XCLP2	O	Pedestal clamp pulse 2 output (negative polarity)	—
49	FRP	O	AC drive inversion timing output	—
50	XFRP	O	AC drive inversion timing output (reverse polarity of FRP)	—
51	SH1A	O	Sample-and-hold pulse 1A output (positive polarity)	—
52	SH2A	O	Sample-and-hold pulse 2A output (positive polarity)	—
53	V_{DD}	—	Power supply	—
54	V_{SS}	—	GND	—
55	SH3A	O	Sample-and-hold pulse 3A output (positive polarity)	—
56	SH4A	O	Sample-and-hold pulse 4A output (positive polarity)	—
57	SH5A	O	Sample-and-hold pulse 5A output (positive polarity)	—
58	SH6A	O	Sample-and-hold pulse 6A output (positive polarity)	—
59	SH7A	O	Sample-and-hold pulse 7A output (positive polarity)	—
60	TEST9	—	Test (Not connected.)	—
61	SH1B	O	Sample-and-hold pulse 1B output (positive polarity)	—
62	SH2B	O	Sample-and-hold pulse 2B output (positive polarity)	—
63	SH3B	O	Sample-and-hold pulse 3B output (positive polarity)	—
64	SH4B	O	Sample-and-hold pulse 4B output (positive polarity)	—
65	V_{SS}	—	GND	—
66	SH5B	O	Sample-and-hold pulse 5B output (positive polarity)	—
67	SH6B	O	Sample-and-hold pulse 6B output (positive polarity)	—
68	SH7B	O	Sample-and-hold pulse 7B output (positive polarity)	—
69	TEST10	—	Test (Not connected.)	—
70	RCK	O	Read clock output (for line buffer)	—

Pin No.	Symbol	I/O	Description	Input pin for open status
71	RSTR	O	Read reset output (for line buffer, negative polarity)	—
72	WCK	O	Write clock output (for line buffer)	—
73	RSTW	O	Write reset output (for line buffer, negative polarity)	—
74	CKO4	I/O	Oscillation cell 4 output (line double-speed controller)	—
75	CKI4	I	Oscillation cell 4 input (line double-speed controller)	—
76	RPD4	O	Phase comparator 4 output (line double-speed controller)	—
77	FPD4	O	Phase comparator 4 output (line double-speed controller)	—
78	V_{DD}	—	Power supply	—
79	V_{SS}	—	GND	—
80	PEO4	I/O	Loop filter integrator 4 output (line double-speed controller)	—
81	PWM4	O	Loop filter integrator 4 input (line double-speed controller)	—
82	TC4	I/O	FPD4 output pulse width adjustment (line double-speed controller)	—
83	TC2	I/O	FPD2 output pulse width adjustment (NTSC/PAL 16:9)	—
84	FPD2	O	Phase comparator 2 output (NTSC/PAL 16:9)	—
85	PEO2	I/O	Loop filter integrator 2 output (NTSC/PAL 16:9)	—
86	PWM2	O	Loop filter integrator 2 input (NTSC/PAL 16:9)	—
87	RPD2	O	Phase comparator 2 output (NTSC/PAL 16:9)	—
88	CKO2	I/O	Oscillation cell 2 output (NTSC/PAL 16:9)	—
89	CKI2	I	Oscillation cell 2 input (NTSC/PAL 16:9)	—
90	V_{SS}	—	GND	—
91	CKO3	I/O	Oscillation cell 3 output (HD)	—
92	CKI3	I	Oscillation cell 3 input (HD)	—
93	RPD3	O	Phase comparator 3 output (HD)	—
94	PEO3	I/O	Loop filter integrator 3 output (HD)	—
95	PWM3	O	Loop filter integrator 3 input (HD)	—
96	FPD3	O	Phase comparator 3 output (HD)	—
97	TC3	I/O	FPD3 output pulse width adjustment (HD)	—
98	CKSL	I	PLL system switching (High: Built-in PLL, Low: External PLL)	H
99	CKI5	I	External clock input (for external phase comparison)	—
100	HDR	O	Phase comparator output (for external phase comparison)	—

* H: Pull up, L: Pull down

Electrical Characteristics

1. DC characteristics

(V_{DD} = 5.0 ± 0.5V, V_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Supply voltage	V_{DD}		4.5	5.0	5.5	V	
Input, output voltages	V_I, Vo		Vss		V_{DD}	V	
Input voltage 1	V_{IH}	CMOS input	0.7V_{DD}			V	*1
	V_{IL}				0.3V_{DD}		
Input voltage 2	V_{t+}	TTL Schmitt trigger input	2.2			V	HSYNC, SCTR, VSYNC, SCLK, SDAT
	V_{t-}				0.8		
	$V_{t+} – V_{t-}$			0.4			
Input voltage 3	V_{t+}	CMOS Schmitt trigger input	0.8V_{DD}			V	TC1, TC2, TC3, TC4
	V_{t-}				0.2V_{DD}		
	$V_{t+} – V_{t-}$			0.6			
Output voltage 1	V_{OH}	I_{OH} = –2mA	V_{DD} – 0.8			V	*2
	V_{OL}	I_{OL} = 4mA			0.4		
Output voltage 2	V_{OH}	I_{OH} = –4mA	V_{DD} – 0.8			V	*3
	V_{OL}	I_{OL} = 8mA			0.4		
Output voltage 3	V_{OH}	I_{OH} = –4mA	V_{DD} – 0.8			V	RCK, WCK
	V_{OL}	I_{OL} = 6mA			0.4		
Output voltage 4	V_{OH}	I_{OH} = –3mA	V_{DD}/2			V	PEO1, PEO2, PEO3, PEO4, CKO4
	V_{OL}	I_{OL} = 3mA			V_{DD}/2		
Output voltage 5	V_{OH}	I_{OH} = –12mA	V_{DD}/2			V	CKO1, CKO2, CKO3
	V_{OL}	I_{OL} = 12mA			V_{DD}/2		
Input leak current	I_I	*4	–10		10	µA	*5
	I_{IL}	*6	–40	–100	–240		*7
	I_I	*8	–40		40		*9
Output leak current	I_{OZ}	*10	–40		40	µA	*11
Current consumption	I_{DD}	*12			110	mA	At a 30pF load*13

*1 XCLR, PRE, CKSL, CKI1, CKI2, CKI3, CKI4, CKI5, CKO1, CKO2, CKO3, CKO4, PWM1, PWM2, PWM3, PWM4, PEO1, PEO2, PEO3, PEO4

*2 HDR, ENB, PCG1, PCG2, XCLP1, XCLP2, VST, FRP, XFRP, VCK, DWN, FLDO, RGT, XRGT, VWA, VWB, RPD1, RPD2, RPD3, RPD4, FPD1, FPD2, FPD3, FPD4, TC1, TC2, TC3, TC4, RSTR, RSTW

*3 HSTA, HCK1A, HCK2A, SH1A, SH2A, SH3A, SH4A, SH5A, SH6A, SH7A, HSTB, HCK1B, HCK2B, SH1B, SH2B, SH3B, SH4B, SH5B, SH6B, SH7B

*4 Normal input pins (V_{IN} = V_{SS} or V_{DD})

*5 HSYNC, VSYNC, SCLK, SDAT, SCTR, CKI5

*6 Pins with pull-up resistors (V_{IN} = V_{SS})

*7 PRE, XCLR, CKSL

*8 Bidirectional pins (input status, V_{IN} = V_{SS} or V_{DD})

*9 CKO1, CKO2, CKO3, CKO4, PEO1, PEO2, PEO3, PEO4, TC1, TC2, TC3, TC4

*10 At high impedance (V_{IN} = V_{SS} or V_{DD})

*11 RPD1, RPD2, RPD3, RPD4, FPD1, FPD2, FPD3, FPD4

*12 fclk = 67MHz, V_{DD} = 5.5V

*13 HSTA, HSTB, HCK1A, HCK2A, HCK1B, HCK2B, SH1A, SH2A, SH3A, SH4A, SH5A, SH6A, SH7A, SH1B, SH2B, SH3B, SH4B, SH5B, SH6B, SH7B, VCK, ENB, FRP, PCG1, PCG2, XCLP1, XCLP2, RGT, DWN

2. AC characteristics (V_{DD} = 5.0 ± 0.5V, Vss = 0V, Topr = –20 to +75°C)

Item	Symbol	Applicable pins	Min.	Typ.	max.	Conditions	Unit
Clock input cycle		CKI1	21.3				ns
		CKI2	16.0				
		CKI3	15				
		CKI4	28.2				
		CKI5	15				
Output rise time	tr	All outputs			20	CL = 30pF	
Output fall time	tf	All outputs			20	CL = 30pF	
Cross-point time difference	Δt	*1	–10		10	CL = 30pF	
Output rise delay time	tpr	All outputs			15	CL = 30pF	
Output fall delay time	tpf	All outputs			15	CL = 30pF	
HCK1 Duty	$t_H/(t_H + t_L)$	HCK1A, HCK1B	48		52	CL = 30pF	%
HCK2 Duty	$t_L/(t_H + t_L)$	HCK2A, HCK2B	48		52	CL = 30pF	

*1 HCK1A, 2A HCK1B, 2B

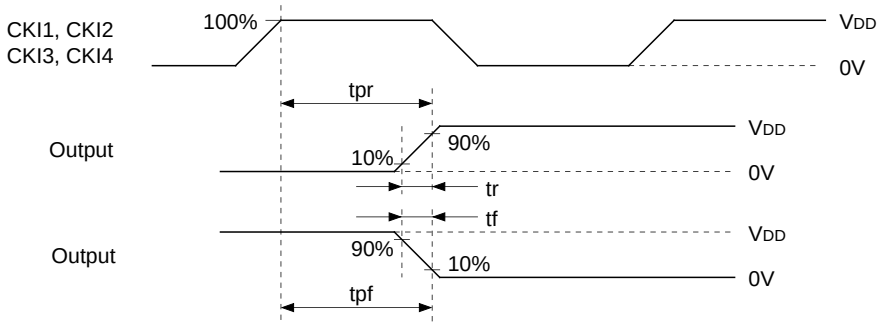
3. Serial transfer AC characteristics (V_{DD} = 5.0 ± 0.5V, Vss = 0V, Topr = –20 to +75°C)

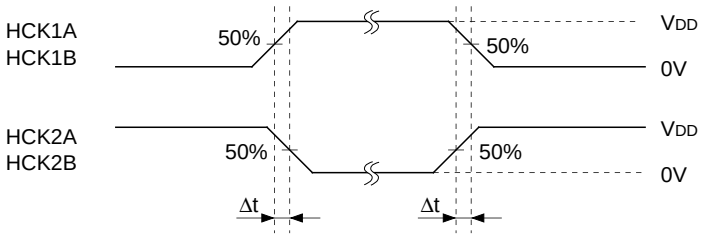
Symbol	Item	Min.	Typ.	Max.	Unit
ts0	SCTR setup time, activated by rise of SCLK	4T			ns
ts1	SDAT setup time, activated by rise of SCLK	2T			
th0	SCTR hold time, activated by rise of SCLK	4T			
th1	SDAT hold time, activated by rise of SCLK	2T			
tw1L	SCLK pulse width	2T			
tw1H	SCLK pulse width	2T			
tw2		5T			
tw3		5T			

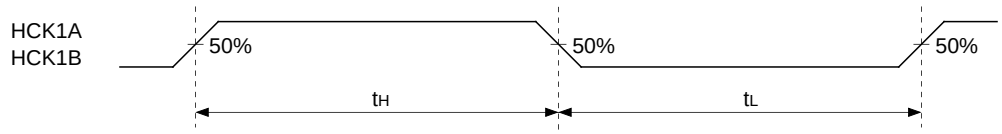
T: Master clock cycle (ns)

4. Timing definitions

AC characteristics

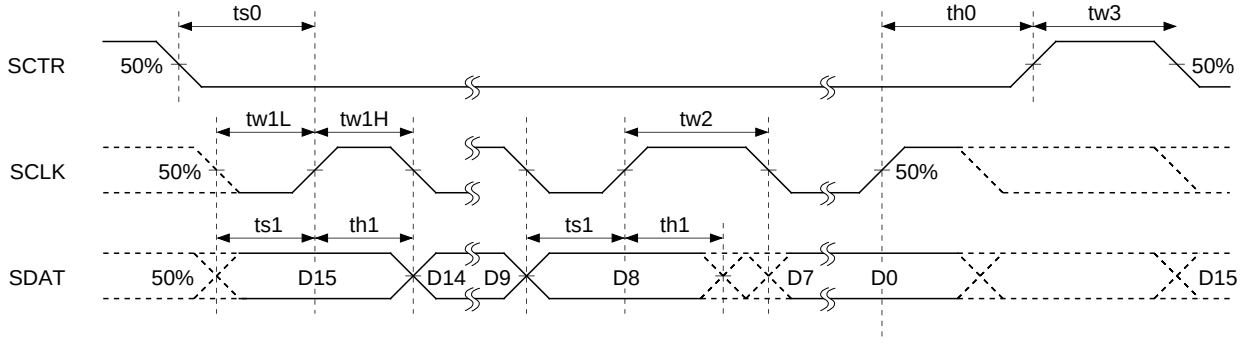






Note) HCK2 is the reverse phase of HCK1.

Serial transfer AC characteristics

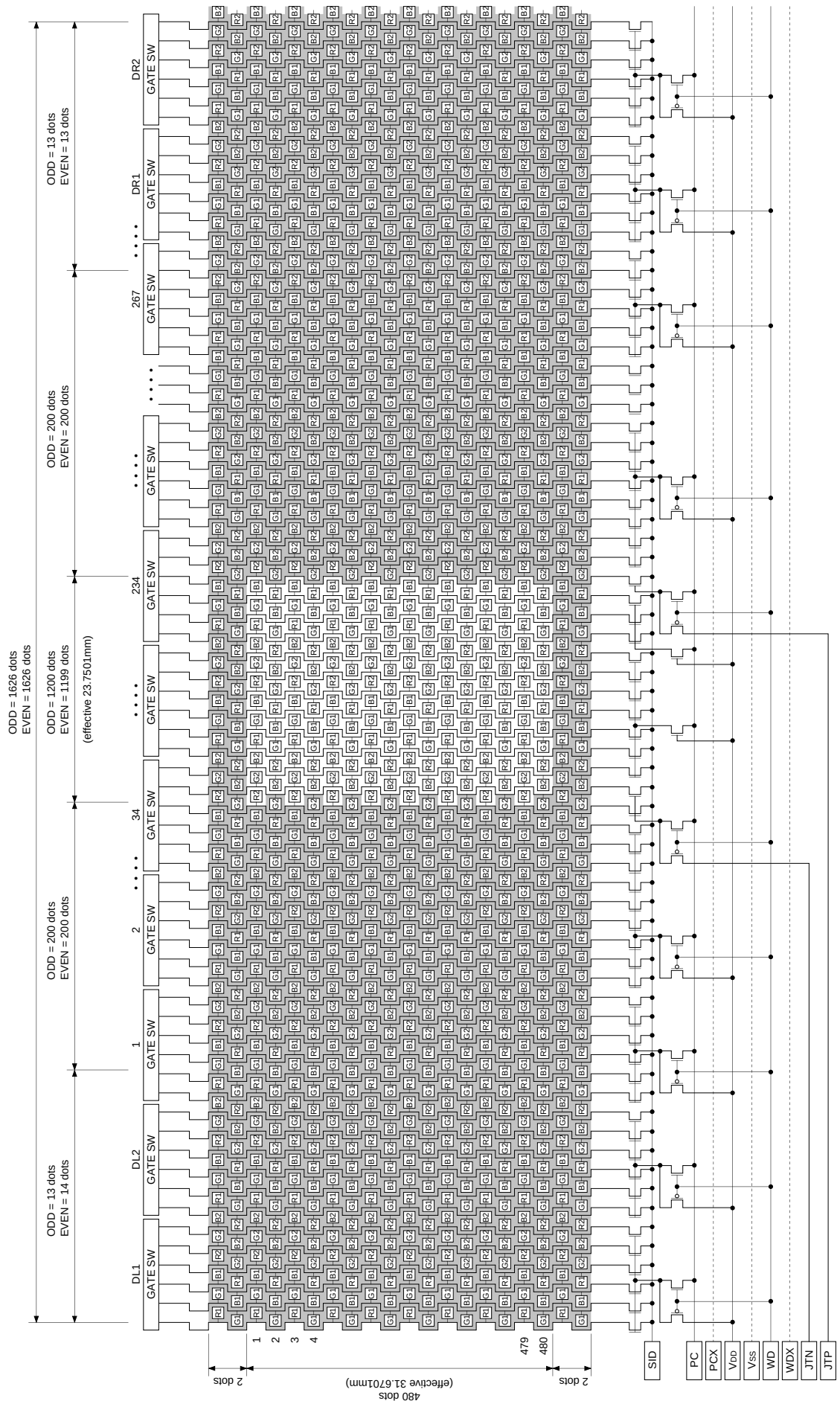


Note) See "Serial transfer timing" on P. 17 for the timing relationship between D15 to D0 and each pulse.

LCX011 Dot Arrangement (1) (4:3 display)

The dot arrangement is a delta arrangement. Also, the shaded region in the diagram is not displayed.

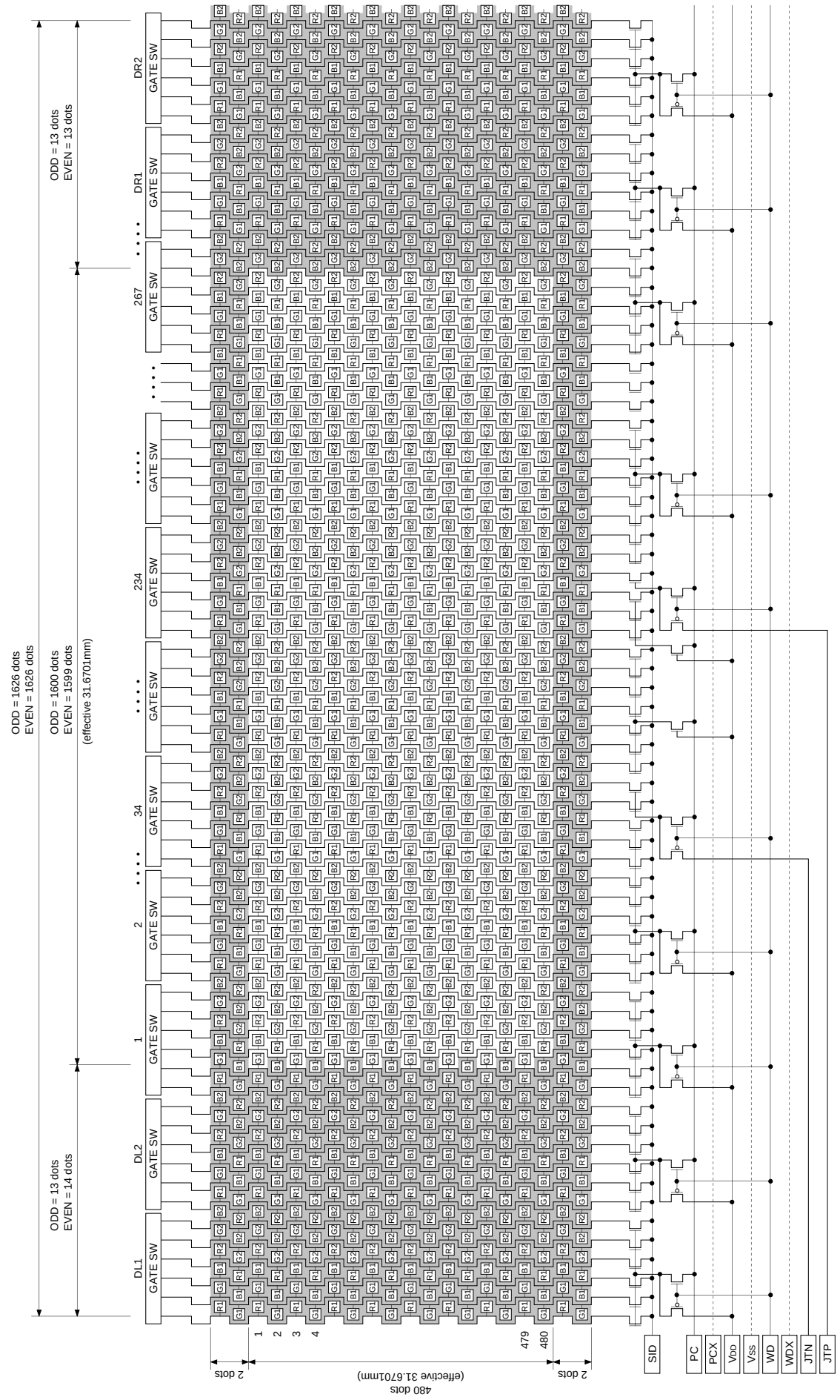
R1 corresponds to SIG2, G1 to SIG1, B1 to SIG3, R2 to SIG5, G2 to SIG4 and B2 to SIG6.



LCX011 Dot Arrangement (2) (16:9 display)

The dot arrangement is a delta arrangement. Also, the shaded region in the diagram is not displayed.

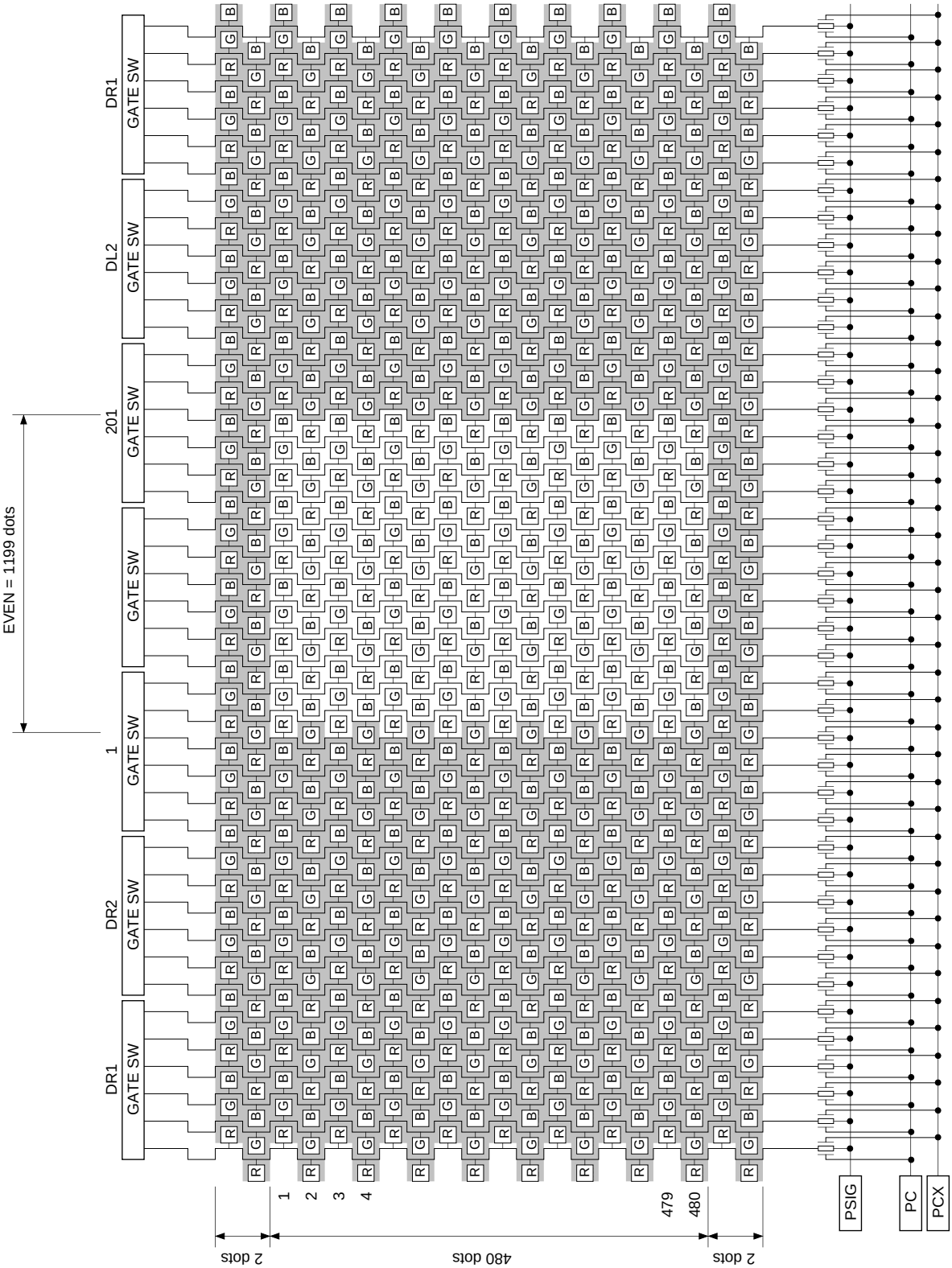
R1 corresponds to SIG2, G1 to SIG1, B1 to SIG3, R2 to SIG5, G2 to SIG4 and B2 to SIG6.



LCX019 Dot Arrangement

The dot arrangement is a delta arrangement. Also, the shaded region in the diagram is not displayed.

R1 corresponds to SIG2, G1 to SIG1, B1 to SIG3, R2 to SIG5, G2 to SIG4 and B2 to SIG6.



Input Signal Protocol

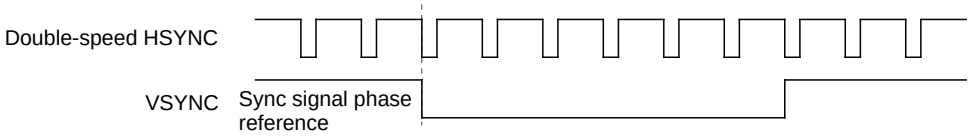
1. Horizontal sync signal

- A double-speed HSYNC or standard HSYNC (or CSYNC) should be input for NTSC and PAL display modes. Double-speed HSYNC and standard HSYNC input switching is set by the serial data (SNSL).
  Note) The double-speed HSYNC should have a cycle and width 1/2 that of the standard HSYNC.
- The signal obtained by cutting off only the bottom of the ternary SYNC should be input for HD display mode.
- The input sync signal polarity is not fixed, and is set by the serial data (HPOL).
- When using the built-in line double-speed controller, set serial data SNSL to Low. The built-in line double-speed controller supports only the standard HSYNC (or CSYNC).

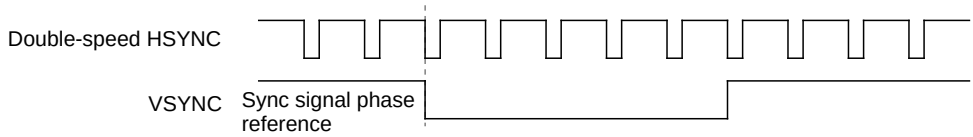
2. Vertical sync signal

- A normal-speed VSYNC (or CSYNC) should be input for NTSC and PAL display modes.
- A VSYNC that has been sync separated by SYNC SEP. should be input for HD display mode.
- The input sync signal polarity is not fixed, and is set by the serial data (VPOL).
- The phase relationship between HSYNC and VSYNC is specified as follows for the CXD2443Q.

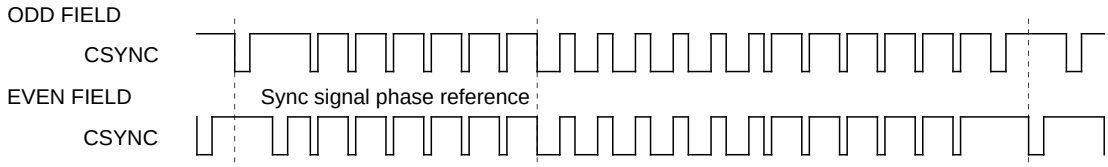
(1) Double-speed NTSC



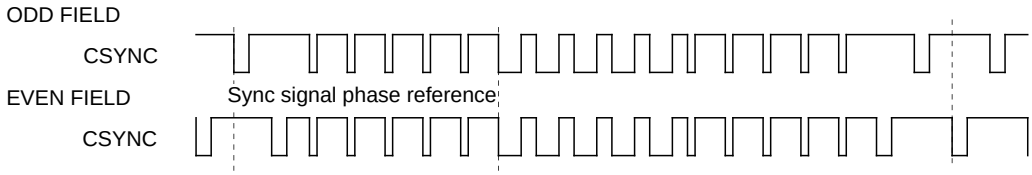
(2) Double-speed PAL



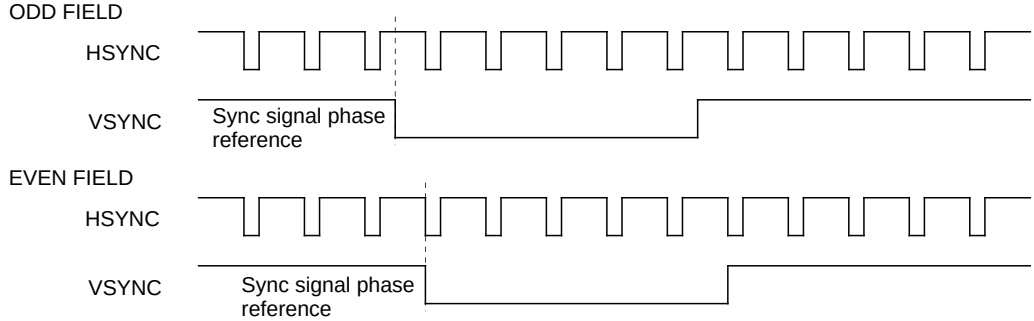
(3) NTSC (CSYNC input)



(4) PAL (CSYNC input)



(5) HD



Description of Operation

Clock input

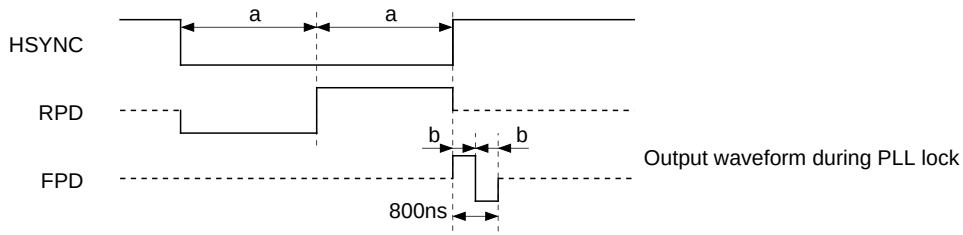
The CXD2443Q supports two types of PLL circuits.
PLL switching is performed by CKSL (Pin 98). (High: Built-in PLL, Low: External PLL)
Note) The built-in line double-speed controller PLL is supported only by the built-in PLL.

(1) Built-in PLL (CKI1, CKI2, CKI3, CKI4)

A PLL circuit is comprised by the built-in phase comparator and an external VCO circuit. There are four clock inputs which support the following modes.

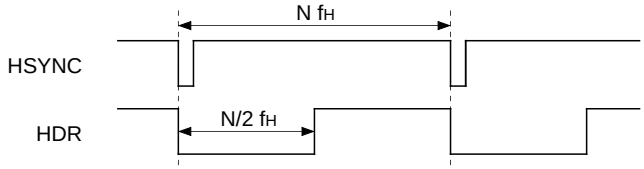
CKI1: NTSC/PAL 4:3 CKI2: NTSC/PAL 16:9
CKI3: HD CKI4: For built-in line double-speed controller

The PLL lock for this system is adjusted by setting the RPD and FPD transition points so that they fall at the center of the windows as shown in the diagram below. (See the Application Circuit.)



(2) External PLL (CKI5)

The CKI5 pin is the clock input pin when using an external PLL IC. The 1/N frequency divider output is output from the HDR pin (frequency division ratio N/2) for the PLL IC. Set CKSL (Pin 98) to Low to switch to the external PLL.



AC driving of LCD panels for no signal

The following measures have been adopted to allow AC driving of LCD panels even when there is no signal.

- **Horizontal direction pulse**

  The PLL is set to free running status. The frequency of the horizontal direction pulse at this time is dependent on the PLL free running frequency.

- **Vertical direction pulse**

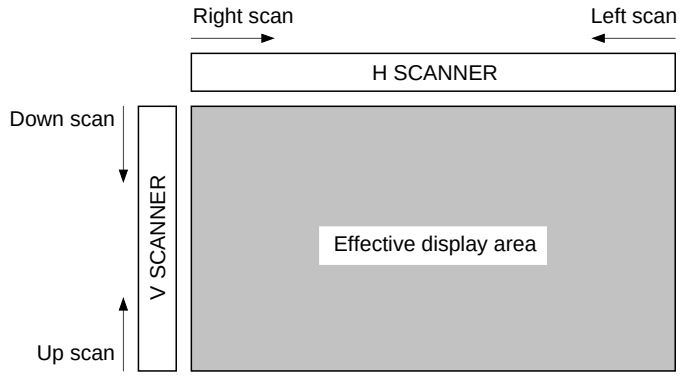
  The number of lines is counted by an internal counter and the vertical direction pulses (VST, FRP) are output at a specified cycle. For the CXD2443Q, no signal (free running) status is judged if there is no VSYNC input for longer than the following (free running detection) periods.

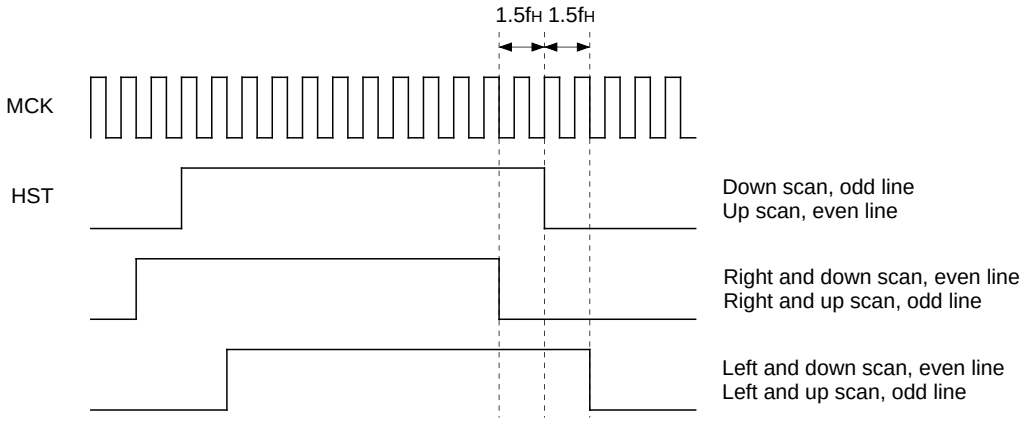
Mode	V cycle for no signal	Free running detection
NTSC	544H (272H)	1024H (512H)
PAL	640H (320H)	
HD	576H	

Note) Numbers in parentheses are for when using the built-in line double-speed controller.

Right/left and/or up/down inversion

In delta arrangement LCD panels, the same signal lines are separated by 1.5 dots for each horizontal line. Therefore, a 1.5 dot offset is added between lines to the LCD's horizontal direction start pulses HST and HCK and sample-and-hold pulse (SH).
When driving an LCD panel with right and left inversed, the dot arrangement is asymmetrical so an offset is attached to HST, HCK and SH. When driving with up and down inversed, the relationship between the panel's odd and even line offsets is reversed.

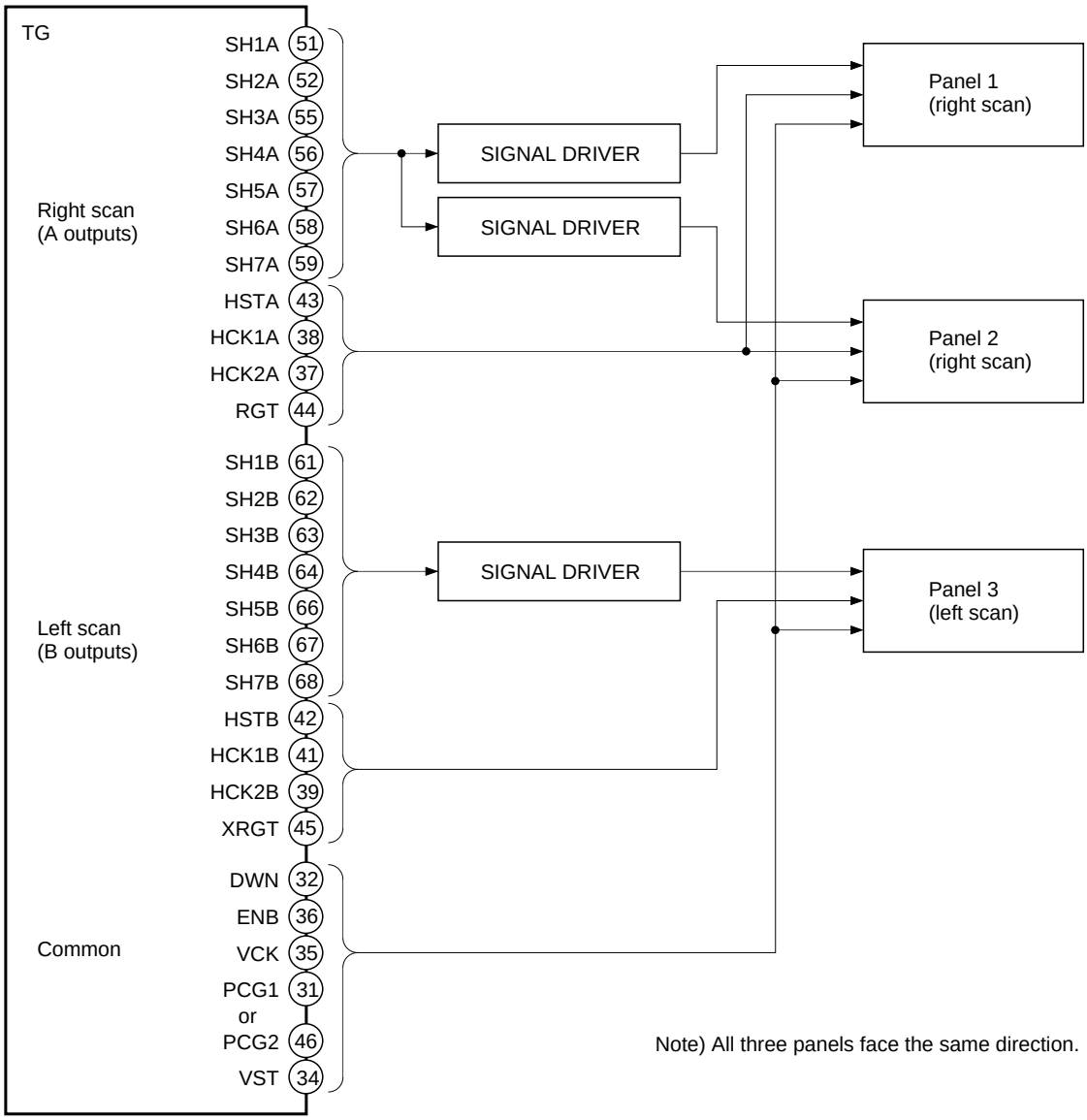




When using three LCD panels

B outputs (HSTB, HCK1B, HCK2B, SH1B to 7B) are provided for driving three LCD panels with and without right/left inversion at the same time. These B outputs are the right/left inversed timings of the A outputs (HSTA, HCK1A, HCK2A, SH1A to 7A).
XRGT (RGT inversed output) is also provided for right/left inversion scanning.

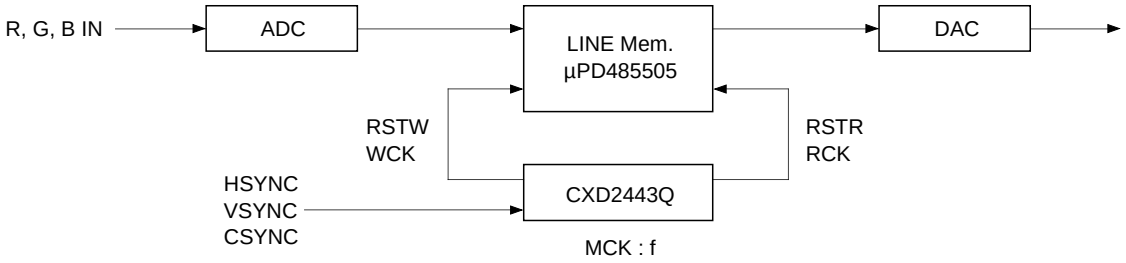
Application circuit (driving three LCD panels)



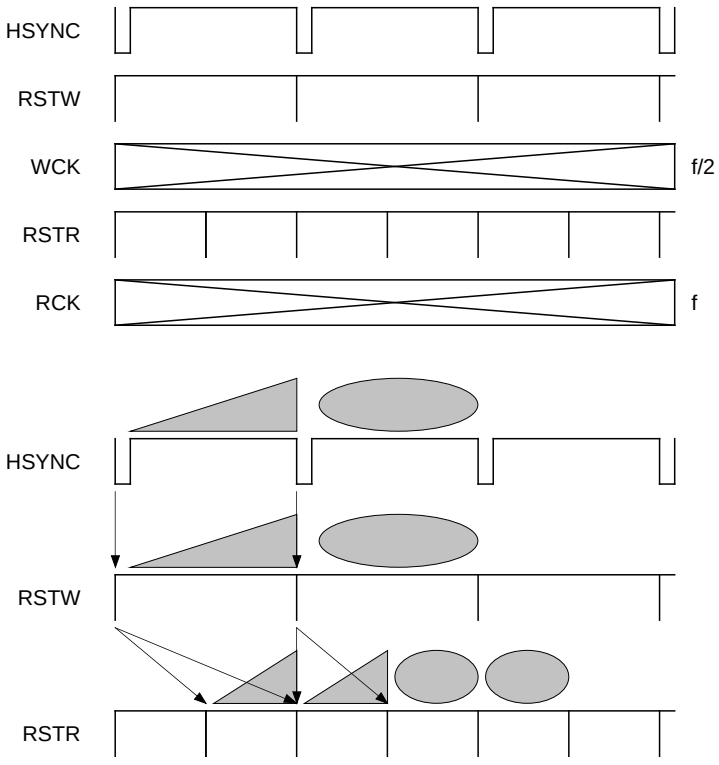
Note) All three panels face the same direction.

Built-in line double-speed controller

This controller is designed to use the µPD485505 (NEC/high-speed line buffer) as the system line memory IC, and generates the double-speed processing pulses RSTW (reset write), WCK (write clock), RSTR (reset read) and RCK (read clock).
Operation is as follows. Write operation is started at the RSTW timing, and this memory information is read twice at double speed at the RSTR timing which is delayed by 1/2H and 1H from the RSTW timing. The write and read clock frequencies at this time are generated by the built-in PLL (CKI4).
See the specifications for a detailed description of µPD485505 operation.



Double-speed display system block



Double-speed display timing

Note) See the timing charts for details.

XCLR pin

The CXD2443Q should be forcibly reset during power on in order to initialize the serial transfer block and other internal circuits.

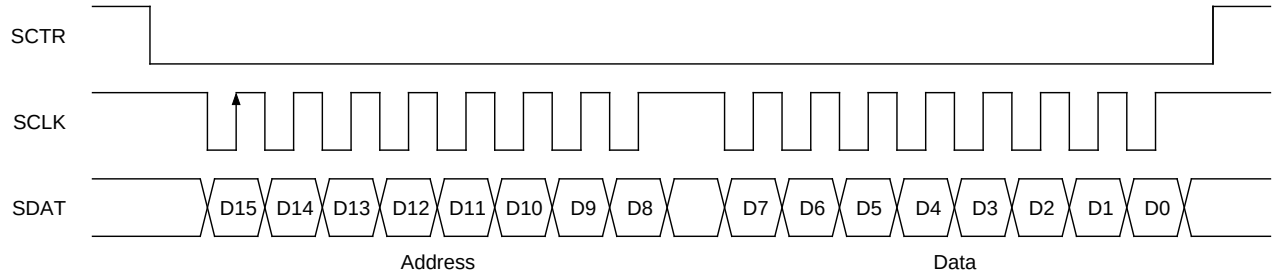
Serial transfer operation

1. Control method

The CXD2443Q operation timing is controlled by serial data.

The control data is comprised of an 8-bit address and 8-bit data, and the individual data is fetched at the rise of SCLK. This fetching operation starts from the fall of SCTR and is completed at the next rise of SCTR.

Serial transfer timing



2. Control data

When using the CXD2443Q, set the control data corresponding to each signal source according to the formats in the table below.

Address								Data								Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	(A) H-POSITION
0	0	0	0	0	0	0	1	—	—	—	—	VP4	VP3	VP2	VP1	(B) V-POSITION
0	0	0	0	0	0	1	0	—	—	—	—	SLSH4	SLSH3	SLSH2	SLSH1	(C) SH-POSITION
0	0	0	0	0	0	1	1	—	—	—	—	—	—	CP2	CP1	(D) XCLP-POSITION
0	0	0	0	0	1	0	0	—	—	—	—	—	—	PCGW2	PCGW1	(E) PCG-POSITION
0	0	0	0	0	1	0	1	—	—	—	—	—	—	VM9J	VM8J	(F) VWA-POSITION (VWA pulse)
0	0	0	0	0	1	1	0	VM7J	VM6J	VM5J	VM4J	VM3J	VM2J	VM1J	VM0J	
0	0	0	0	0	1	1	1	—	—	—	—	—	—	VM9K	VM8K	
0	0	0	0	1	0	0	0	VM7K	VM6K	VM5K	VM4K	VM3K	VM2K	VM1K	VM0K	
0	0	0	0	1	0	0	1	—	—	—	—	—	—	TEST1	SLBA	(G) Double-speed setting
0	0	0	0	1	0	1	0	—	—	—	—	—	—	MA	TEST2	(H) Double-speed PAL pulse eliminate
0	0	0	0	1	0	1	1	—	—	—	—	—	—	DWN	RGT	(I) Right/left and/or up/down inversion
0	0	0	0	1	1	0	0	—	—	TEST4	TEST3	SL3B	VPOL	HPOL	SLFR	(J) Various settings
0	0	0	0	1	1	0	1	—	—	—	—	—	—	SLVWB	SLEG	
0	0	0	0	1	1	1	0	—	—	—	—	SNSL	XHD	XWID	NT-PAL	(K) Mode settings

Note) 1. Set "High" as the TEST1, TEST2, TEST3 and TEST4 data.

2. "—" indicates not set.

Serial settings during power on

The CXD2443Q should be forcibly reset during power on using the XCLR pin. After being forcibly reset, the master clock for the CXD2443Q is supplied from CKI3. The initial serial data after power on is loaded to the CXD2443Q using the clock from CKI3.

Serial settings during PLL free running

When the PLL is in free running status, the serial clock cycle (F ns) may be less than F ≥ 2T with respect to the master clock cycle (T ns). Take care that the serial clock cycle setting is such that F ≥ 2T during PLL free running.

Each control data is described in detail below.

(A) H-POSITION
(HP1, HP2, HP3, HP4, HP5, HP6, HP7, HP8)

These bits set the horizontal display start position. The minimum adjustment width is 1 dot, and adjustment of up to ±128 dots is possible with respect to the design center value. (data: 8 bits)

	HP1	HP2	HP3	HP4	HP5	HP6	HP7	HP8
Design center value	L	L	L	L	L	L	L	H

MODE	Variable time (±128f_H)
NTSC (4:3)	±2.8µs
NTSC (16:9)	±2.1µs
PAL (4:3)	±2.7µs
PAL (16:9)	±2.0µs
HD	±1.9µs

(B) V-POSITION
(VP1, VP2, VP3, VP4)

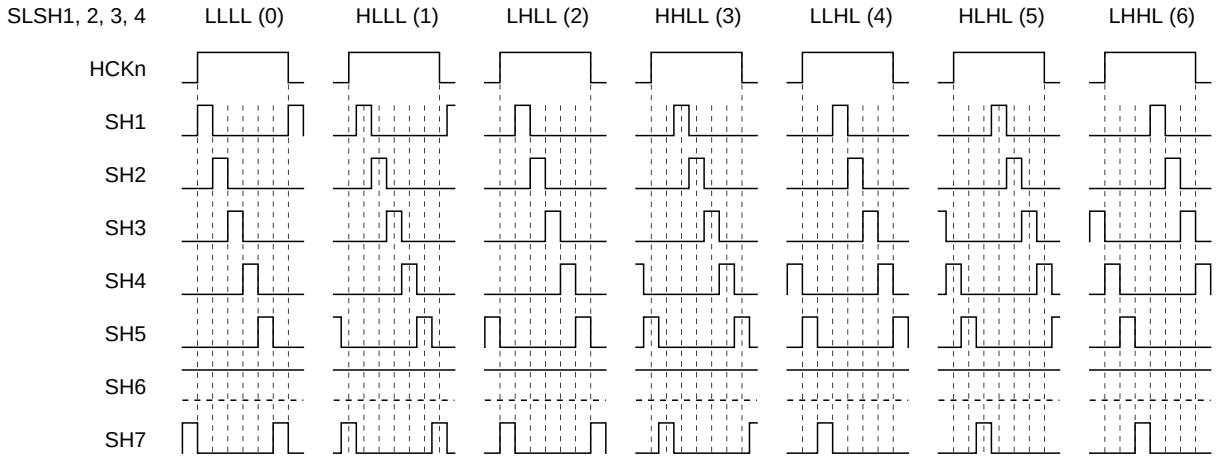
These bits set the vertical display start position. The minimum adjustment width is 1H, and adjustment of up to ±8H is possible with respect to the design center value. (data: 4 bits)

	VP1	VP2	VP3	VP4
Design center value	L	L	L	H

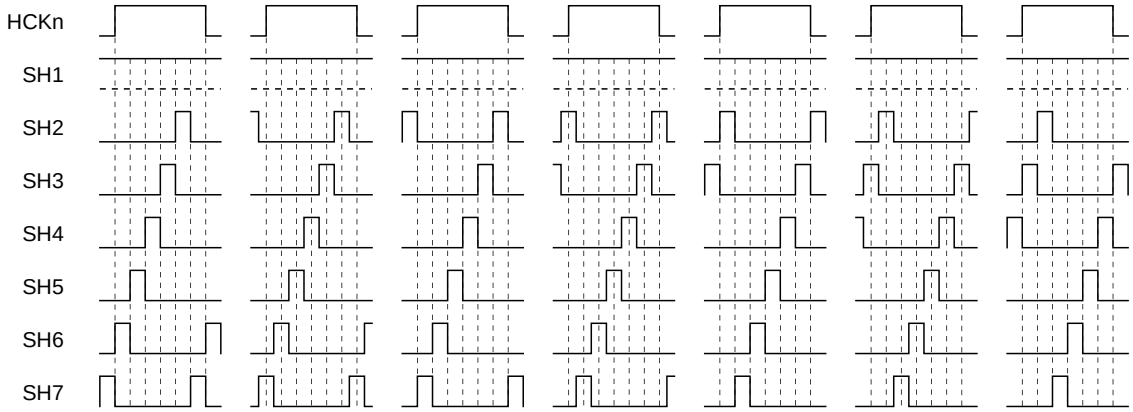
(C) SH-POSITION
(SLSH1, SLSH2, SLSH3, SLSH4)

These bits control the phase relationship between HCK1, HCK2 and SH1, 2, 3, 4, 5, 6 and 7. The minimum adjustment width is 0.5 dots, and adjustment of up to 6 dots is possible. (data: 4 bits)

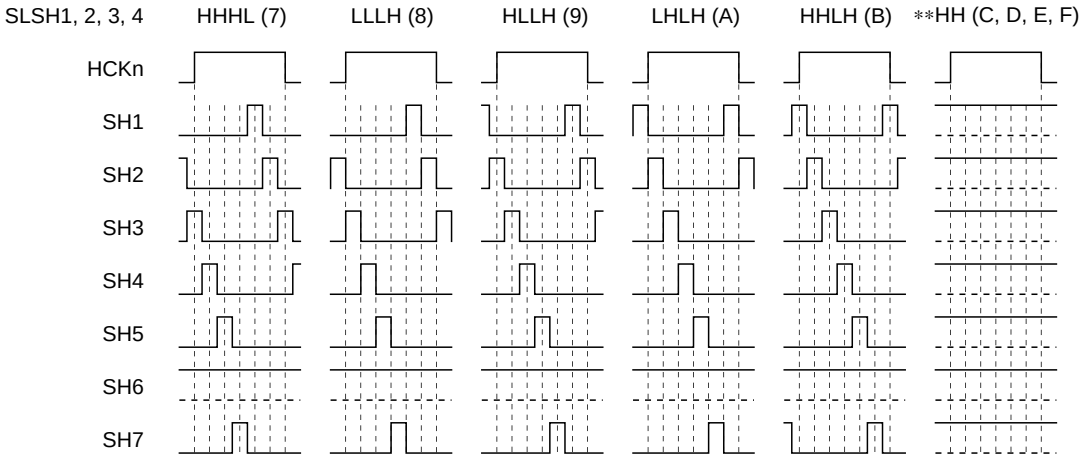
RGT = High: A output
RGT = Low: B output



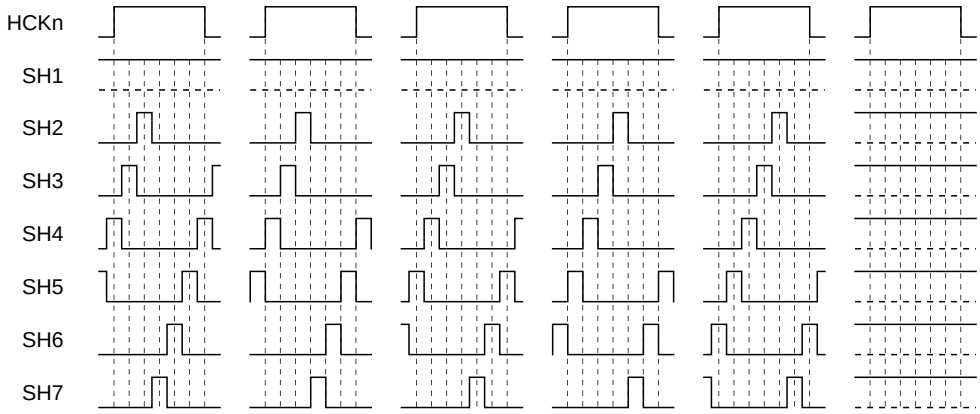
RGT = Low: A output
RGT = High: B output



RGT = High: A output
RGT = Low: B output

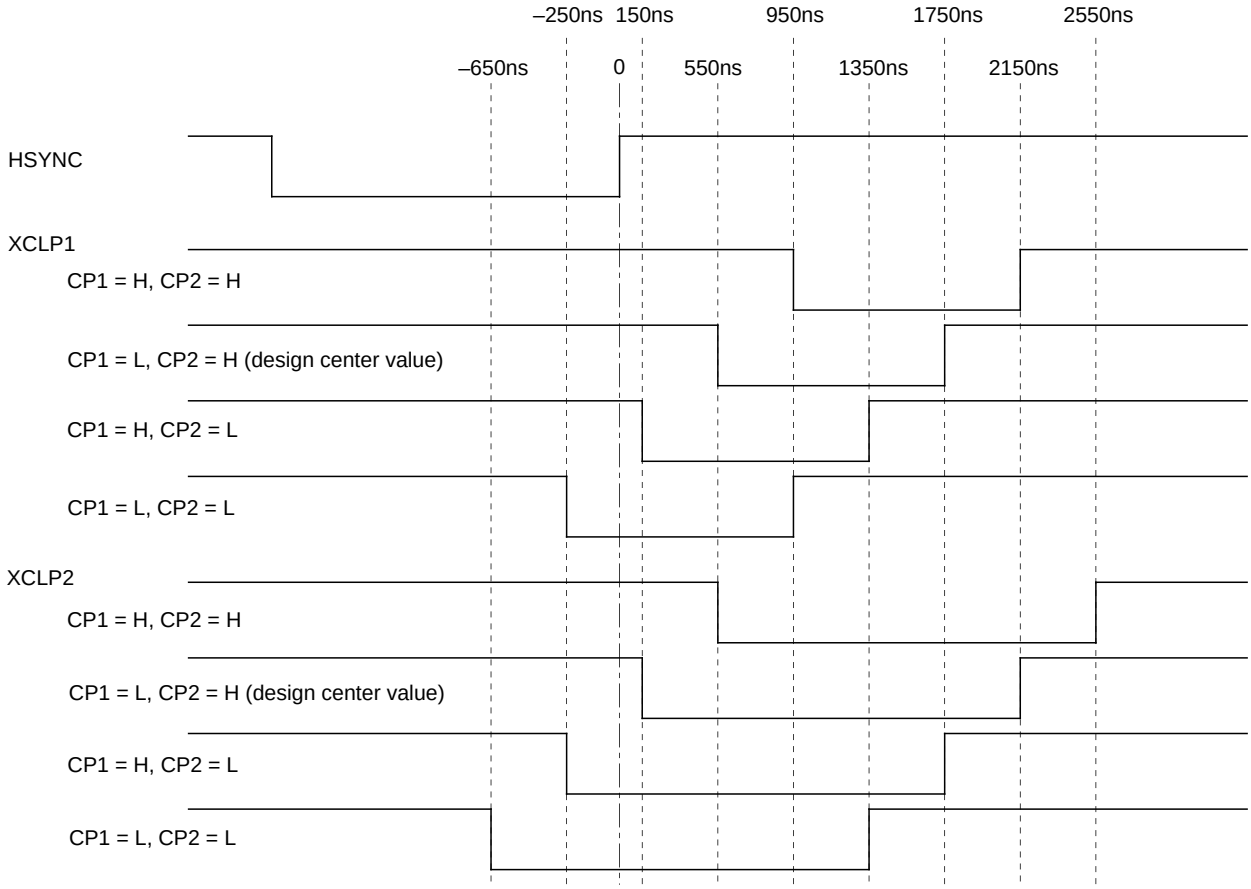


RGT = Low: A output
RGT = High: B output



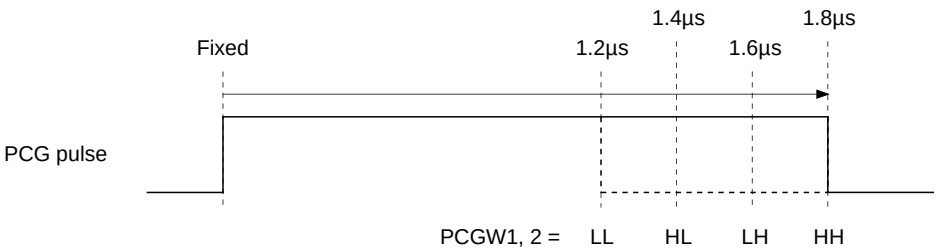
(D) XCLP-POSITION
(CP1, CP2)

These bits control the phase relationship between pedestal clamp pulses XCLP1 and XCLP2 and HSYNC. The phase can be adjusted in 400ns units to four levels. (data: 2 bits)



(E) PCG-POSITION
(PCGW1, PCGW2)

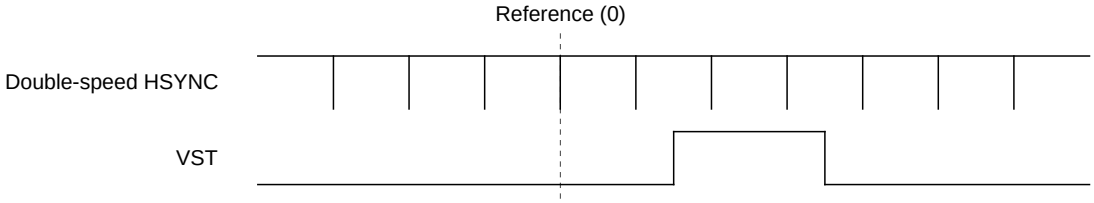
These bits control the PCG1 pulse width (falling edge). The width can be adjusted in 200ns units to four levels. (data: 2 bits)



(F) VWA-POSITION
(VM0J, VM1J, VM2J, VM3J, VM4J, VM5J, VM6J, VM7J, VM8J, VM9J, VM0K, VM1K, VM2K, VM3K, VM4K, VM5K, VM6K, VM7K, VM8K, VM9K)

The VWA pulse rise and fall can be varied in 1H units in the vertical direction.

Rise position: VW0J to 9J (10 bits)
Fall position: VW0K to 9K (10 bits)
Rise, fall transition points: ENB pulse fall position
Reference (0): 1.5H before the VST output position



(G) Double-speed setting
(SLBA)

- This bit sets the built-in line double-speed controller.
  SLBA
  High: Line double-speed controller off
  Low: Line double-speed controller on
- The loop counter is an N multiple of the following.

NTSC	PAL
$910f_H$	$1135f_H$

Notes on operation

The built-in line double-speed controller is supported only when driving a single LCD panel in NTSC/PAL 4:3 mode. When using the CXD2443Q in other modes (NTSC/PAL 16:9 mode, HD mode, 3-panel mode), be sure to set the line double-speed controller to off (SLBA = High).

(H) Double-speed PAL pulse eliminate (MA)

This bit sets the double-speed PAL pulse eliminate (conversion from 575 to 480 vertical lines by 6, 7 pulse eliminate). The setting is as follows.

MA
High: Pulse eliminate off
Low: Pulse eliminate on

The 2N + 1 field pulse eliminate position is shifted 1H (line) to the rear with respect to the 2N field pulse eliminate position.

(I) Right/left and/or up/down inversion (RGT, DWN)

These bits switch the right/left inversion and/or up/down inversion timing for the LCD panel.

Setting		Output				
RGT	DWN	A outputs	B outputs	RGT	XRGT	DWN
H	H	Right scan, down scan	Left scan, down scan	H	L	H
L	H	Left scan, down scan	Right scan, down scan	L	H	H
H	L	Right scan, up scan	Left scan, up scan	H	L	L
L	L	Left scan, up scan	Right scan, up scan	L	H	L

Note) The B outputs (HSTB, HCKnB, SHnB) are the outputs for 3-panel projectors, and are output at the right/left inversed timing of the A outputs.

(J) Various settings

SLFR
This bit sets the cycle of the LCD AC drive signals FRP and XFRP.
High: 1H (line) inversion
Low: 1F (field) inversion

VPOL, HPOL
These bits set the input SYNC polarity.
High: Negative polarity
Low: Positive polarity

SL3B

This bit sets the 3-panel projector output (B outputs) switching.

The HSTB, HCKnB, and SHnB outputs can be switched on and off.

High: B outputs off

Low: B outputs on

Note) When driving a single LCD panel, set the B outputs to off (SL3B = High).

SLVWB

This bit sets the VWB output.

High: VWB off

Low: VWB on

SLEG

This bit sets the VWB transition timing.

High: HSYNC front edge

Low: HSYNC rear edge

Note) VWB is the equalizing pulse masking pulse.

The rise position is counted from the VD inside the previous field. Therefore, when the number of lines within one field differs from the standard protocol, the phase between the next field's VSYNC and the VWB rise position changes.

The phase also changes when a value other than the default value is used as the V-POSITION setting.

(K) Mode settings

SNSL

This bit sets the double-speed HSYNC and standard HSYNC (or CSYNC) input switching.

High: Double-speed HSYNC input

Low: Standard HSYNC (CSYNC) input

Note) When using the built-in line double-speed controller, only the standard HSYNC is supported.

Set SNSL to standard HSYNC input (SNSL = Low).

NT-PAL, XWID, HD

These bits set the various display modes.

	NT-PAL	XWID	XHD
NTSC (4:3)	H	H	H
NTSC (16:9)	H	L	H
PAL (4:3)	L	H	H
PAL (16:9)	L	L	H
HD	*	*	L

Note) Test mode

Serial data TEST1, TEST2, TEST3 and TEST4 are test mode data. Care should be taken as these bits are not used, and must be set to High.

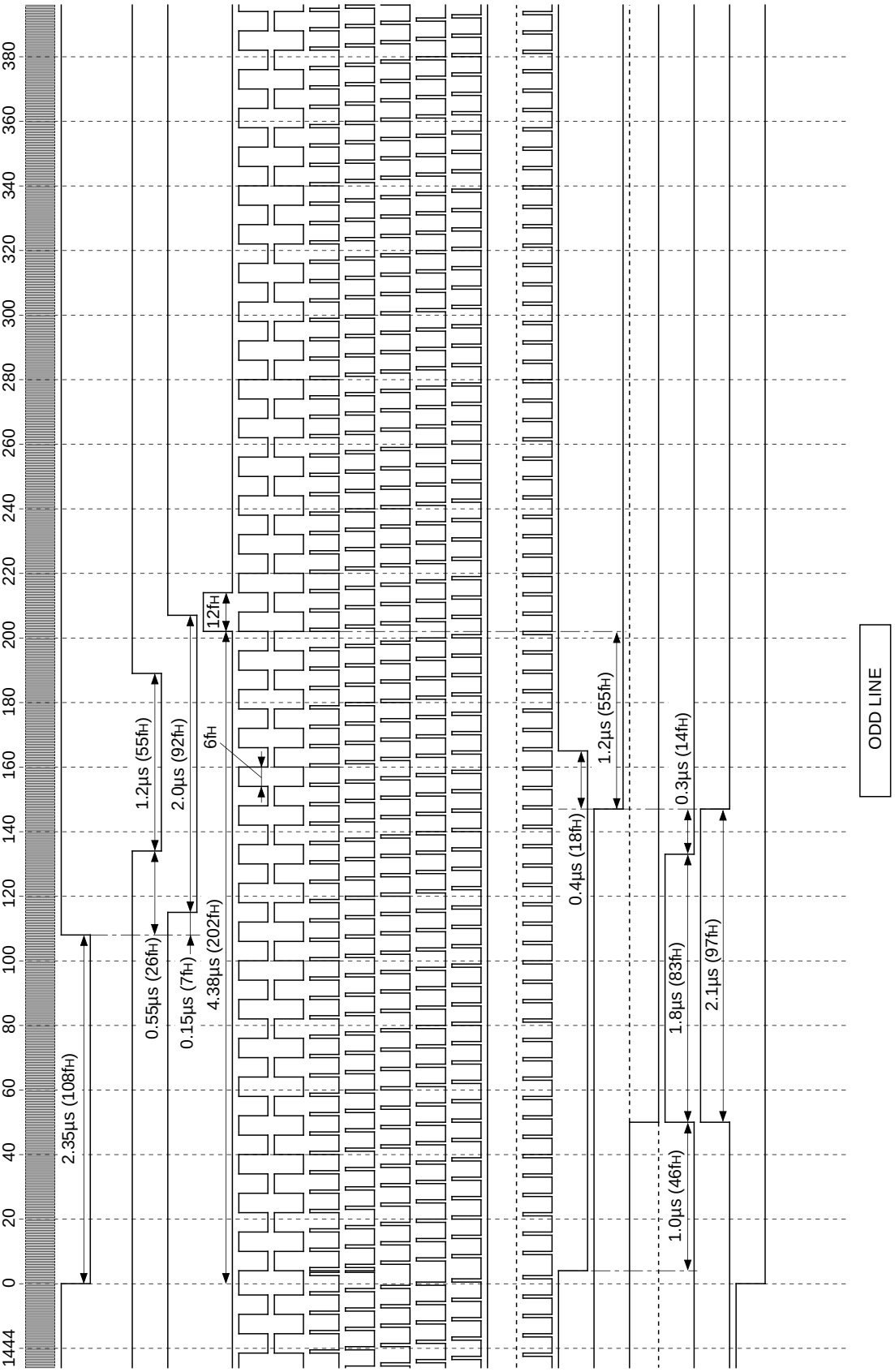
NTSC (4:3) Horizontal Direction Timing Chart

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL CP1, 2: LH PCGW1, 2: HH RGT: H DWN: H

HPOL: H SLFR: H SNSL: H NT-PL: H XWID: H XHD: H

Loop counter 1464fH

Master Clock 46.07MHz



Note) The FRP polarity is not specified for each line and field.

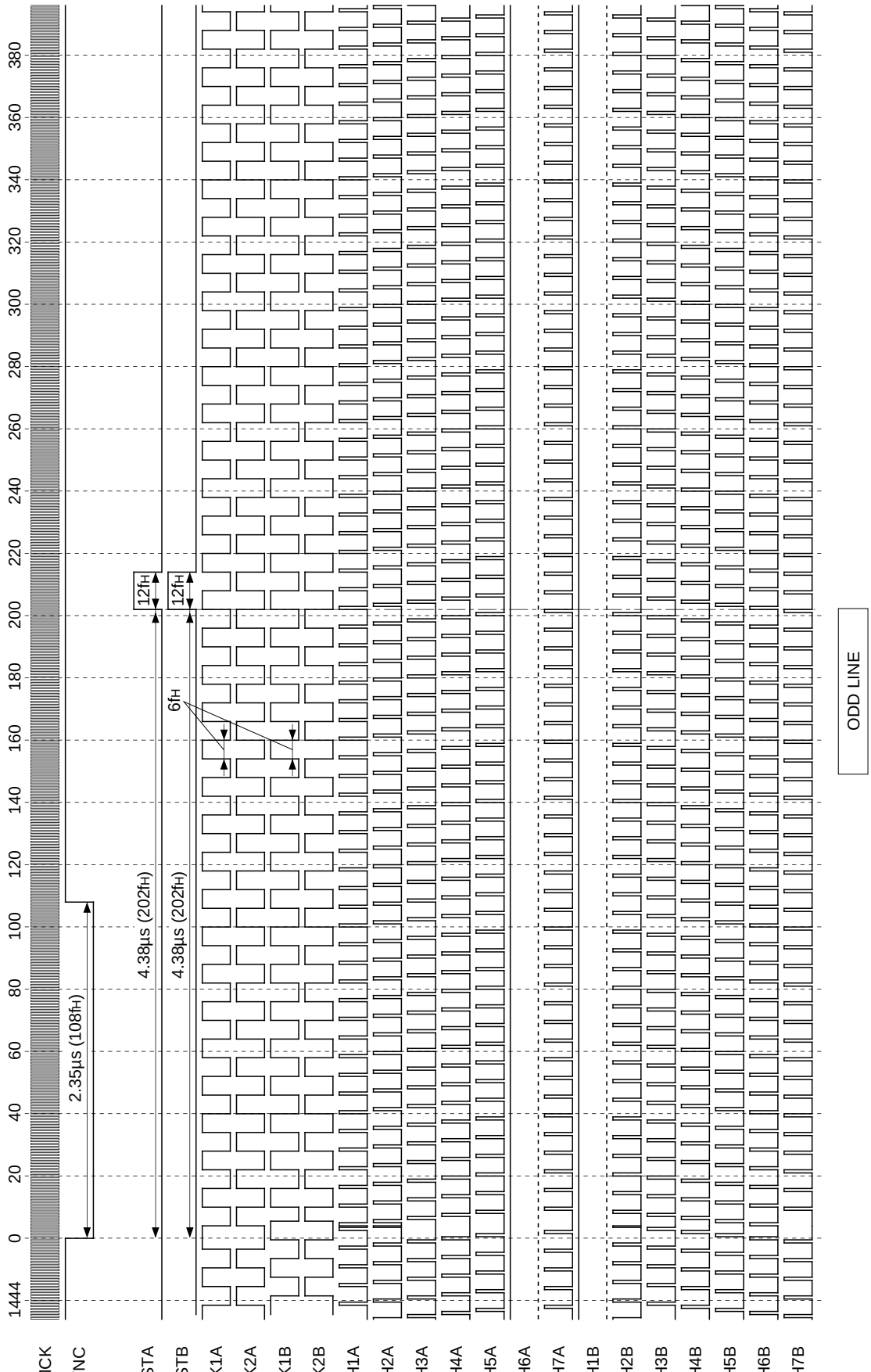
NTSC (4:3) Horizontal Direction Timing Chart (B outputs)

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL RGT: H DWN: H

HPOL: H SLFR: H SL3B: L SNSL: H NT-PL: H XWID: H XHD: H

Loop counter 1464f_H

Master Clock 46.07MHz



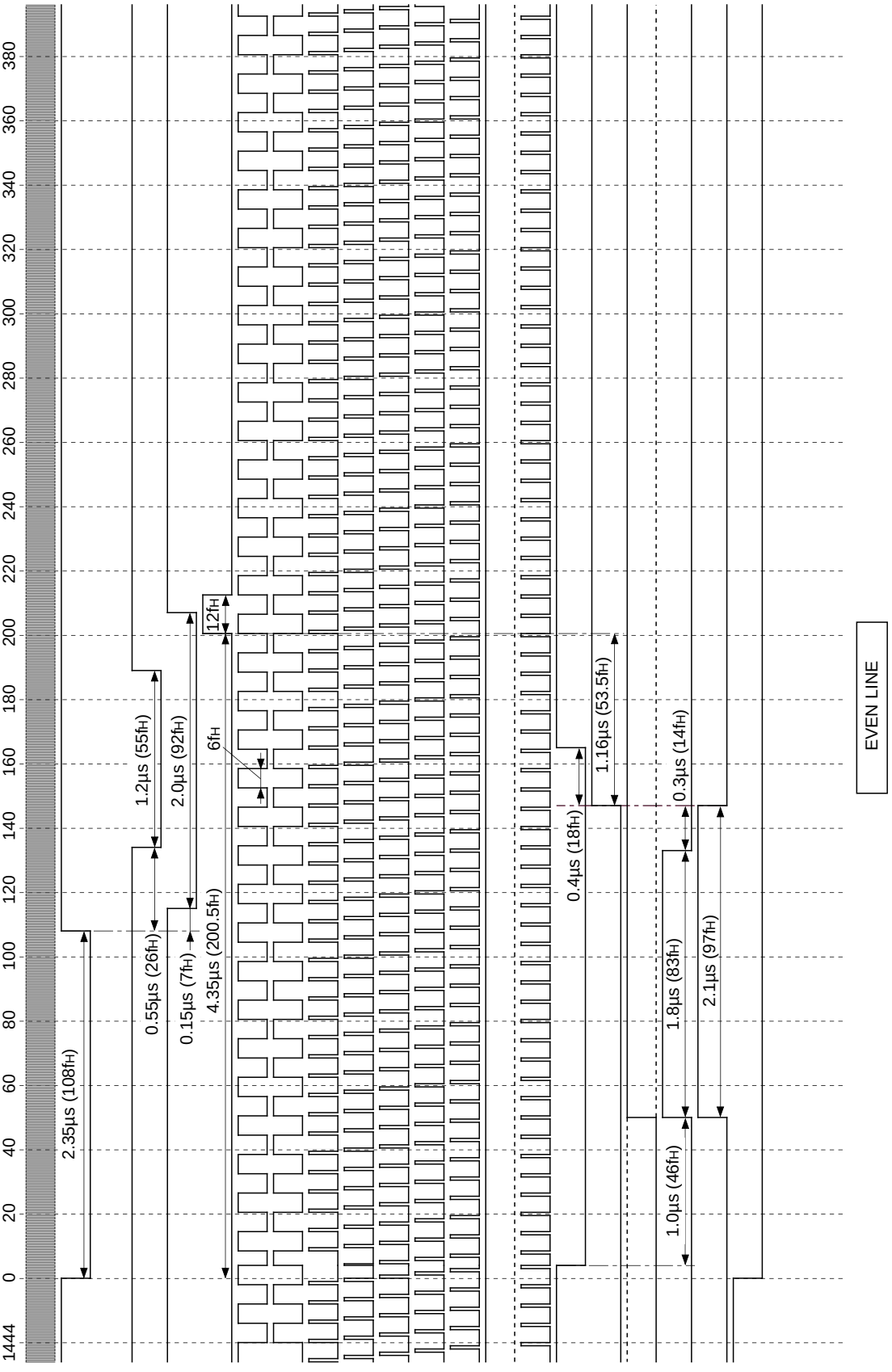
NTSC (4:3) Horizontal Direction Timing Chart

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL CP1, 2: LH PCGW1, 2: HH RGT: H DWN: H

HPOL: H SLFR: H SNSL: H NT-PL: H XWID: H XHD: H

Loop counter 1464fH

Master Clock 46.07MHz



Note) The FRP polarity is not specified for each line and field.

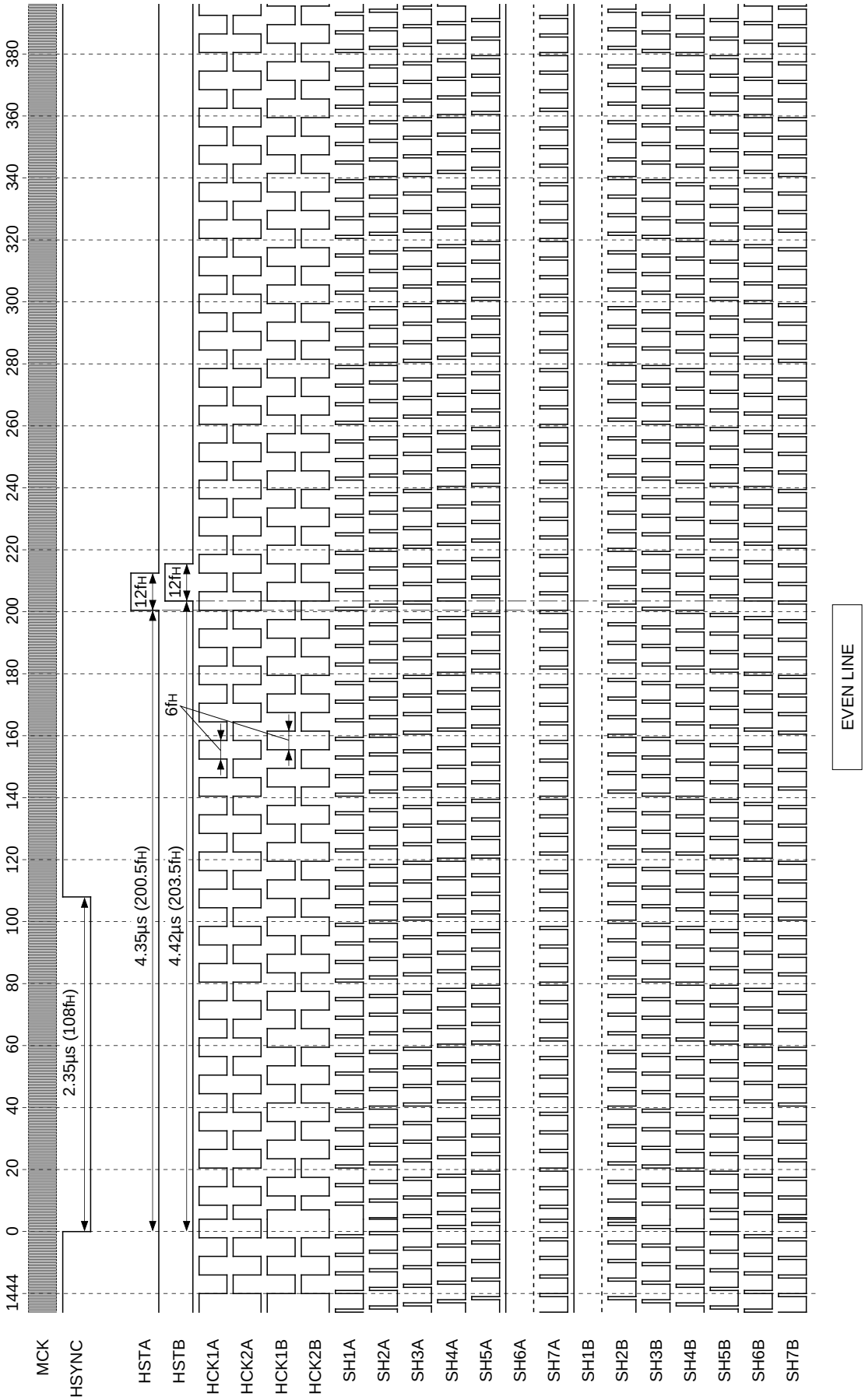
NTSC (4:3) Horizontal Direction Timing Chart (B outputs)

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL RGT: H DWN: H

HPOL: H SLFR: H SL3B: L SNSL: H NT-PL: H XWID: H XHD: H

Loop counter 1464f_H

Master Clock 46.07MHz



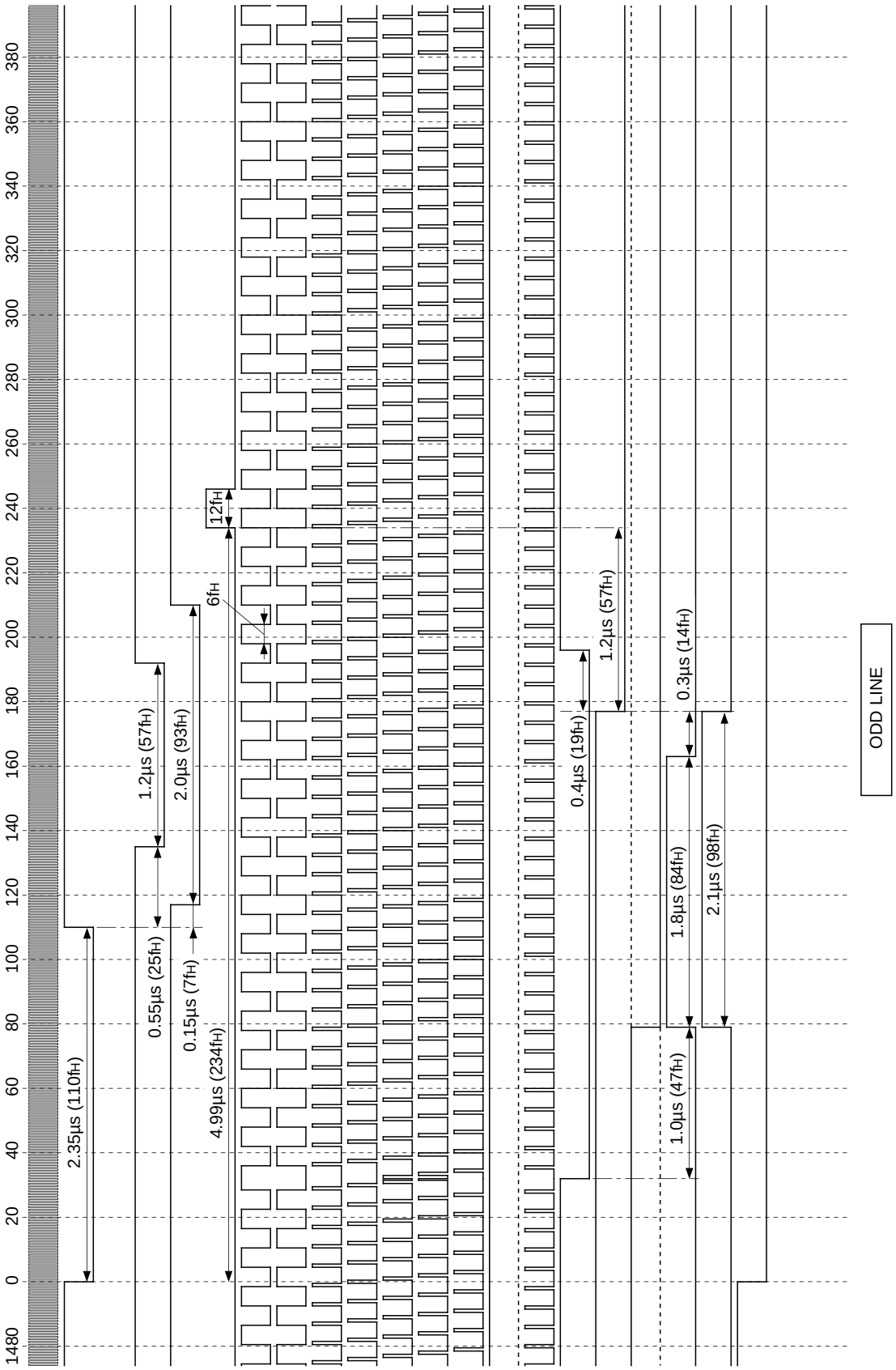
PAL (4:3) Horizontal Direction Timing Chart

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL CP1, 2: LH PCGW1, 2: HH RGT: H DWN: H

HPOL: H SLFR: H SNSL: H NT-PL: L XWID: H XHD: H

Loop counter 1500f_H

Master Clock 46.88MHz



Note) The FRP polarity is not specified for each line and field.

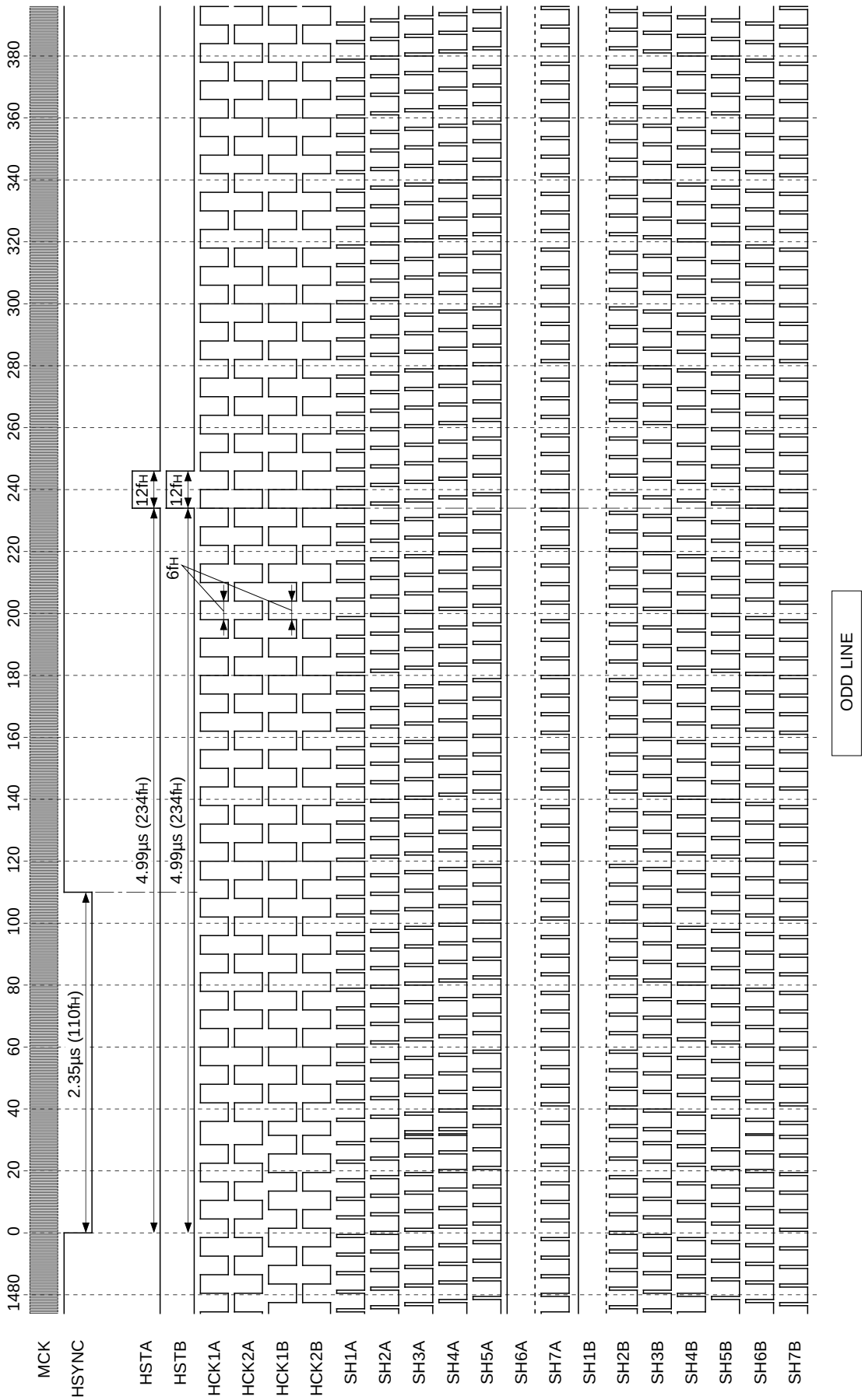
PAL (4:3) Horizontal Direction Timing Chart (B outputs)

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL RGT: H DWN: H

HPOL: H SLFR: H SL3B: L SNSL: H NT-PL: L XWID: H XHD: H

Loop counter 1500f_H

Master Clock 46.88MHz



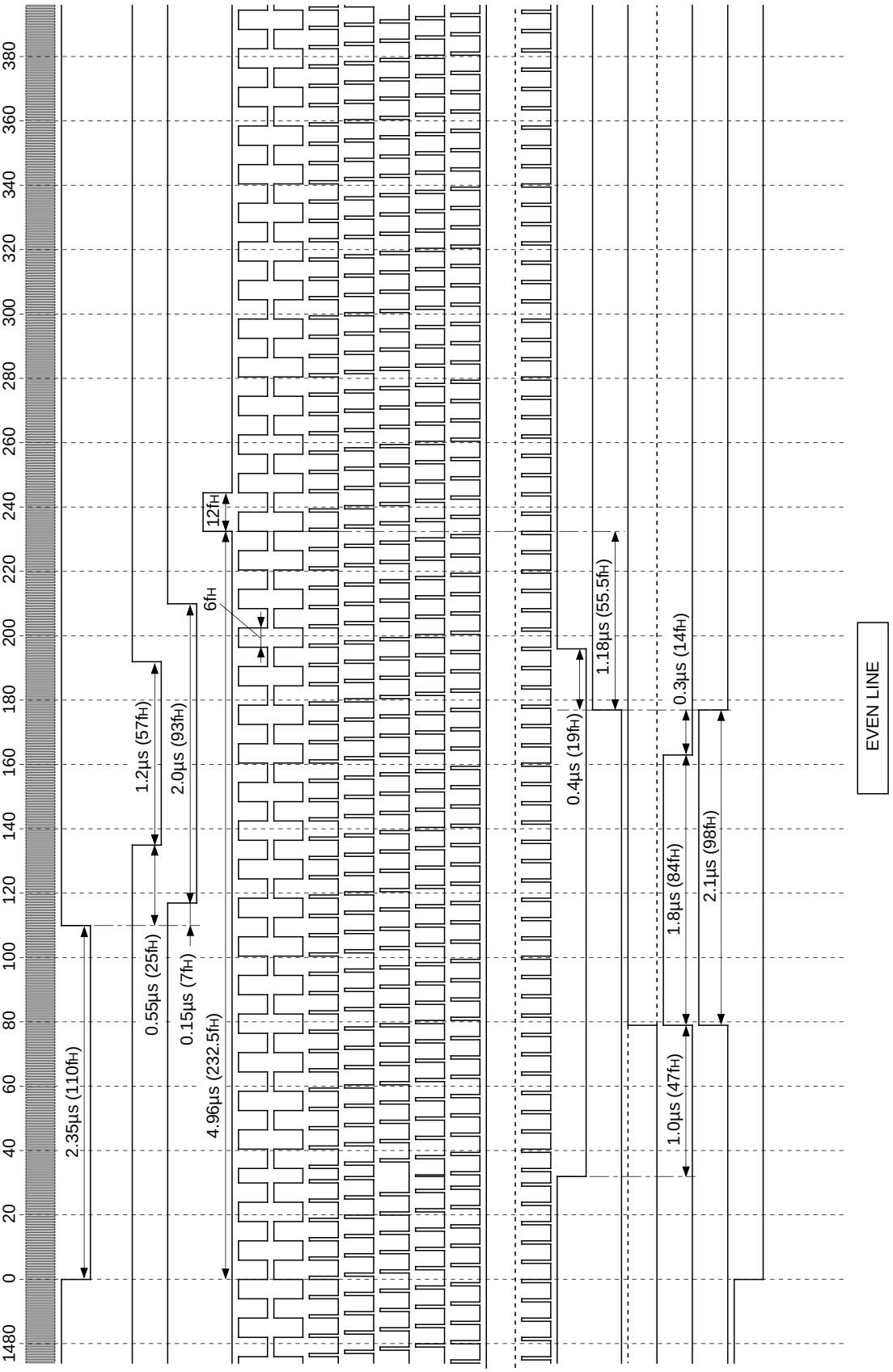
PAL (4:3) Horizontal Direction Timing Chart

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL CP1, 2: LH PCGW1, 2: HH RGT: H DWN: H

HPOL: H SLFR: H SNSL: H NT-PL: L XWID: H XHD: H

Loop counter 1500f_H

Master Clock 46.88MHz



Note) The FRP polarity is not specified for each line and field.

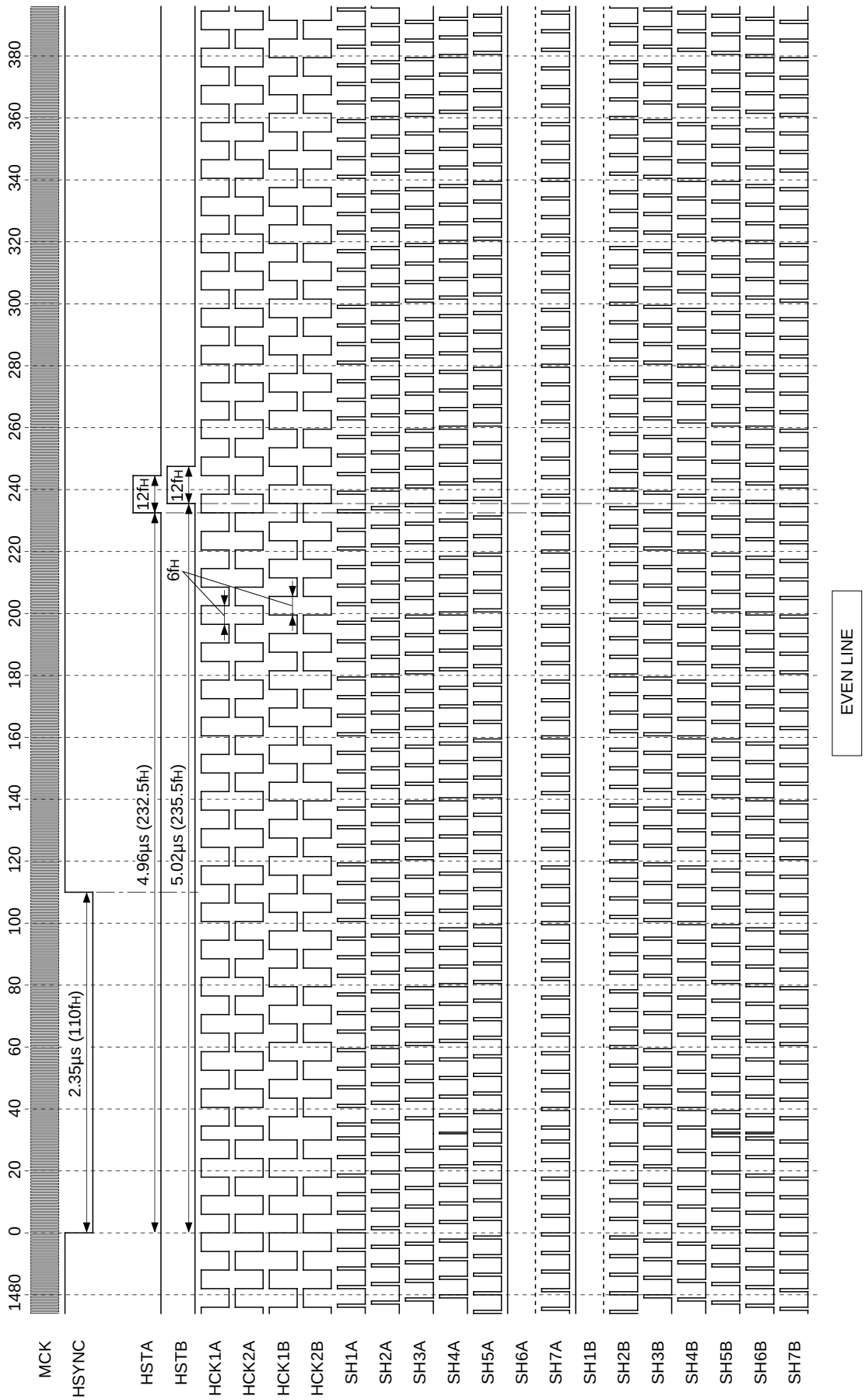
PAL (4:3) Horizontal Direction Timing Chart (B outputs)

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL RGT: H DWN: H

HPOL: H SLFR: H SL3B: L SNSL: H NT-PL: L XWID: H XHD: H

Loop counter 1500f_H

Master Clock 46.88MHz



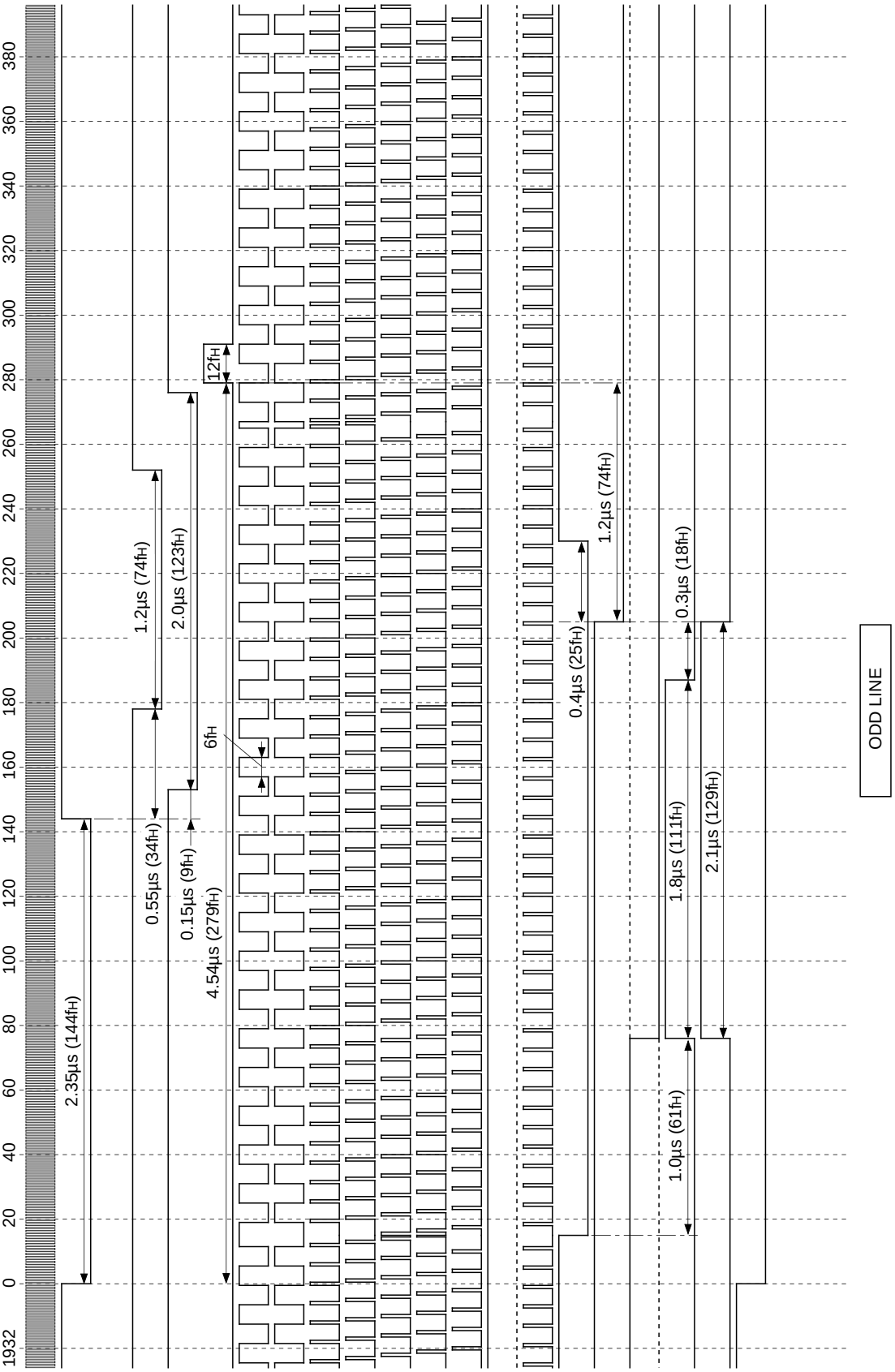
NTSC (16:9) Horizontal Direction Timing Chart

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL CP1, 2: LH PCGW1, 2: HH RGT: H DWN: H

HPOL: H SLFR: H SNSL: H NT-PL: H XWID: L XHD: H

Loop counter 1952fH

Master Clock 61.43MHz



Note) The FRP polarity is not specified for each line and field.

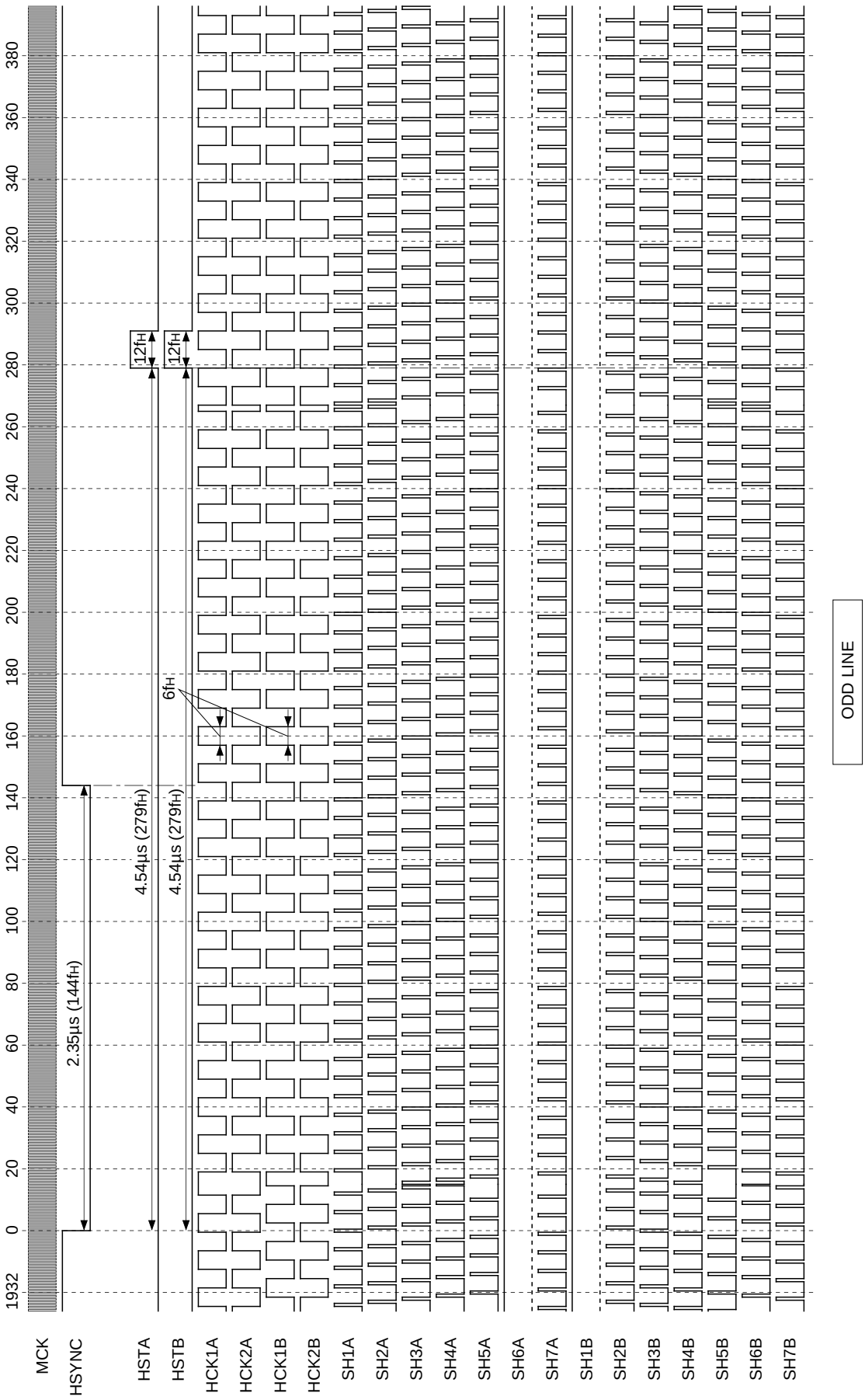
NTSC (16:9) Horizontal Direction Timing Chart (B outputs)

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL RGT: H DWN: H

HPOL: H SLFR: H SL3B: L SNSL: H NT-PL: H XWID: L XHD: H

Loop counter 1952fH

Master Clock 61.43MHz



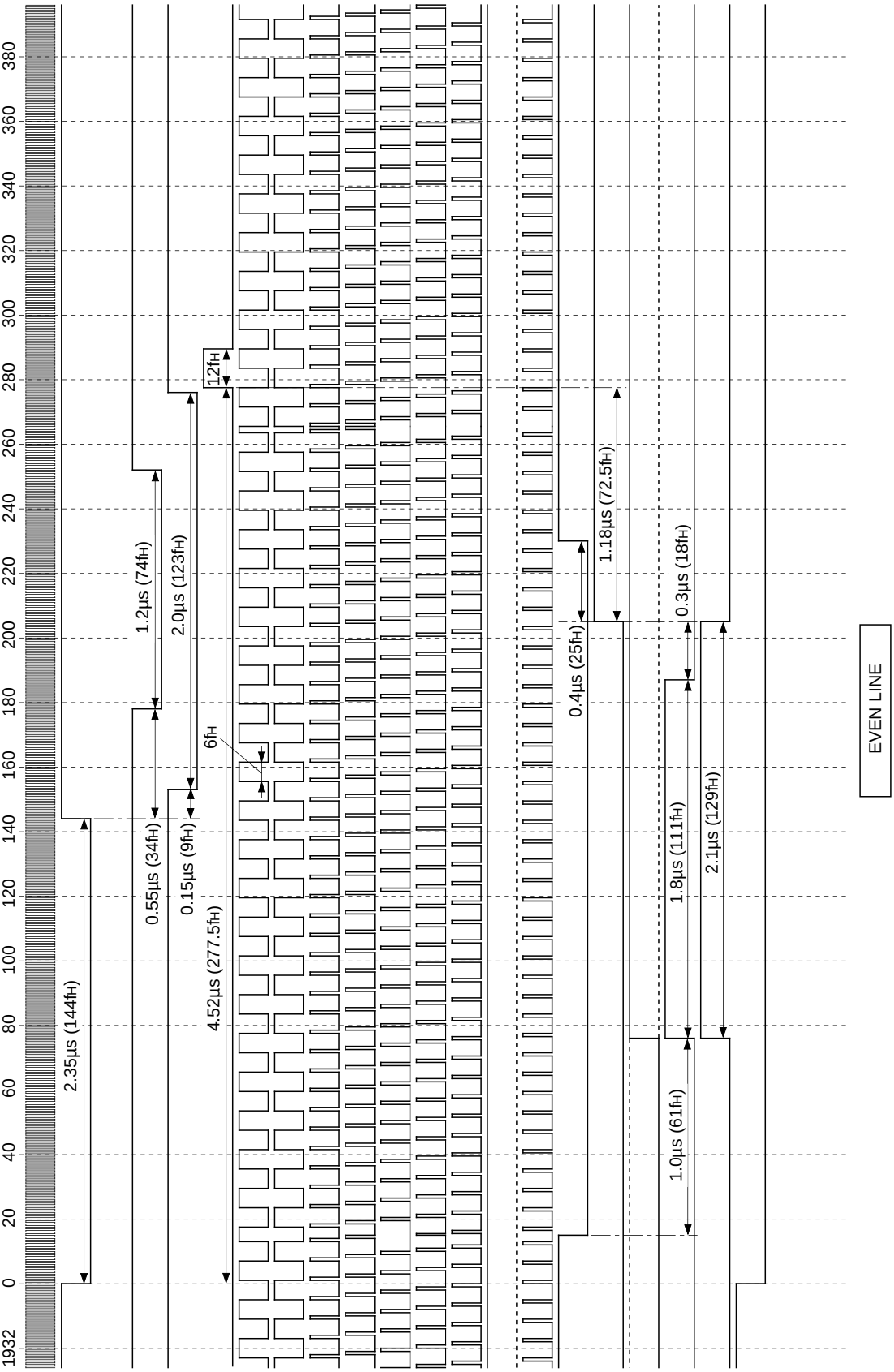
NTSC (16:9) Horizontal Direction Timing Chart

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL CP1, 2: LH PCGW1, 2: HH RGT: H DWN: H

HPOL: H SLFR: H SNSL: H NT-PL: H XWID: L XHD: H

Loop counter 1952fH

Master Clock 61.43MHz



Note) The FRP polarity is not specified for each line and field.

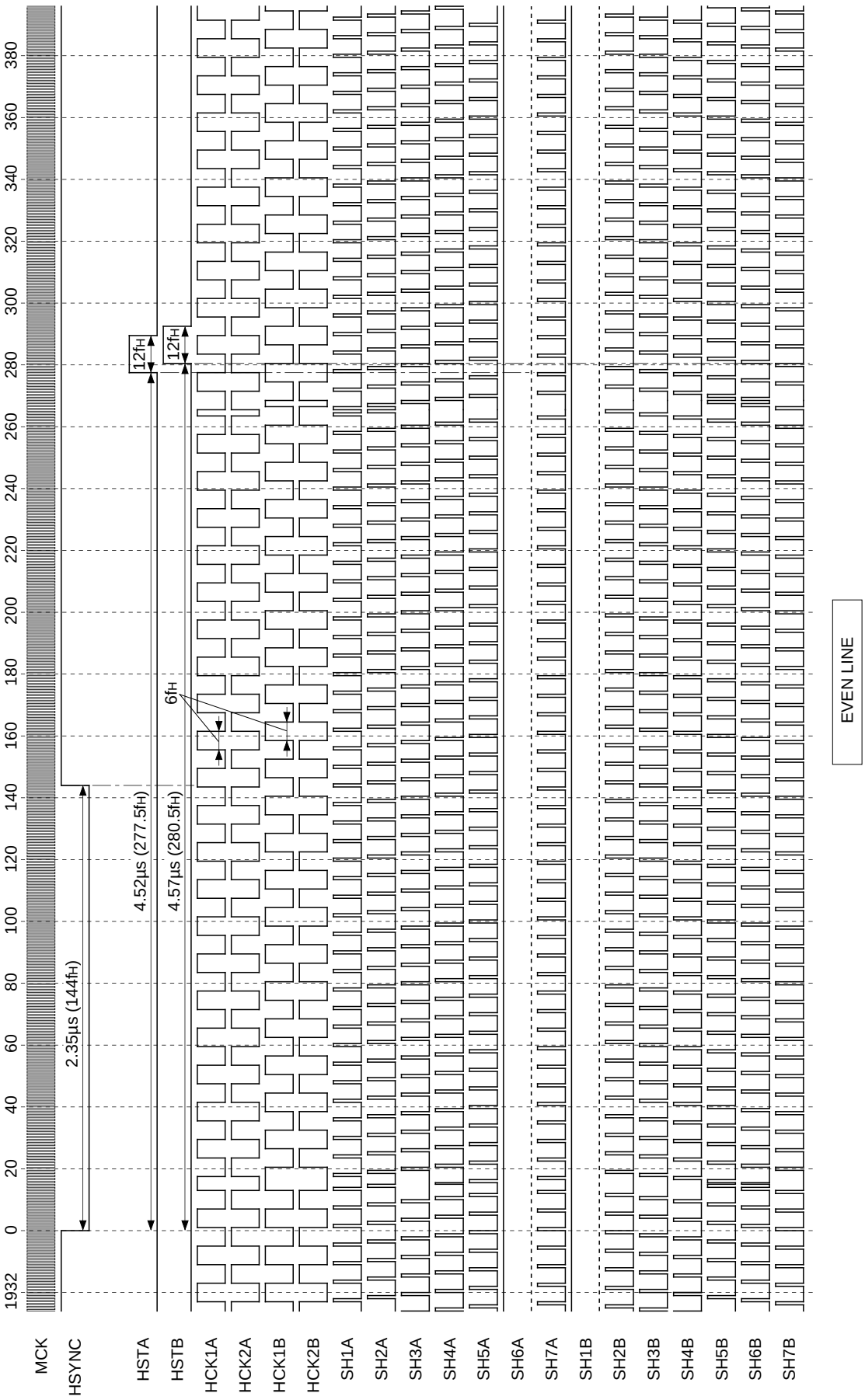
NTSC (16:9) Horizontal Direction Timing Chart (B outputs)

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL RGT: H DWN: H

HPOL: H SLFR: H SL3B: L SNSL: H NT-PL: H XWID: L XHD: H

Loop counter 1952fH

Master Clock 61.43MHz



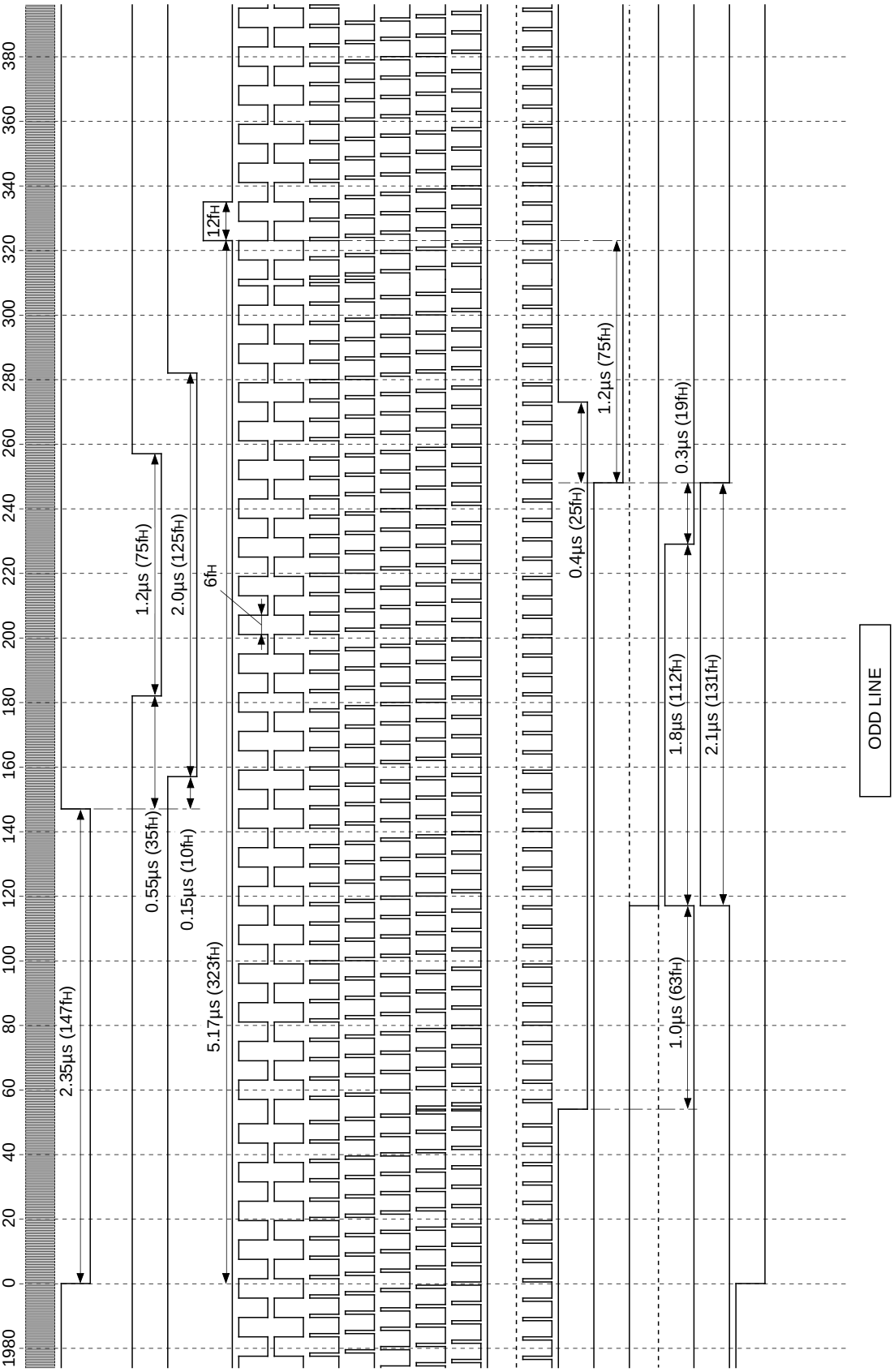
PAL (16:9) Horizontal Direction Timing Chart

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL CP1, 2: LH PCGW1, 2: HH RGT: H DWN: H

HPOL: H SLFR: H SNSL: H NT-PL: L XWID: L XHD: H

Loop counter 2000f_H

Master Clock 62.5MHz



Note) The FRP polarity is not specified for each line and field.

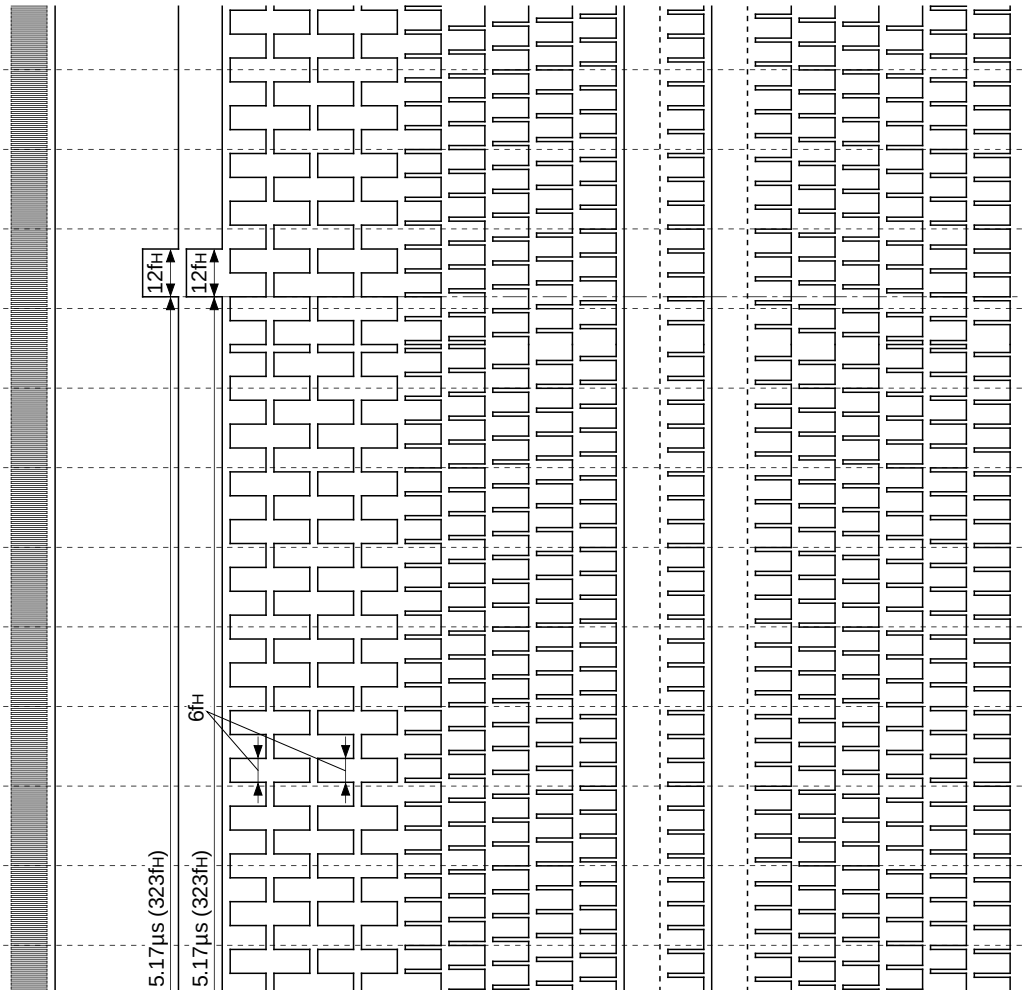
PAL (16:9) Horizontal Direction Timing Chart (B outputs)

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL RGT: H DWN: H

HPOL: H SLFR: H SL3B: L SNSL: H NT-PL: L XWID: L XHD: H

Loop counter 2000fH

Master Clock 62.5MHz



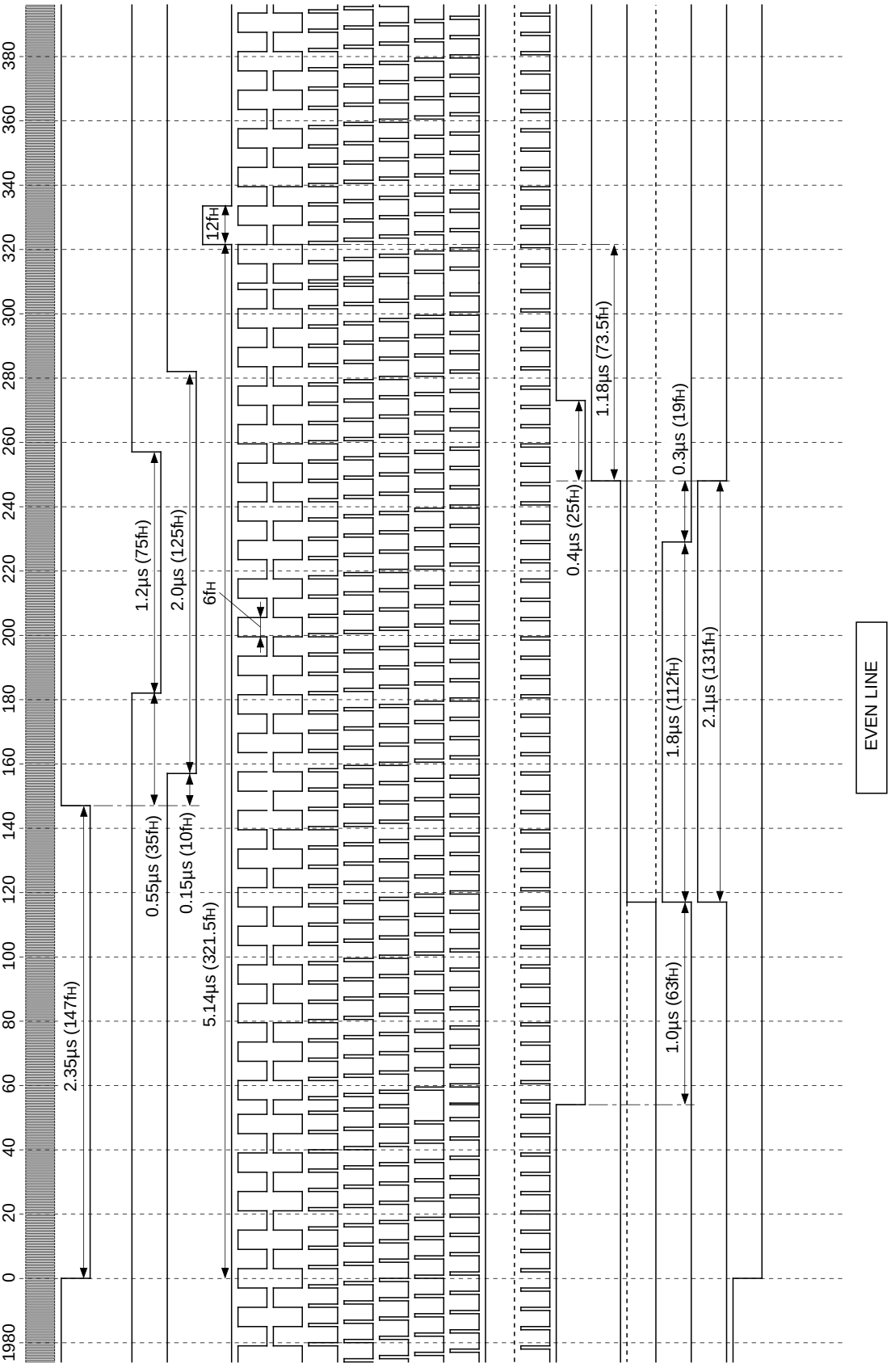
PAL (16:9) Horizontal Direction Timing Chart

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL CP1, 2: LH PCGW1, 2: HH RGT: H DWN: H

HPOL: H SLFR: H SNSL: H NT-PL: L XWID: L XHD: H

Loop counter 2000f_H

Master Clock 62.5MHz



Note) The FRP polarity is not specified for each line and field.

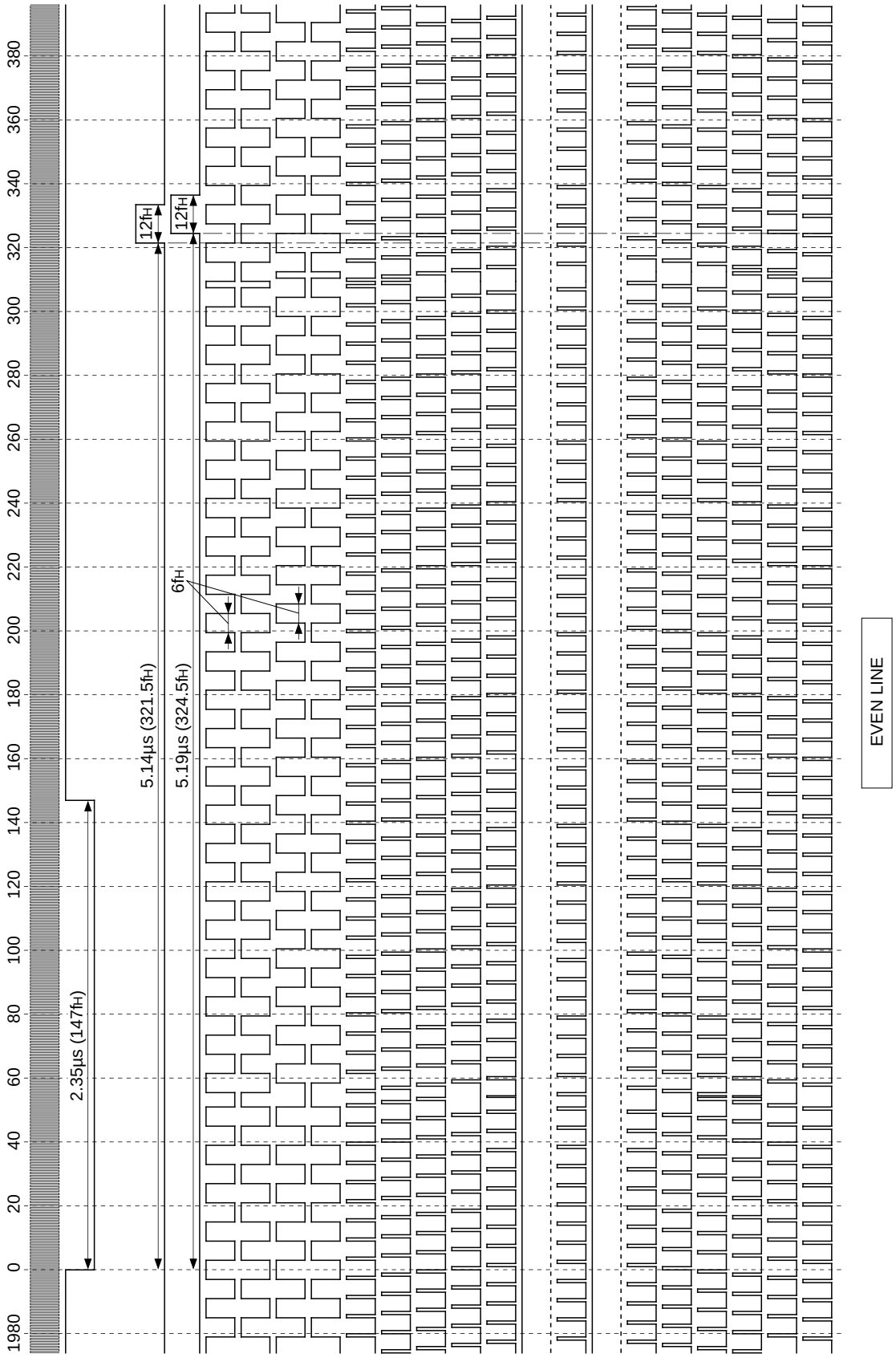
PAL (16:9) Horizontal Direction Timing Chart (B outputs)

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL RGT: H DWN: H

HPOL: H SLFR: H SL3B: L SNSL: H NT-PL: L XWID: L XHD: H

Loop counter 2000f_H

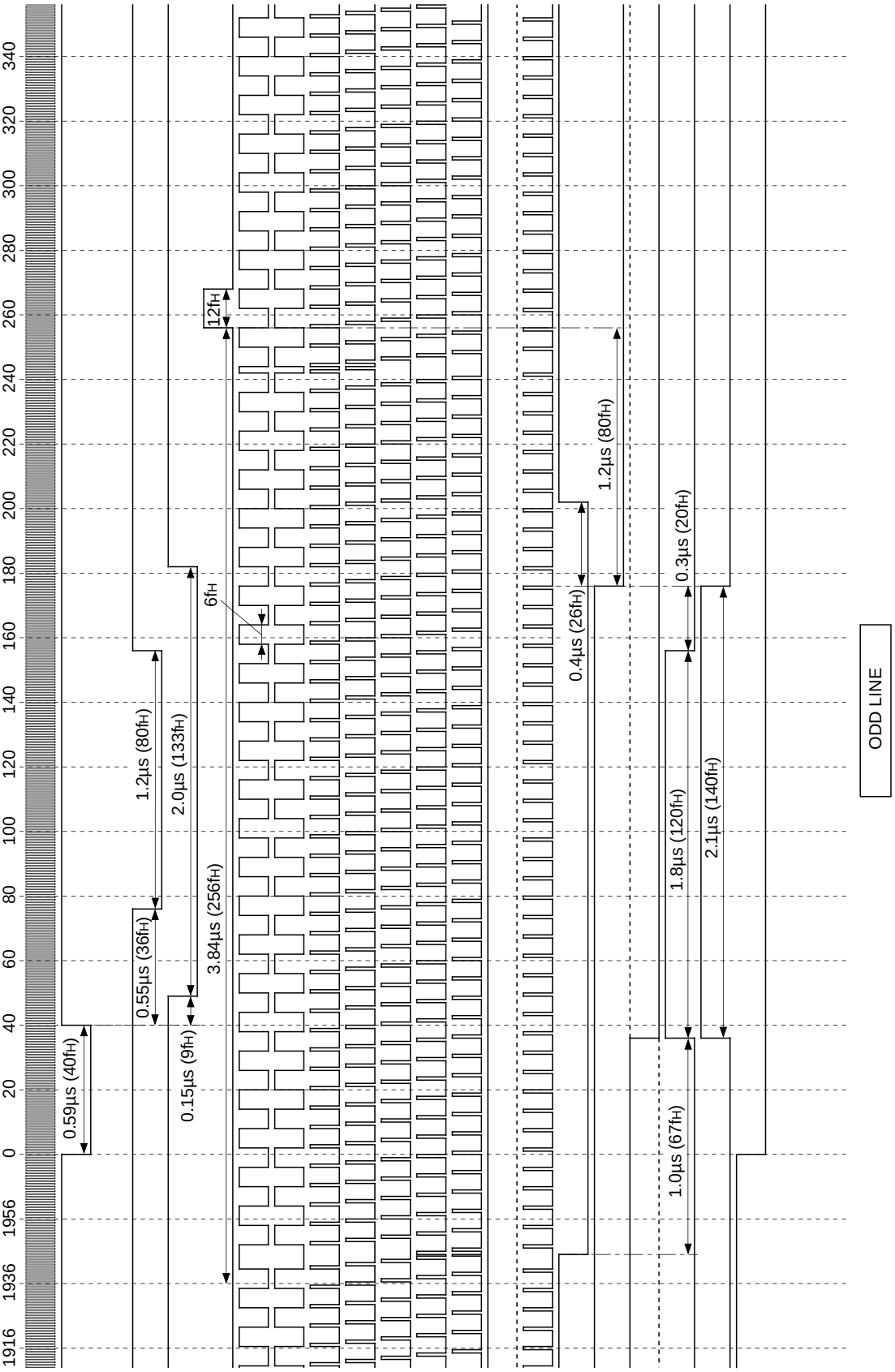
Master Clock 62.5MHz



HD Horizontal Direction Timing Chart

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL CP1, 2: LH PCGW1, 2: HH RGT: H DWN: H
HPOL: H SLFR: H XHD: L

Loop counter 1976fH
Master Clock 66.69MHz



Note) The FRP polarity is not specified for each line and field.

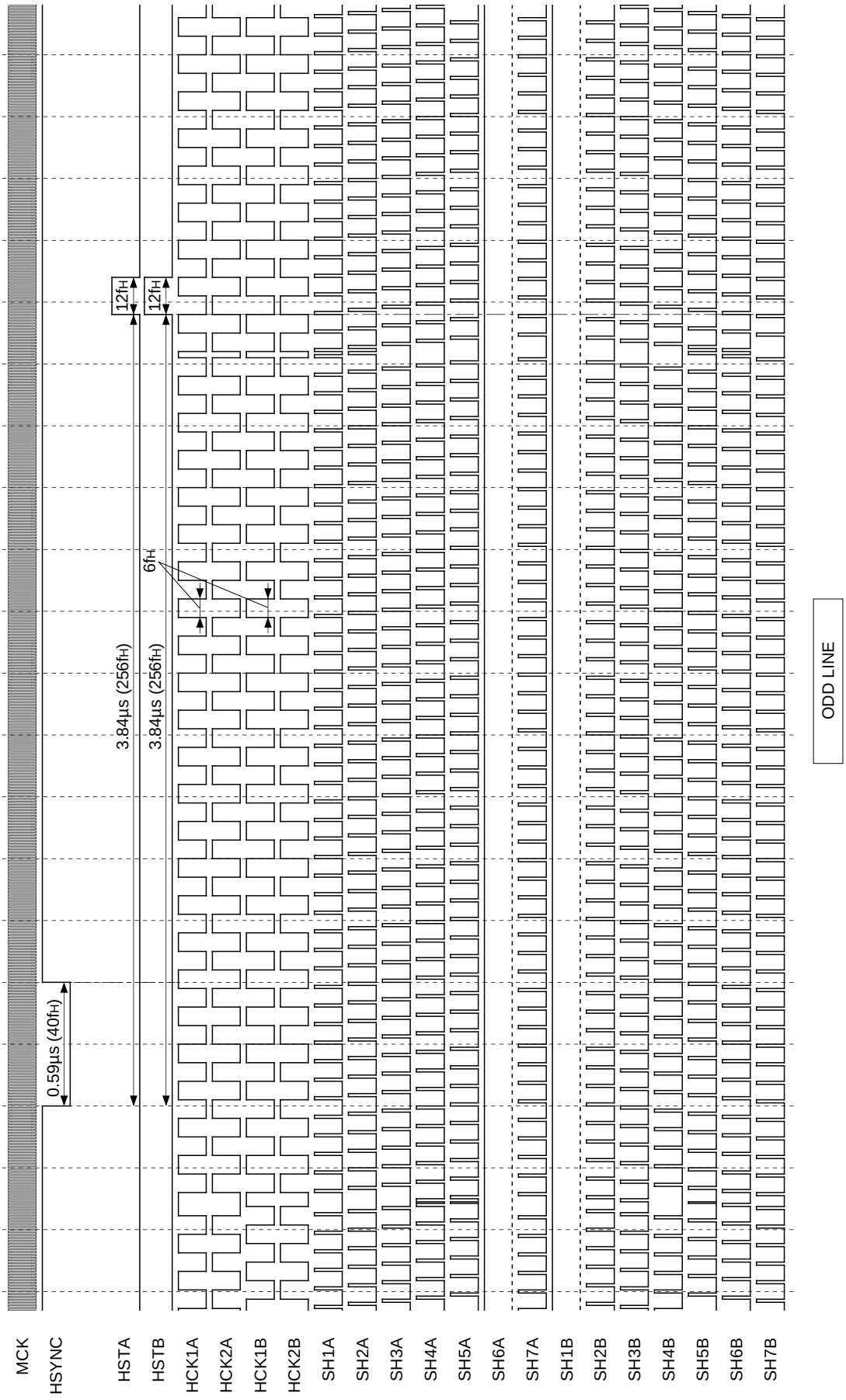
HD Horizontal Direction Timing Chart (B outputs)

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL RGT: H DWN: H

HPOL: H SLFR: H SL3B: L XHD: L

Loop counter 1976f_H

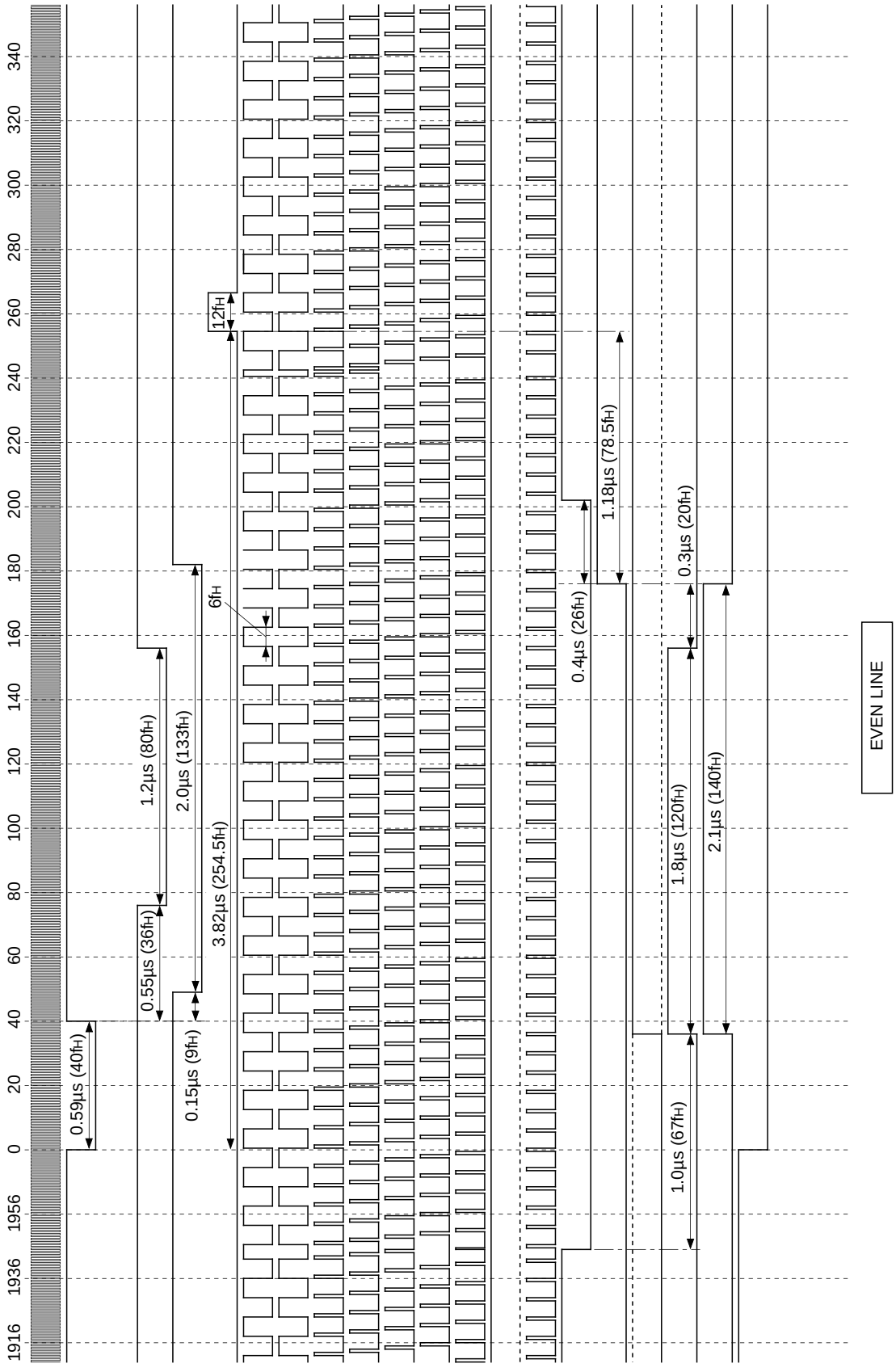
Master Clock 66.69MHz



HD Horizontal Direction Timing Chart

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL CP1, 2: LH PCGW1, 2: HH RGT: H DWN: H
HPOL: H SLFR: H XHD: L

Loop counter 1976fH
Master Clock 66.69MHz



Note) The FRP polarity is not specified for each line and field.

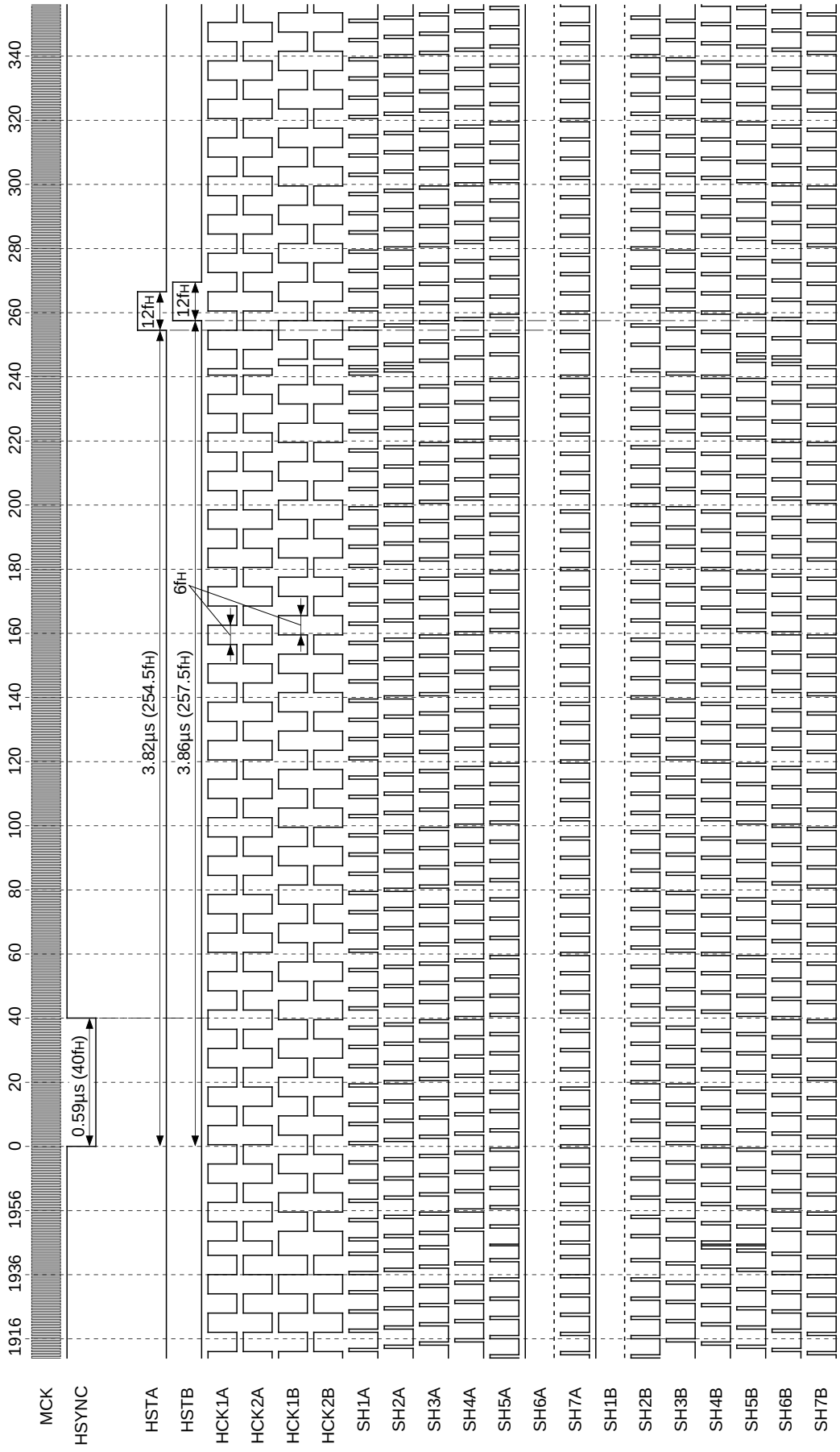
HD Horizontal Direction Timing Chart (B outputs)

HP1, 2, 3, 4, 5, 6, 7, 8: LLLLLLLH SLSH1, 2, 3, 4: LLLL RGT: H DWN: H

HPOL: H SLFR: H SL3B: L XHD: L

Loop counter 1976fH

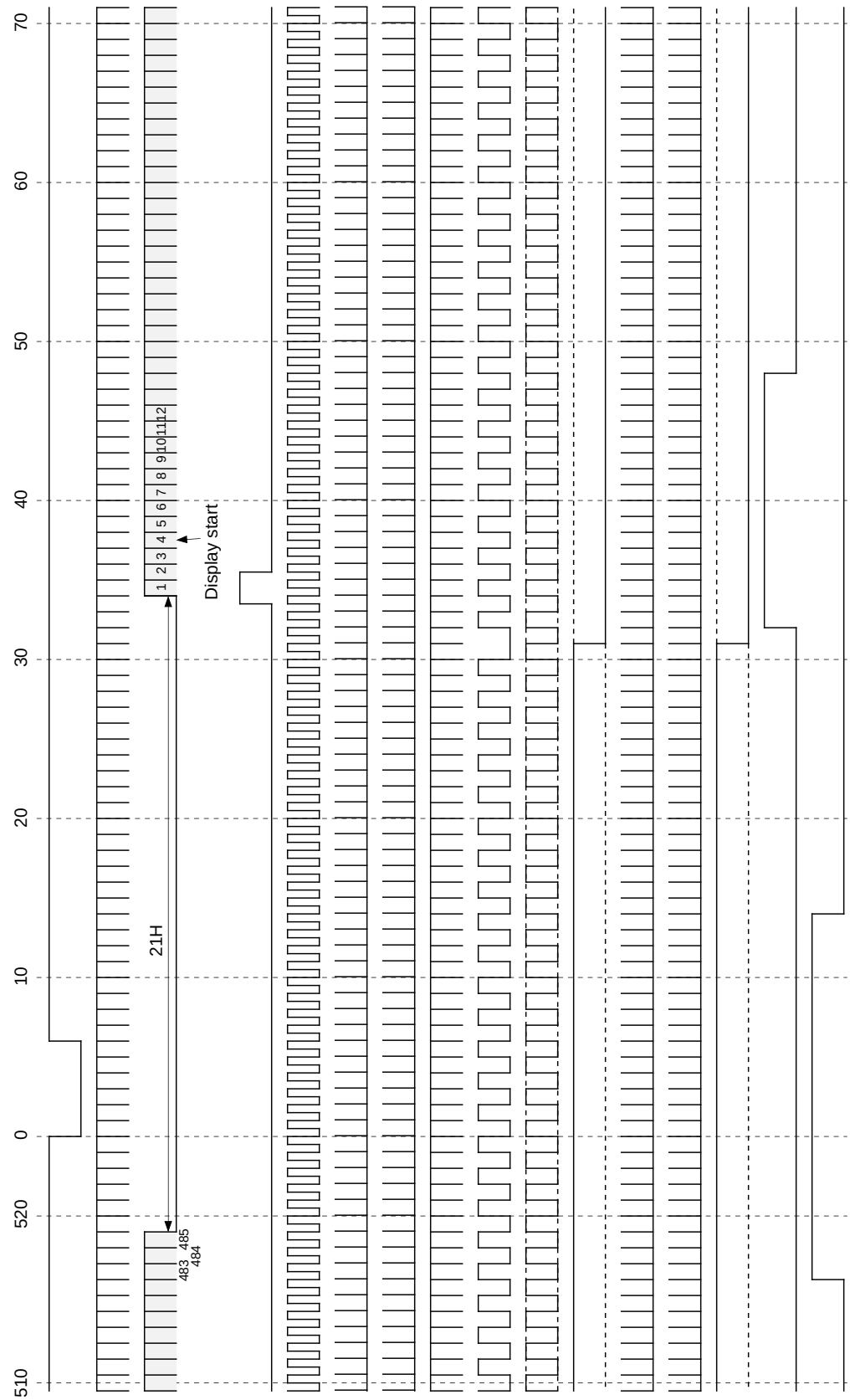
Master Clock 66.69MHz



NTSC (double-speed HSYNC input) Vertical Direction Timing Chart

VP1, 2, 3, 4: LLLH VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLLLLLL VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLHLLLL

MA: H SL3B: L VPOL: H SNSL: H NT-PL: H XHD: H

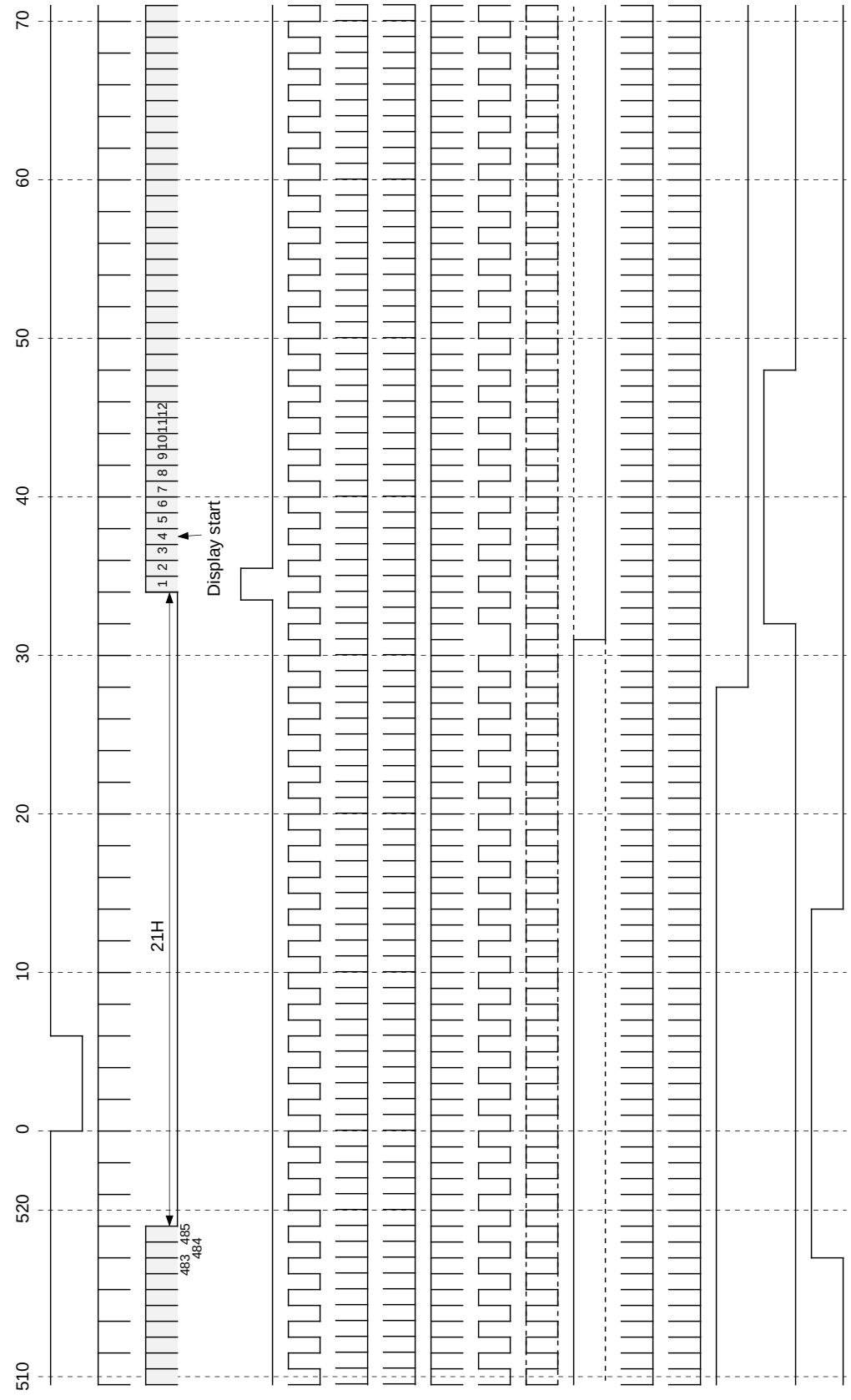


Note) The FRP polarity is not specified for each line and field.
(BLK) in the timing chart is a pulse indicated as a reference and is not a pulse output from pins.

NTSC (standard HSYNC input) Vertical Direction Timing Chart

VP1, 2, 3, 4: LLLH VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLLLLLL VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLHLLLL

MA: H SL3B: L VPOL: H SNSL: L NT-PL: H XHD: H

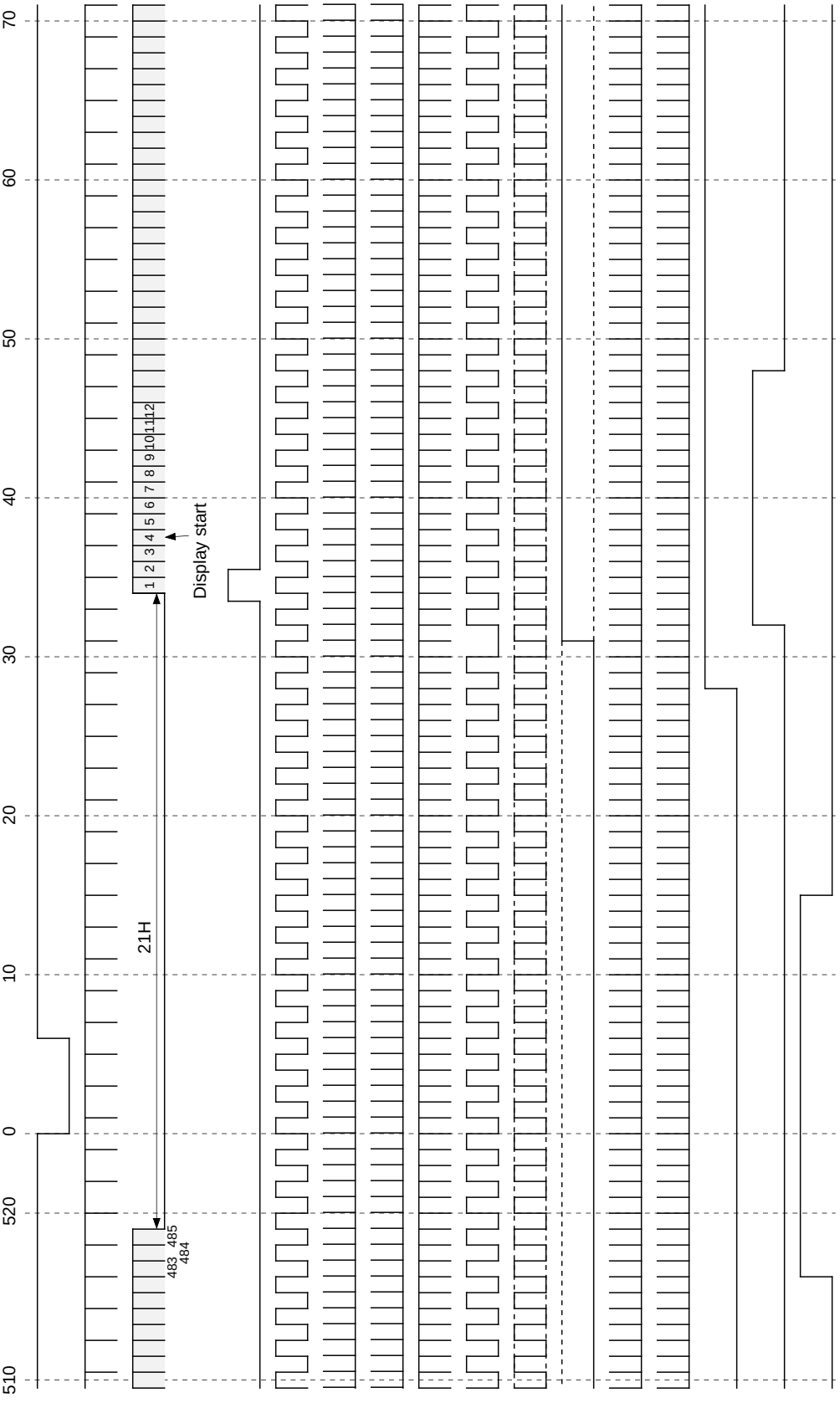


Note) The FRP polarity is not specified for each line and field.
(BLK) in the timing chart is a pulse indicated as a reference and is not a pulse output from pins.

NTSC (standard HSYNC input) Vertical Direction Timing Chart

VP1, 2, 3, 4: LLLH VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLLLLLL VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLHLLLL

MA: H SL3B: L VPOL: H SNSL: L NT-PL: H XHD: H

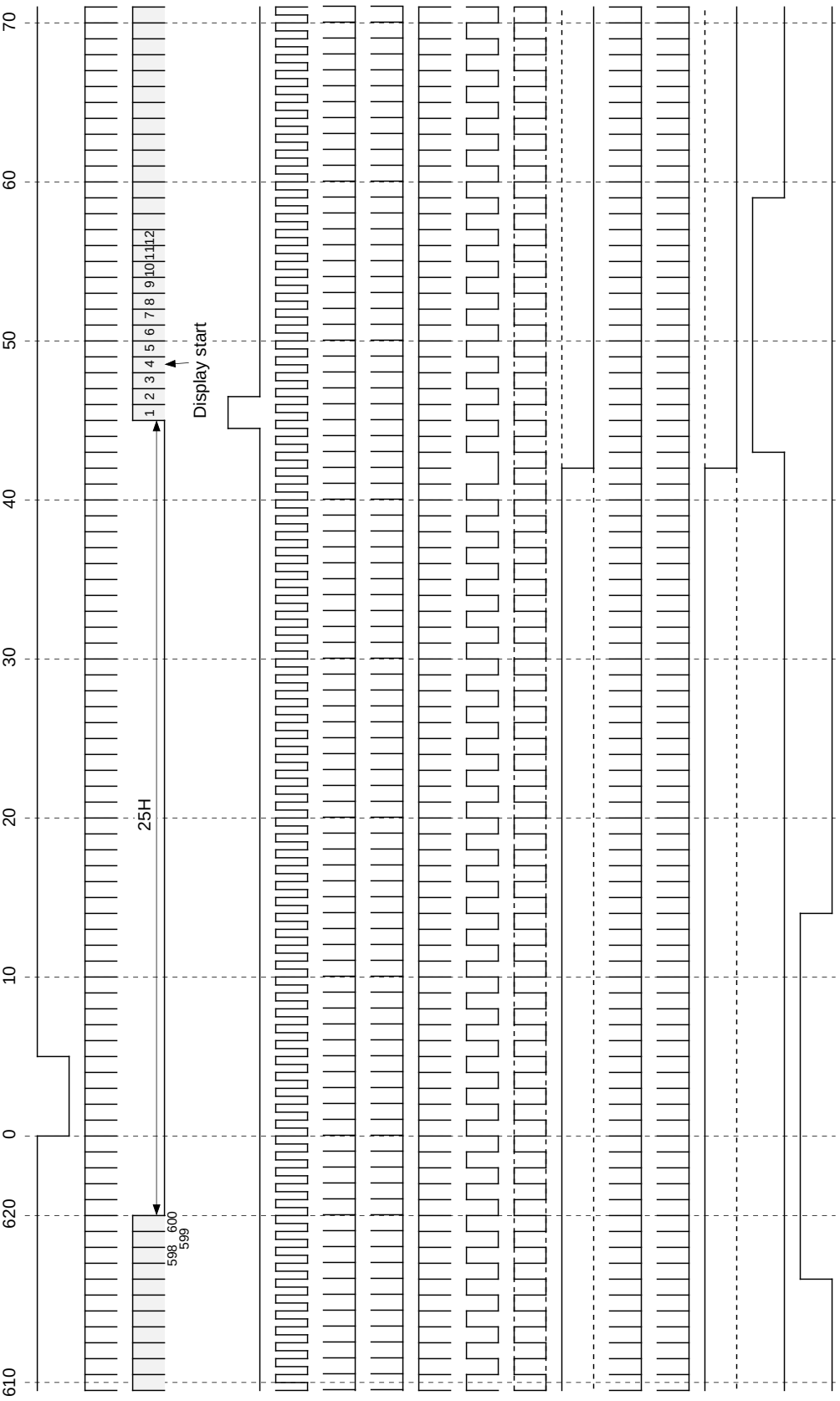


Note) The FRP polarity is not specified for each line and field.
(BLK) in the timing chart is a pulse indicated as a reference and is not a pulse output from pins.

PAL (double-speed HSYNC input) Vertical Direction Timing Chart

VP1, 2, 3, 4: LLLH VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLLLLLL VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLHLLLL

MA: H SL3B: L VPOL: H SNSL: H NT-PL: L XHD: H

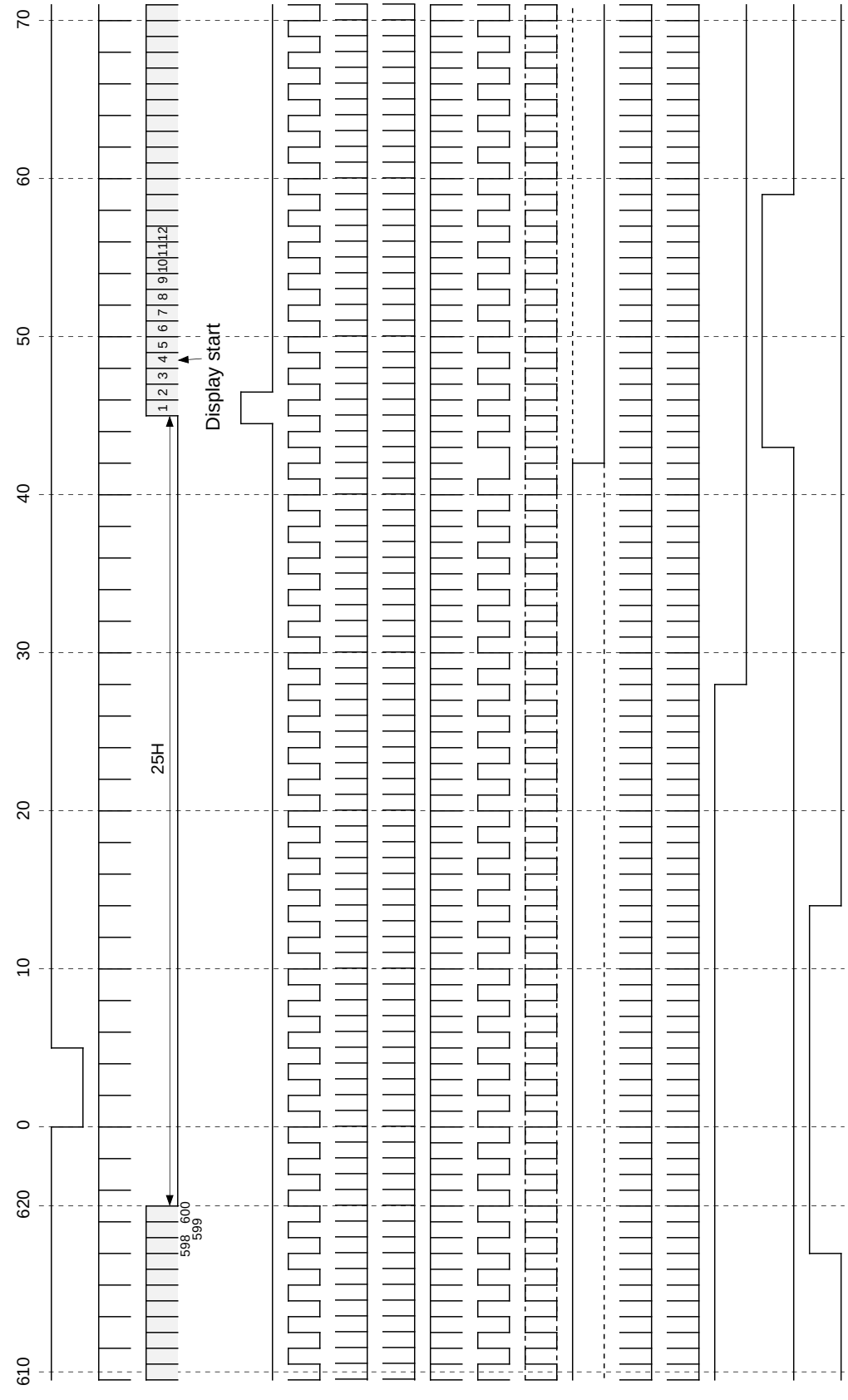


Note) The FRP polarity is not specified for each line and field.
(BLK) in the timing chart is a pulse indicated as a reference and is not a pulse output from pins.

PAL (standard HSYNC input) Vertical Direction Timing Chart

VP1, 2, 3, 4: LLLH VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLLLLLL VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLHLLLL

MA: H SL3B: L VPOL: H SNSL: L NT-PL: L XHD: H

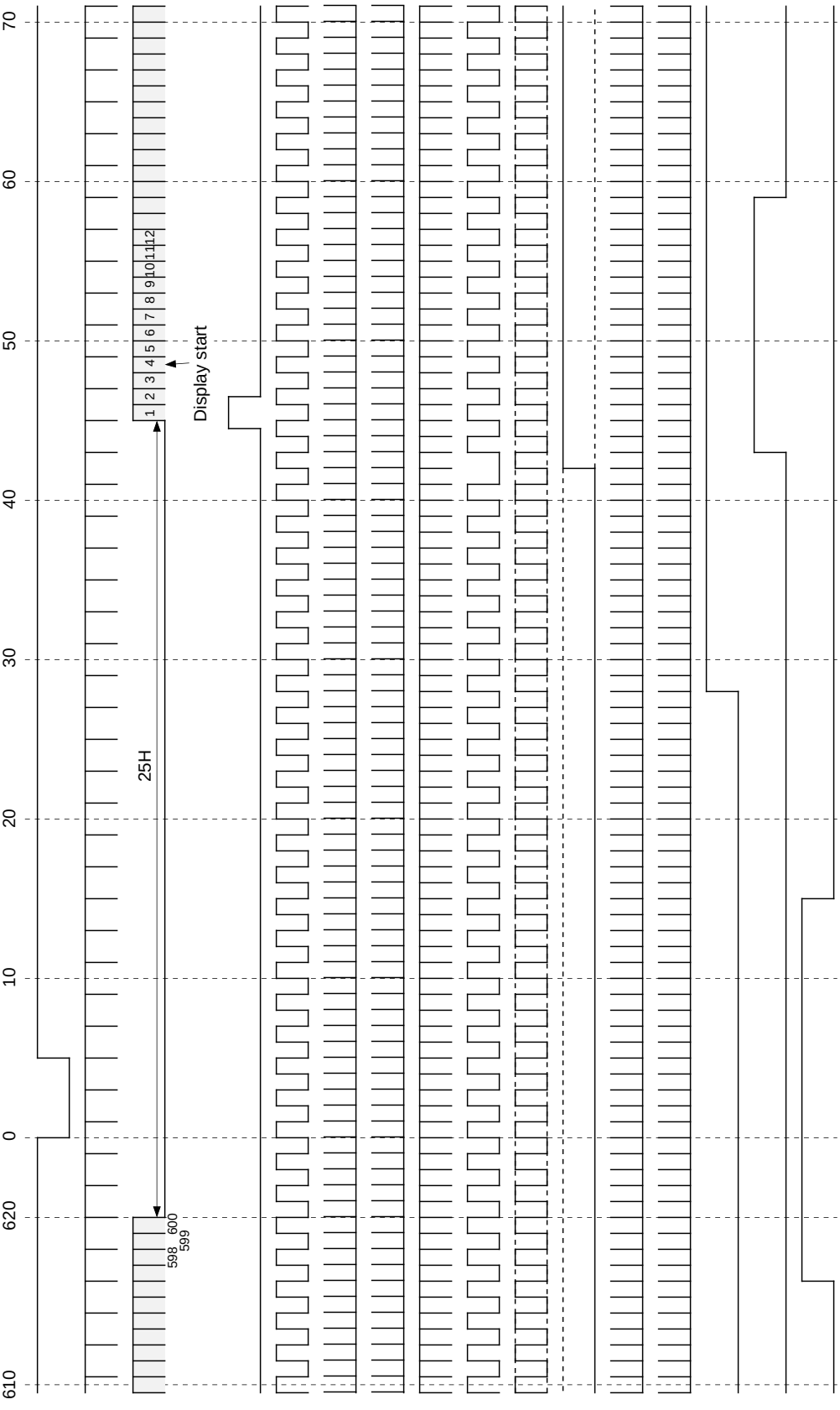


Note) The FRP polarity is not specified for each line and field.
(BLK) in the timing chart is a pulse indicated as a reference and is not a pulse output from pins.

PAL (standard HSYNC input) Vertical Direction Timing Chart

VP1, 2, 3, 4: LLLH VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLLLLLL VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLHLLLL

MA: H SL3B: L VPOL: H SNSL: L NT-PL: L XHD: H

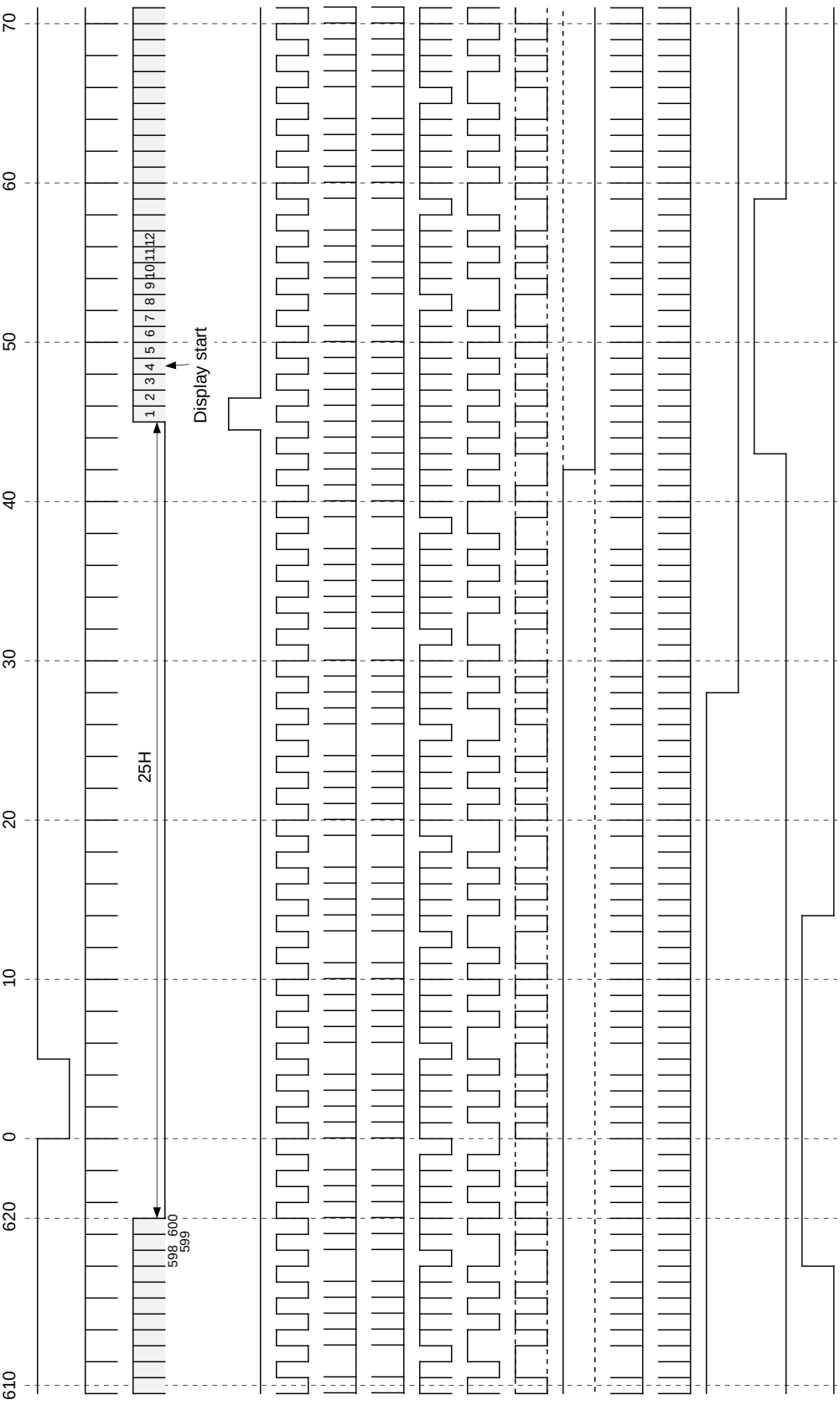


Note) The FRP polarity is not specified for each line and field.
(BLK) in the timing chart is a pulse indicated as a reference and is not a pulse output from pins.

PAL (pulse eliminate display, standard HSYNC input) Vertical Direction Timing Chart

VP1, 2, 3, 4: LLLH VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLLLLLL VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLHLLLL

MA: L SL3B: L VPOL: H SNSL: L NT-PL: L XHD: H

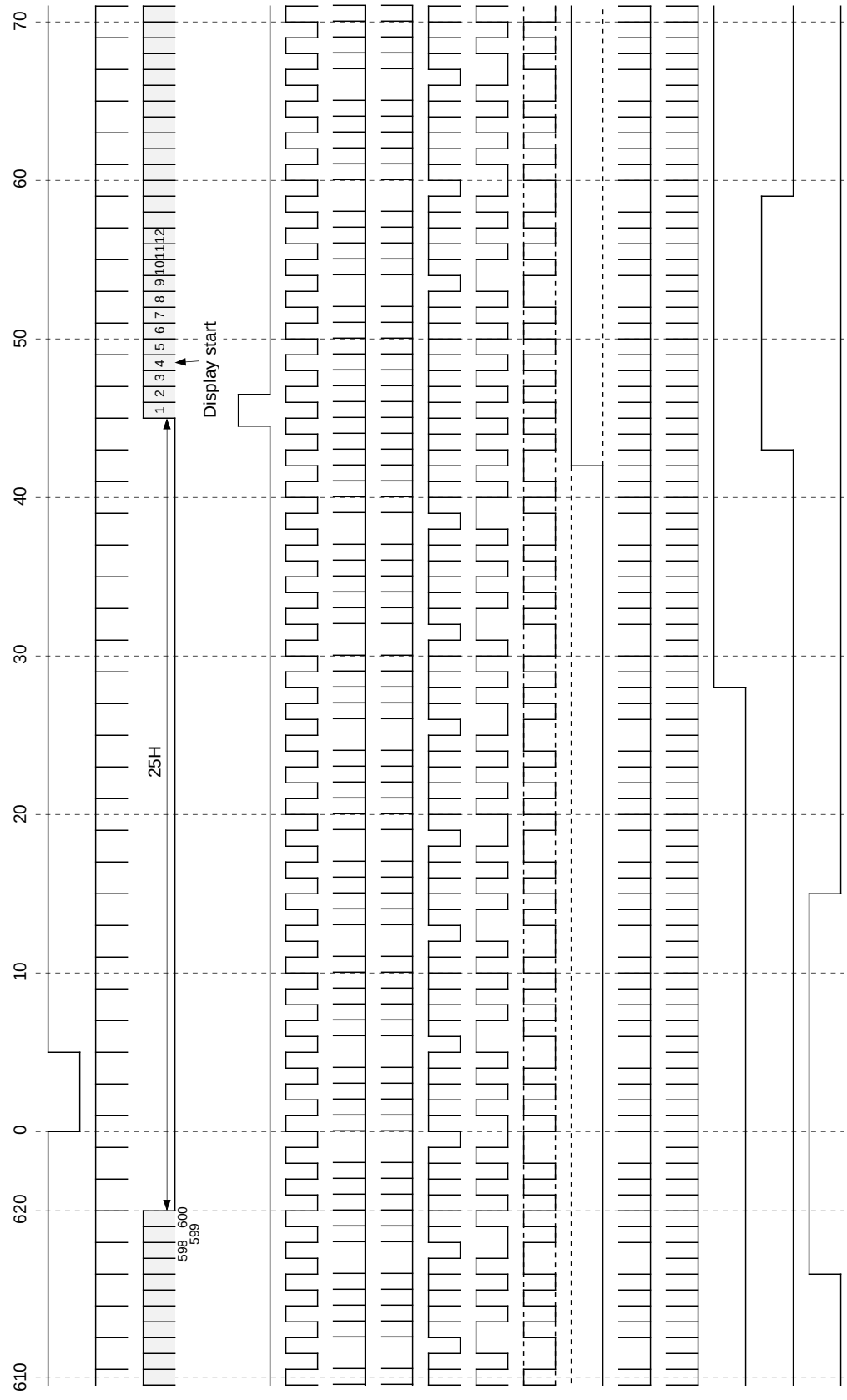


Note) The FRP polarity is not specified for each line and field.
(BLK) in the timing chart is a pulse indicated as a reference and is not a pulse output from pins.

PAL (pulse eliminate display, standard HSYNC input) Vertical Direction Timing Chart

VP1, 2, 3, 4: LLLH VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLLLLLL VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLHLLLL

MA: L SL3B: L VPOL: H SNSL: L NT-PL: L XHD: H

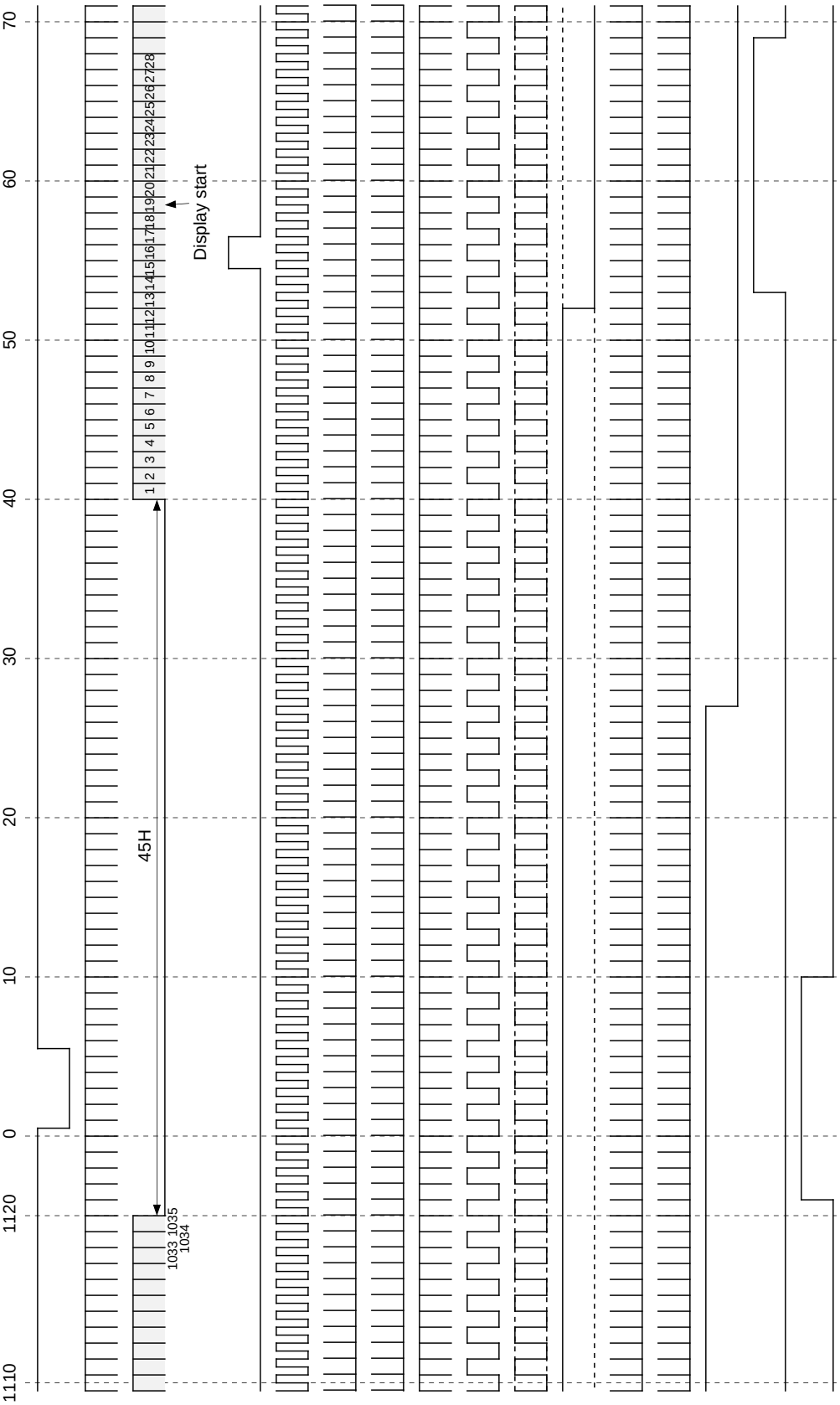


Note) The FRP polarity is not specified for each line and field.
(BLK) in the timing chart is a pulse indicated as a reference and is not a pulse output from pins.

HD Vertical Direction Timing Chart

VP1, 2, 3, 4: LLLH VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLLLLLL VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLHLLLL

MA: H SL3B: L VPOL: H XHD: L

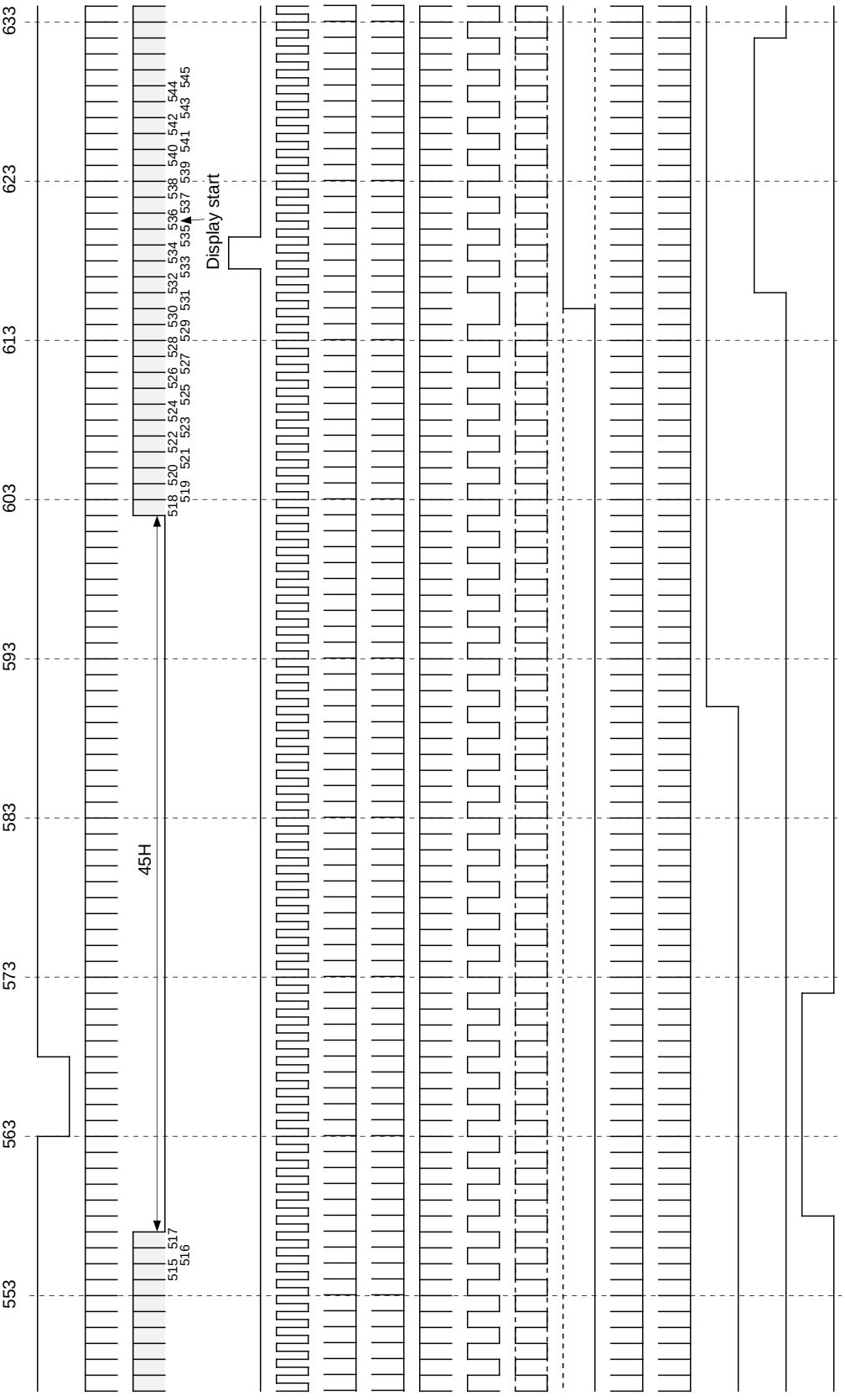


Note) The FRP polarity is not specified for each line and field.
(BLK) in the timing chart is a pulse indicated as a reference and is not a pulse output from pins.

HD Vertical Direction Timing Chart

VP1, 2, 3, 4 : LLLH VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLLLLLL VM0J, 1J, 2J, 3J, 4J, 5J, 6J, 7J, 8J, 9J: LLLLHLLLL

MA: H SL3B: L VPOL: H XHD: L

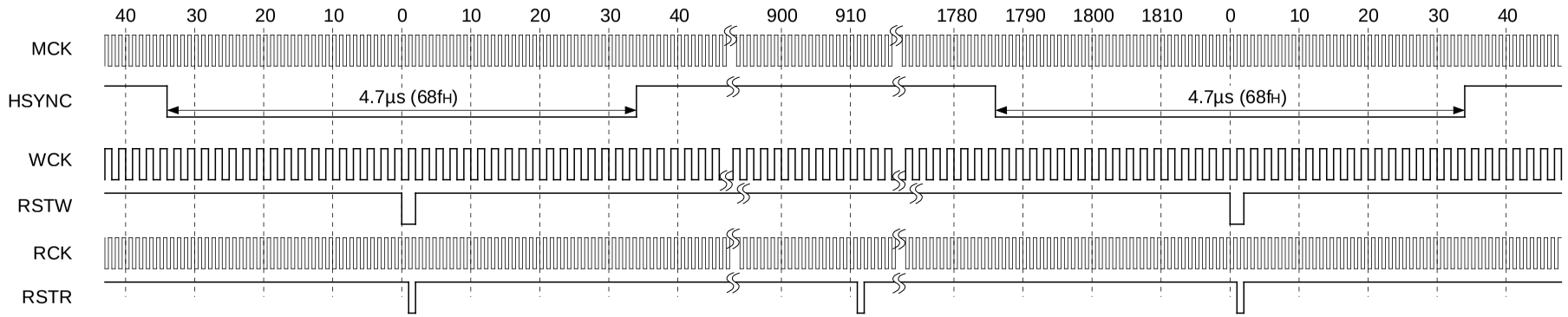


Note) The FRP polarity is not specified for each line and field.
(BLK) in the timing chart is a pulse indicated as a reference and is not a pulse output from pins.

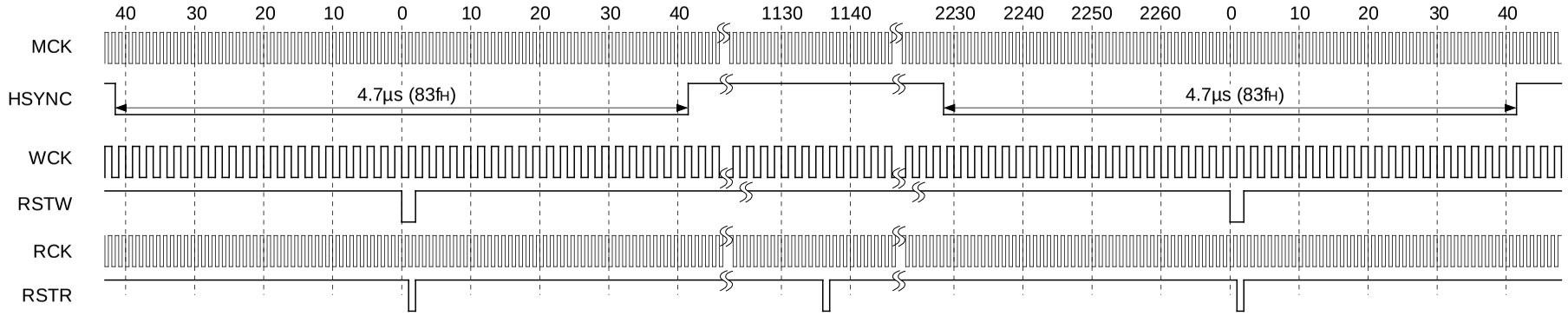
Line Double-Speed Timing Chart

SLBA = L

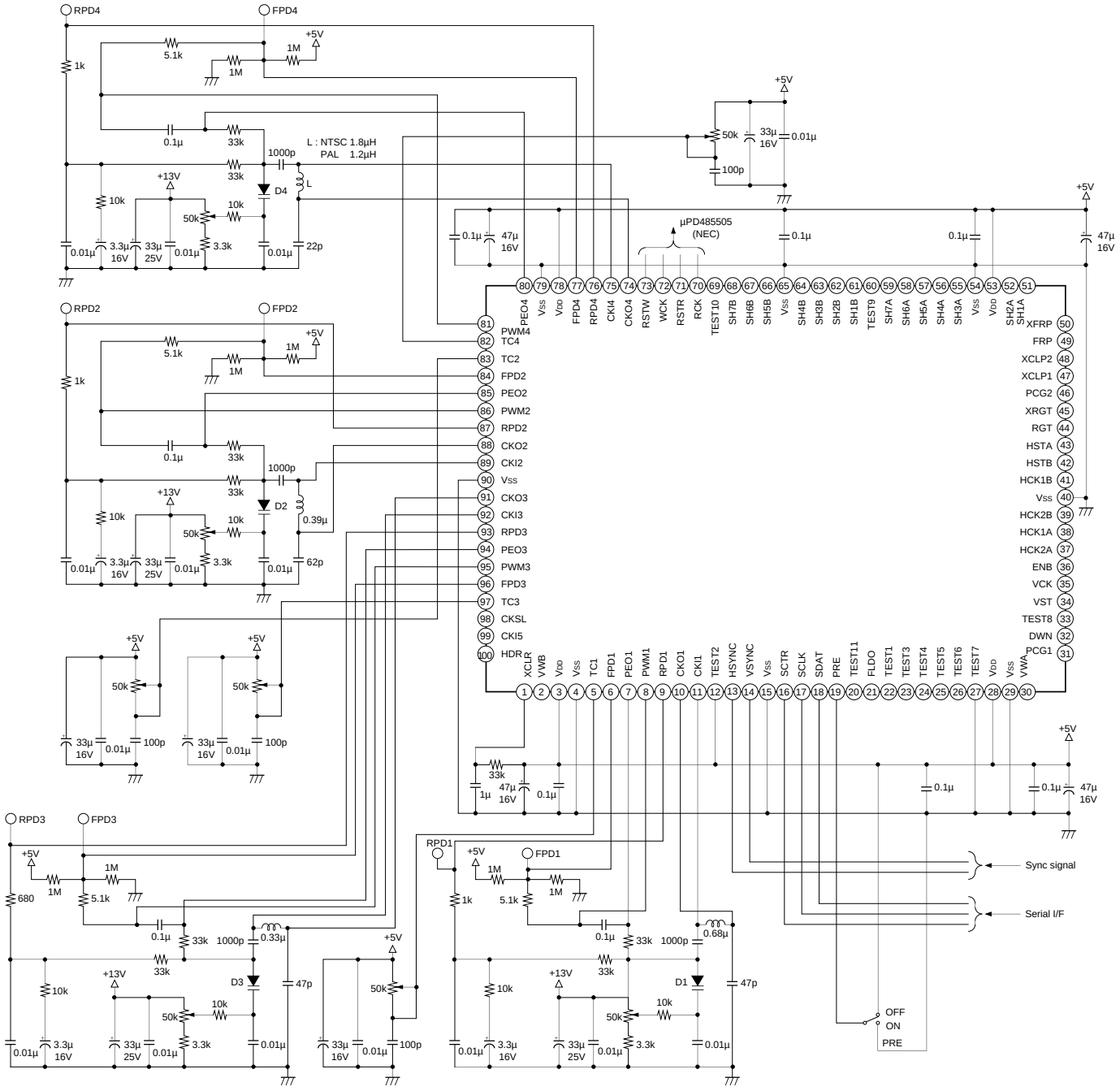
NTSC Loop counter 910f_H, Master Clock 28.6MHz



PAL Loop counter 1135f_H, Master Clock 35.5MHz



Application Circuit

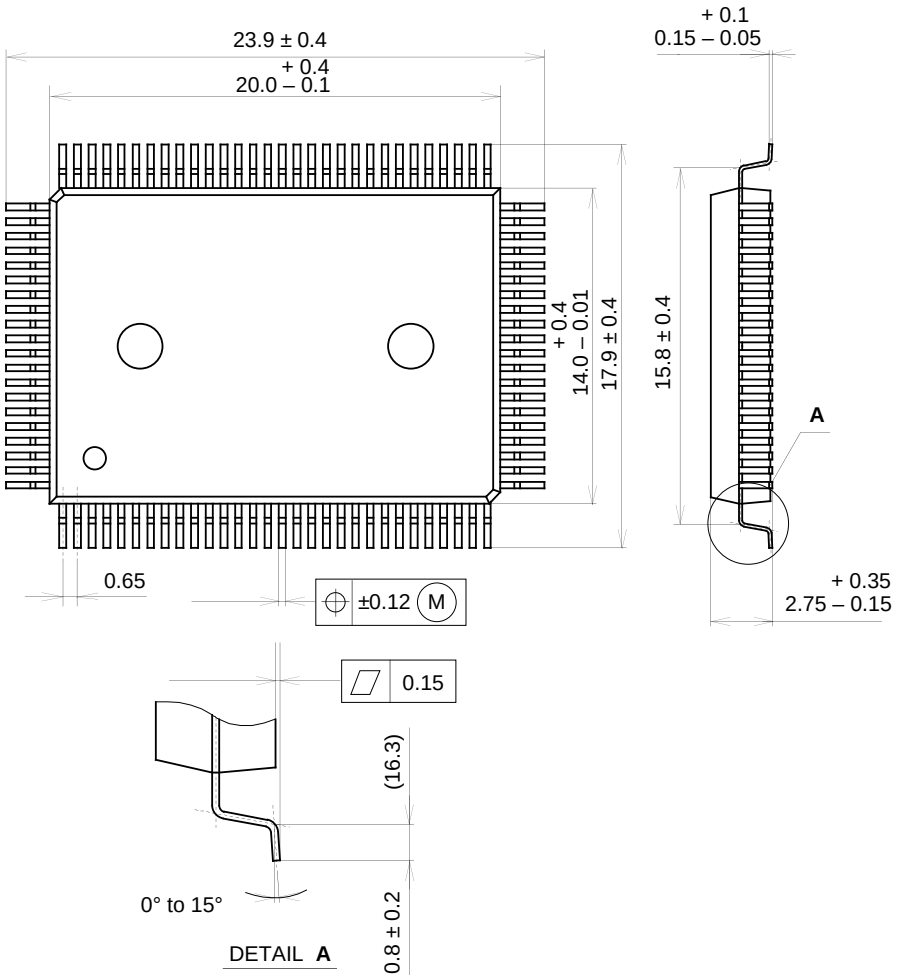


D1, D2, D3, D4 : 1T363A (Sony)

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	∗QFP100-P-1420-A
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g