HYUNDAI

# HY514400 Series

## 1M x 4-bit CMOS DRAM

## DESCRIPTION

The HY514400 is the new generation and fast dynamic RAM organized 1,048,576 x 4 bits. The HY514400 utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY514400 to be packaged in a standard 20/26 pin plastic SOJ.

The package size provides high system bit densities and is compatible with widely available automated-test equipments. System oriented-feature includes single power supply of 5V± 10% tolerence and direct interfacing capability with high performance logic families such as Schottky TTL.

## FEATURES

- **Low power dissipation**
  **Max. CMOS standby 5.5mW**
  **Max. TTL standby 11.0mW**
  **Max. operating**

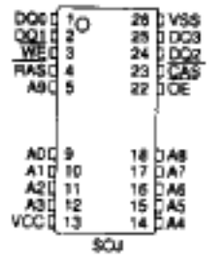
| Speed | Power |
|---|---|
| 70 | 522.5mW |
| 80 | 467.5mW |
| 10 | 412.5mW |

- **Single power supply of 5V± 10%**
- **TTL compatible inputs and outputs**
- **Fast access Time**

| Speed | tRAC | tCAC | tPC |
|---|---|---|---|
| 70 | 70ns | 20ns | 50ns |
| 80 | 80ns | 25ns | 50ns |
| 10 | 100ns | 25ns | 60ns |

- **Fast page mode operation**
- **Multi-bit test capability**
- **Read-Modify-Write capability**
- **CAS-before-RAS, RAS-only, Hidden refresh**
- **1024 refresh cycles / 16ms**

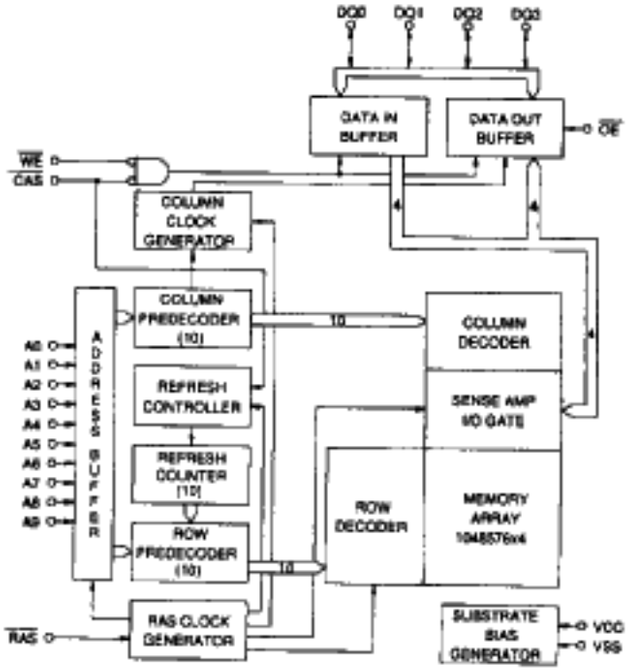
## PIN CONNECTION




## PIN DESCRIPTION

| | |
|---|---|
| RAS | Row Address Strobe |
| CAS | Column Address Strobe |
| WE | Write Enable |
| OE | Output Enable |
| A0-A9 | Address Input |
| DQ0-DQ3 | Data Input/Output |
| Vcc | Power (+ 5V) |
| Vss | Ground |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_A$ | Ambient Temperature | 0 to 70 | °C |
| $T_{STG}$ | Storage Temperature | –55 to 150 | °C |
| $V_{IN}$, $V_{OUT}$ | Voltage on Any Pin Relative to Vss | –1.0 to 7.0 | V |
| $V_{CC}$ | Voltage on Vcc Relative to Vss | –1.0 to 7.0 | V |
| $I_{OS}$ | Short Circuit Output Current | 50 | mA |
| $P_D$ | Power Dissipation | 0.67 | W |
| $T_{SOLDER}$ | Soldering Temperature• Time | 260• 10 | °C• sec |

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

## RECOMMENDED DC OPERATING CONDITIONS

($T_A$= 0°C to 70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | Input High Voltage | 2.4 | - | $V_{CC}$+ 1.0 | V |
| $V_{IL}$ | Input Low Voltage | –1.0 | - | 0.8 | V |

NOTE : All voltages are referenced to Vss.

## DC CHARACTERISTICS

($T_A$= 0°C to 70°C, $V_{CC}$= 5V± 10%, $V_{SS}$= 0V, unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS | SPEED | MIN. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current (Any Input Pins) | $V_{SS} \le V_{IN} \le 6.5V$, All other pins not under test= $V_{SS}$ | | -10 | 10 | µA | |
| $I_{LO}$ | Output Leakage Current (High Impedance State) | $V_{SS} \le V_{OUT} \le 5.5V$, $\overline{RAS}$ & $\overline{CAS}$ at $V_{IH}$ | | -10 | 10 | µA | |
| $I_{CC1}$ | $V_{CC}$ Supply Current, Operating | $t_{RC}$= $t_{RC}$ (min.) | 70<br>80<br>10 | -<br>-<br>- | 95<br>85<br>75 | mA | 1,2,3 |
| $I_{CC2}$ | $V_{CC}$ Supply Current, TTL Standby | $\overline{RAS}$ & $\overline{CAS}$ at $V_{IH}$ | | - | 2 | mA | |
| $I_{CC3}$ | $V_{CC}$ Supply Current, $\overline{RAS}$-only refresh | $t_{RC}$= $t_{RC}$ (min.) | 70<br>80<br>10 | -<br>-<br>- | 95<br>85<br>75 | mA | 1,3 |
| $I_{CC4}$ | $V_{CC}$ Supply Current, Fast Page mode | $t_{PC}$= $t_{PC}$ (min.) | 70<br>80<br>10 | -<br>-<br>- | 80<br>70<br>60 | mA | 1,2,3 |
| $I_{CC5}$ | $V_{CC}$ Supply Current, CMOS Standby | $\overline{RAS}$ & $\overline{CAS}$ ≤ $V_{CC}$-0.2V | | - | 1 | mA | |
| $I_{CC6}$ | $V_{CC}$ Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh | $t_{RC}$= $t_{RC}$ (min.) | 70<br>80<br>10 | -<br>-<br>- | 95<br>85<br>75 | mA | 1,3 |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$= 4.2mA | | - | 0.4 | V | |
| $V_{OH}$ | Output High Voltage | $I_{OH}$= -5mA | | 2.4 | - | V | |

NOTE :

1. $I_{CC1}$, $I_{CC3}$, $I_{CC4}$, and $I_{CC6}$ depend on cycle rate.
2. $I_{CC1}$ and $I_{CC4}$ depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while $\overline{RAS}$= $V_{IL}$ and $\overline{CAS}$= $V_{IH}$.

## AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.) NOTE : 1, 2, 3

| # | SYMBOL | PARAMETER | HY514400J | | | | | | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | -70 | | -80 | | -10 | | | |
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| 1 | tRC | Random Read or Write Cycle Time | 130 | - | 150 | - | 180 | - | ns | |
| 2 | tRWC | Read-Modify-Write Cycle Time | 185 | - | 210 | - | 245 | - | ns | |
| 3 | tPC | Fast Page Mode Cycle Time | 50 | - | 50 | - | 60 | - | ns | |
| 4 | tPRWC | Fast Page Mode Read-Modify-Write Cycle Time | 105 | - | 115 | - | 125 | - | ns | |
| 5 | tRAC | Access Time from $\overline{RAS}$ | - | 70 | - | 80 | - | 100 | ns | 4,9,10 |
| 6 | tCAC | Access Time from $\overline{CAS}$ | - | 20 | - | 25 | - | 25 | ns | 4,9 |
| 7 | tAA | Access Time from Column Address | - | 35 | - | 40 | - | 45 | ns | 4,10 |
| 8 | tCPA | Access Time from $\overline{CAS}$ Precharge | - | 45 | - | 45 | - | 55 | ns | 4 |
| 9 | tCLZ | $\overline{CAS}$ to Output Low Impedance | 0 | - | 0 | - | 0 | - | ns | 4 |
| 10 | tOFF | Output Buffer Turn-off Delay | 0 | 20 | 0 | 20 | 0 | 20 | ns | 5 |
| 11 | tT | Transition Time (Rise and Fall) | 3 | 50 | 3 | 50 | 3 | 50 | ns | 3 |
| 12 | tRP | $\overline{RAS}$ Precharge Time | 50 | - | 60 | - | 70 | - | ns | |
| 13 | tRAS | $\overline{RAS}$ Pulse Width | 70 | 10K | 80 | 10K | 100 | 10K | ns | |
| 14 | tRASP | $\overline{RAS}$ Pulse Width (Fast Page Mode) | 70 | 200K | 80 | 200K | 100 | 200K | ns | |
| 15 | tRSH | $\overline{RAS}$ Hold Time | 20 | - | 25 | - | 25 | - | ns | |
| 16 | tCSH | $\overline{CAS}$ Hold Time | 70 | - | 80 | - | 100 | - | ns | |
| 17 | tCAS | $\overline{CAS}$ Pulse Width | 20 | 10K | 25 | 10K | 25 | 10K | ns | |
| 18 | tRCD | $\overline{RAS}$ to $\overline{CAS}$ Delay | 20 | 50 | 20 | 55 | 25 | 75 | ns | 9 |
| 19 | tRAD | $\overline{RAS}$ to Column Address Delay Time | 15 | 35 | 15 | 40 | 20 | 55 | ns | 10 |
| 20 | tCRP | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 5 | - | 5 | - | 10 | - | ns | |
| 21 | tCP | $\overline{CAS}$ Precharge Time | 10 | - | 10 | - | 10 | - | ns | |
| 22 | tASR | Row Address Set-up Time | 0 | - | 0 | - | 0 | - | ns | |
| 23 | tRAH | Row Address Hold Time | 10 | - | 10 | - | 15 | - | ns | |
| 24 | tASC | Column Address Set-up Time | 0 | - | 0 | - | 0 | - | ns | |
| 25 | tCAH | Column Address Hold Time | 15 | - | 15 | - | 20 | - | ns | |
| 26 | tAR | Column Address Hold Time from $\overline{RAS}$ | 55 | - | 60 | - | 80 | - | ns | |
| 27 | tRAL | Column Address to $\overline{RAS}$ Lead Time | 35 | - | 40 | - | 45 | - | ns | |
| 28 | tRCS | Read Command Set-up Time | 0 | - | 0 | - | 0 | - | ns | |
| 29 | tRCH | Read Command Hold Time Referenced to $\overline{CAS}$ | 0 | - | 0 | - | 0 | - | ns | 6 |
| 30 | tRRH | Read Command Hold Time Referenced to $\overline{RAS}$ | 0 | - | 0 | - | 0 | - | ns | 6 |
| 31 | tWCH | Write Command Hold Time | 15 | - | 15 | - | 20 | - | ns | |
| 32 | tWCR | Write Command Hold Time from $\overline{RAS}$ | 55 | - | 60 | - | 80 | - | ns | |
| 33 | tWP | Write Command Pulse Width | 15 | - | 15 | - | 20 | - | ns | |
| 34 | tRWL | Write Command to $\overline{RAS}$ Lead Time | 20 | - | 25 | - | 25 | - | ns | |
| 35 | tCWL | Write Command to $\overline{CAS}$ Lead Time | 20 | - | 25 | - | 25 | - | ns | |
| 36 | tDS | Data-In Set-up Time | 0 | - | 0 | - | 0 | - | ns | 7 |
| 37 | tDH | Data-In Hold Time | 15 | - | 15 | - | 20 | - | ns | 7 |
| 38 | tDHR | Data-In Hold Time Referenced to $\overline{RAS}$ | 55 | - | 60 | - | 80 | - | ns | |
| 39 | tREF | Refresh Period (1024 cycles) | - | 16 | - | 16 | - | 16 | ms | |
| 40 | tWCS | Write Command Set-up Time | 0 | - | 0 | - | 0 | - | ns | 8 |

## AC CHARACTERISTICS

(continued)

| # | SYMBOL | PARAMETER | HY514400J | | | | | | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | -70 | | -80 | | -10 | | | |
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| 41 | tCWD | $\overline{CAS}$ to $\overline{WE}$ Delay Time | 50 | - | 55 | - | 60 | - | ns | 8 |
| 42 | tRWD | $\overline{RAS}$ to $\overline{WE}$ Delay Time | 100 | - | 110 | - | 135 | - | ns | 8 |
| 43 | tAWD | Column Address to $\overline{WE}$ Delay Time | 65 | - | 70 | - | 80 | - | ns | 8 |
| 44 | tCSR | $\overline{CAS}$ Set-up Time (CBR Cycle) | 10 | - | 10 | - | 10 | - | ns | |
| 45 | tCHR | $\overline{CAS}$ Hold Time (CBR Cycle) | 30 | - | 30 | - | 30 | - | ns | |
| 46 | tRPC | $\overline{RAS}$ to $\overline{CAS}$ Precharge Time | 0 | - | 0 | - | 0 | - | ns | |
| 47 | tCPT | $\overline{CAS}$ Precharge Time (CBR Counter Test) | 40 | - | 40 | - | 50 | - | ns | |
| 48 | tROH | $\overline{RAS}$ Hold Time Referenced to $\overline{OE}$ | 10 | - | 10 | - | 20 | 20 | ns | |
| 49 | tOEA | $\overline{OE}$ Access Time | - | 20 | - | 20 | - | 25 | ns | |
| 50 | tOED | $\overline{OE}$ to Data Delay | 20 | - | 20 | - | 25 | - | ns | |
| 51 | tOEZ | Output Buffer Turn Off Delay Time from $\overline{OE}$ | 0 | 20 | 0 | 20 | 0 | 20 | ns | 5 |
| 52 | tOEH | $\overline{OE}$ Command Hold Time | 20 | - | 20 | - | 25 | - | ns | |
| 53 | tCPWD | $\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge | 10 | - | 10 | - | 10 | - | ns | 8 |
| 54 | tRHCP | $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge | 10 | - | 10 | - | 10 | - | ns | |
| 55 | tWRP | $\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle) | 10 | - | 10 | - | 10 | - | ns | |
| 56 | tWRH | $\overline{WE}$ to $\overline{RAS}$ Hold Time (CBR Cycle) | 10 | - | 10 | - | 10 | - | ns | |
| 57 | tWTS | Write Command Set-up Time (Test Mode In) | 70 | - | 75 | - | 85 | - | ns | |
| 58 | tWTH | Write Command Hold Time (Test Mode In) | 40 | - | 45 | - | 50 | - | ns | |

## AC CHARACTERISTICS IN TEST MODE NOTE : 11

| # | SYMBOL | PARAMETER | HY514400J | | | | | | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | -70 | | -80 | | -10 | | | |
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| 1 | tRC | Random Read or Write Cycle Time | 135 | - | 155 | - | 185 | - | ns | |
| 2 | tRWC | Read-Modify-Write Cycle Time | 190 | - | 215 | - | 250 | - | ns | |
| 3 | tPC | Fast Page Mode Cycle Time | 55 | - | 55 | - | 65 | - | ns | |
| 4 | tPRWC | Fast Page Mode Read-Modify-Write Cycle Time | 110 | - | 120 | - | 130 | - | ns | |
| 5 | tRAC | Access Time from $\overline{RAS}$ | - | 75 | - | 85 | - | 105 | ns | 4,9,10 |
| 6 | tCAC | Access Time from $\overline{CAS}$ | - | 25 | - | 30 | - | 30 | ns | 4,9 |
| 7 | tAA | Access Time from Column Address | - | 40 | - | 45 | - | 50 | ns | 4,10 |
| 8 | tCPA | Access Time from $\overline{CAS}$ Precharge | - | 50 | - | 50 | - | 60 | ns | 4 |
| 13 | tRAS | $\overline{RAS}$ Pulse Width | 75 | 10K | 85 | 10K | 105 | 10K | ns | |
| 14 | tRASP | $\overline{RAS}$ Pulse Width (Fast Page Mode) | 75 | 200K | 85 | 200K | 105 | 200K | ns | |
| 15 | tRSH | $\overline{RAS}$ Hold Time | 25 | - | 30 | - | 30 | - | ns | |
| 16 | tCSH | $\overline{CAS}$ Hold Time | 75 | - | 85 | - | 105 | - | ns | |
| 17 | tCAS | $\overline{CAS}$ Pulse Width | 25 | 10K | 30 | 10K | 30 | 10K | ns | |
| 27 | tRAL | Column Address to $\overline{RAS}$ Lead Time | 35 | - | 45 | - | 50 | - | ns | |
| 41 | tCWD | $\overline{CAS}$ to $\overline{WE}$ Delay Time | 55 | - | 60 | - | 65 | - | ns | 8 |
| 42 | tRWD | $\overline{RAS}$ to $\overline{WE}$ Delay Time | 105 | - | 115 | - | 140 | - | ns | 8 |
| 43 | tAWD | Column Address to $\overline{WE}$ Delay Time | 70 | - | 75 | - | 85 | - | ns | 8 |
| 49 | tOEA | $\overline{OE}$ Access Time | - | 25 | - | 25 | - | 30 | ns | |
| 50 | tOED | $\overline{OE}$ to Data Delay | 25 | - | 25 | - | 30 | - | ns | |
| 52 | tOEH | $\overline{OE}$ Command Hold Time | 25 | - | 25 | - | 30 | - | ns | |

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode during initialization.
2. AC measurements assume $t_T$= 5ns.
3. $V_{IH}$(min.) and $V_{IL}$(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ and $V_{IL}$.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. $t_{OFF}$(max.) and $t_{OEZ}$ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
8. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.), and $t_{CPWD} \geq t_{CPWD}$(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the $t_{RCD}$(max.) limit insures that $t_{RAC}$(max.) can be met. $t_{RCD}$(max.) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$(max.) limit, then access time is controlled by $t_{CAC}$.
10. Operation within the $t_{RAD}$(max.) limit insures that $t_{RAC}$(max.) can be met. $t_{RAD}$(max.) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$(max.) limit, then access time is controlled by $t_{AA}$.
11. These specifications are applied to the Test Mode.

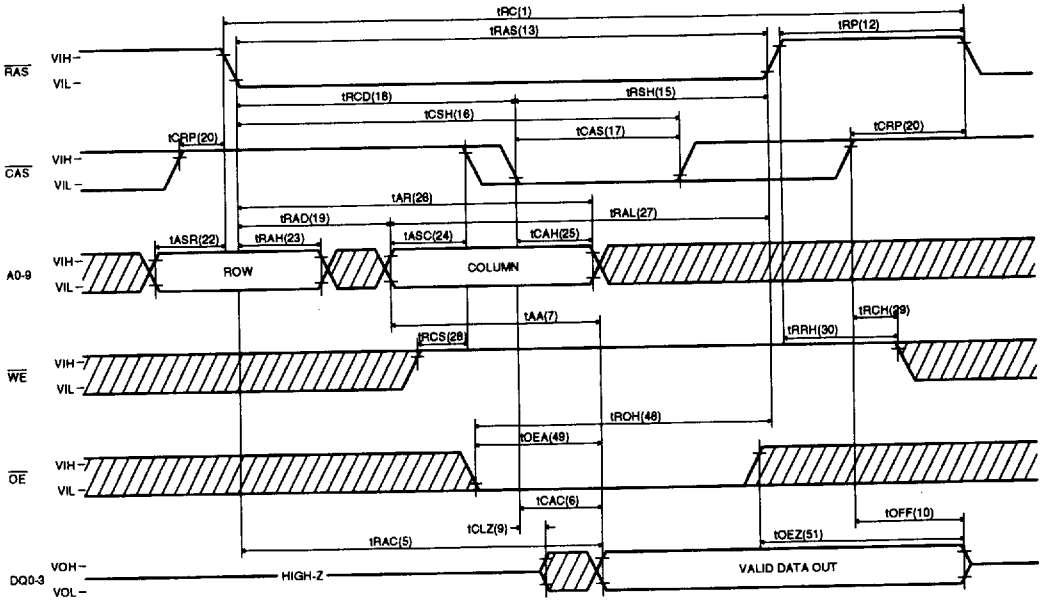
## CAPACITANCE

($T_A$= 25°C, $V_{CC}$= 5V± 10%, $V_{SS}$= 0V, f= 1MHz, unless otherwise noted.)

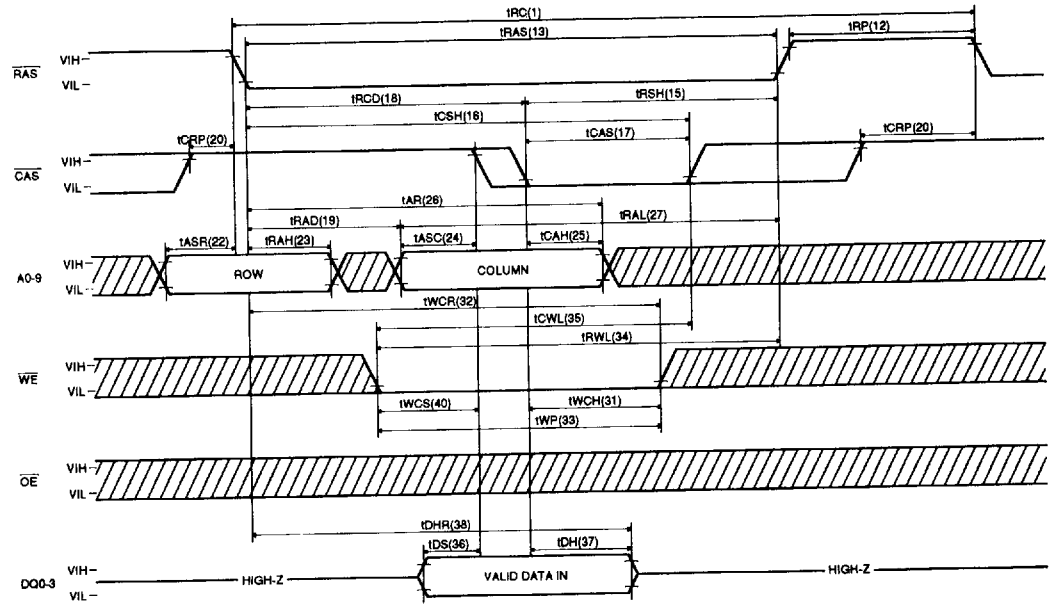
| SYMBOL | PARAMETER | TYP. | MAX. | UNIT |
|---|---|---|---|---|
| $C_{IN1}$ | Input Capacitance (A0-A9, D) | - | 5 | pF |
| $C_{IN2}$ | Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) | - | 7 | pF |
| $C_{OUT}$ | Output Capacitance (Q) | - | 7 | pF |

## TIMING DIAGRAM

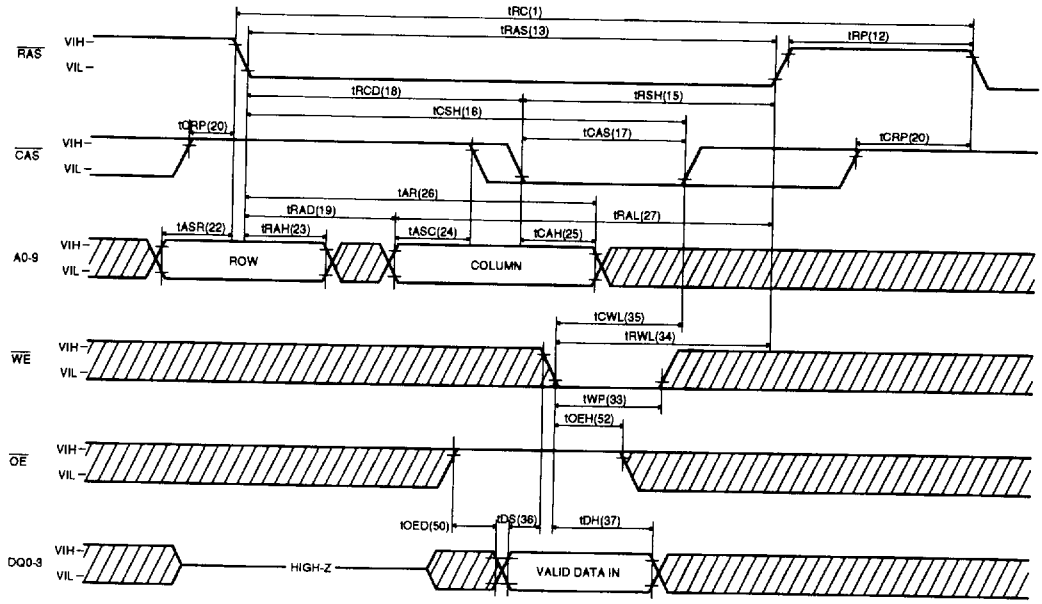
### READ CYCLE



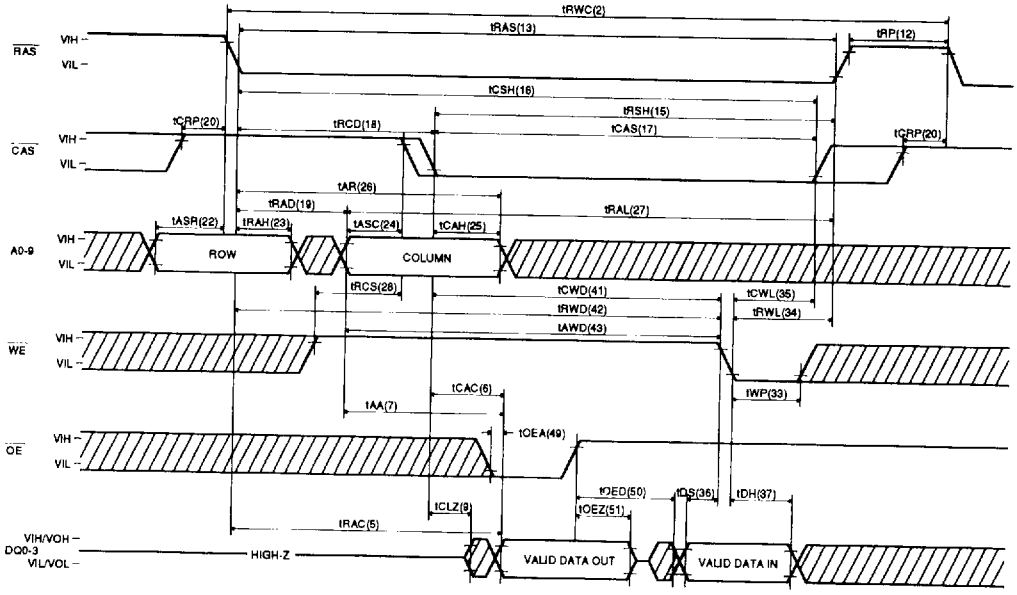

### EARLY WRITE CYCLE



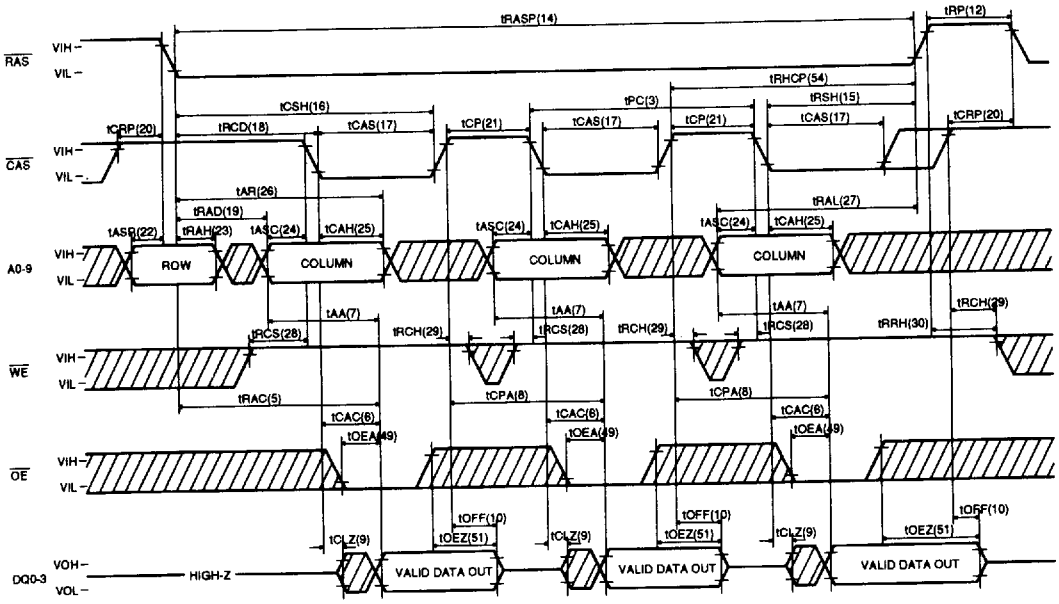
## WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



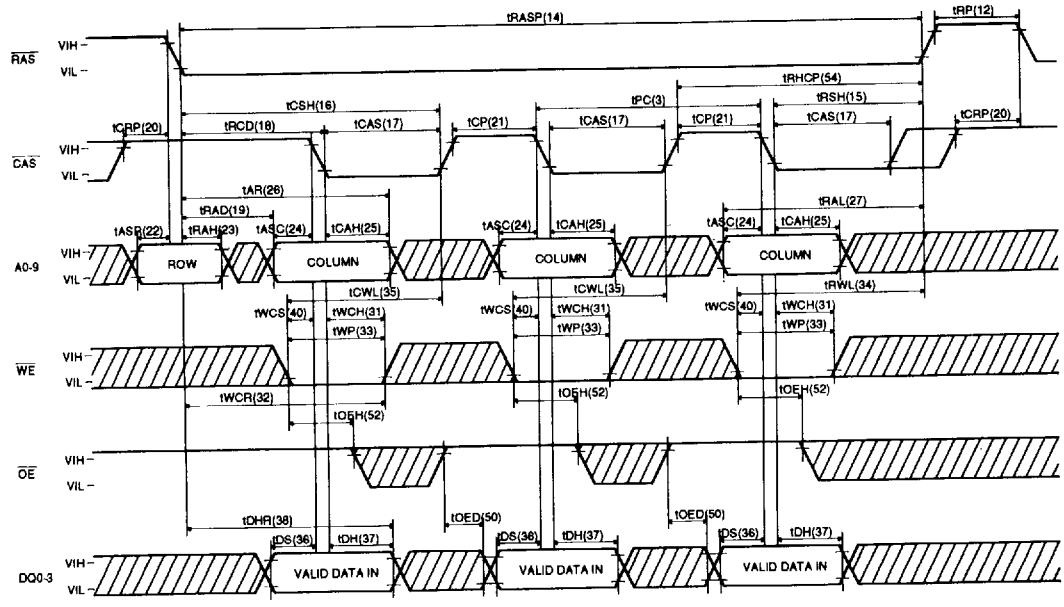

## READ-MODIFY-WRITE CYCLE



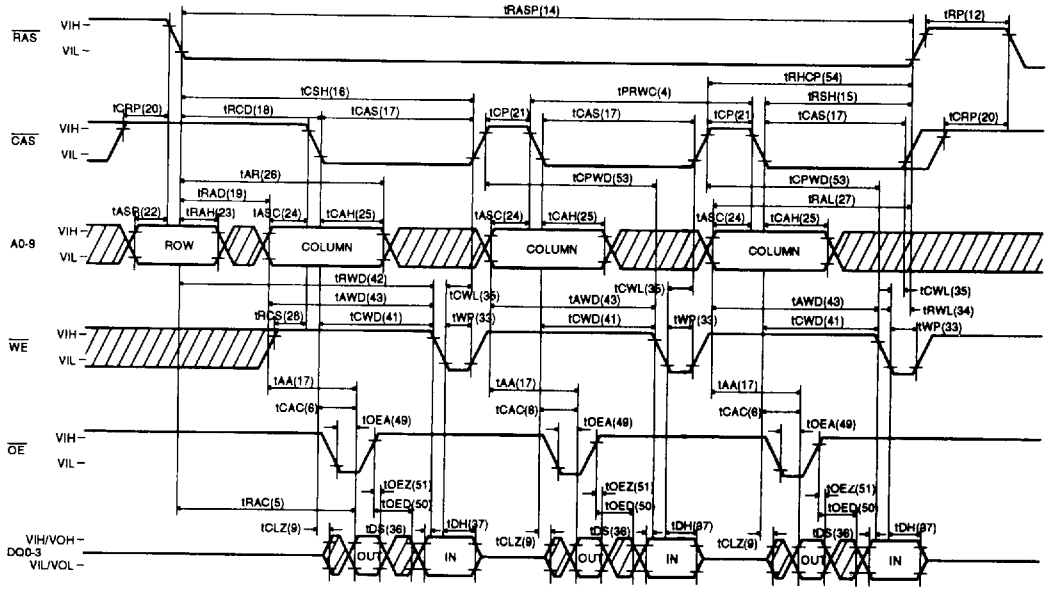
## FAST PAGE MODE READ CYCLE



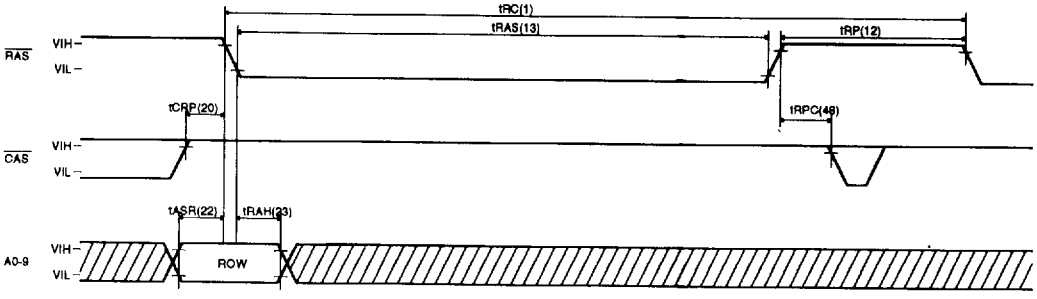

## FAST PAGE MODE EARLY WRITE CYCLE



## FAST PAGE MODE READ-MODIFY-WRITE CYCLE

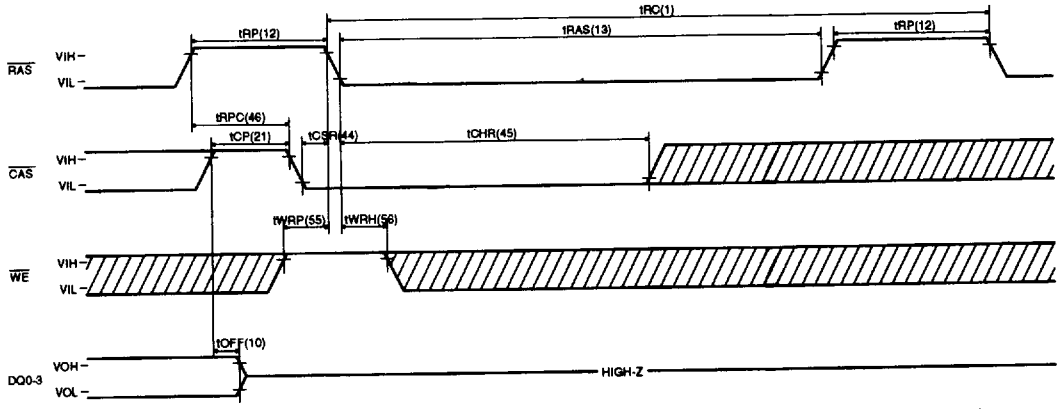



## RAS-ONLY REFRESH CYCLE



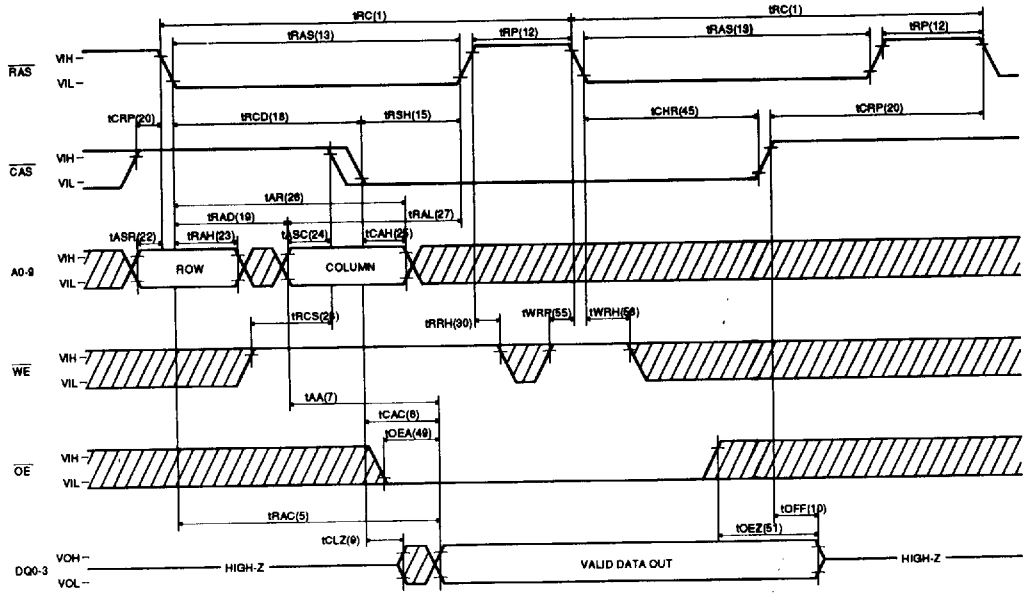

NOTE : $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

## CAS-BEFORE-RAS REFRESH CYCLE

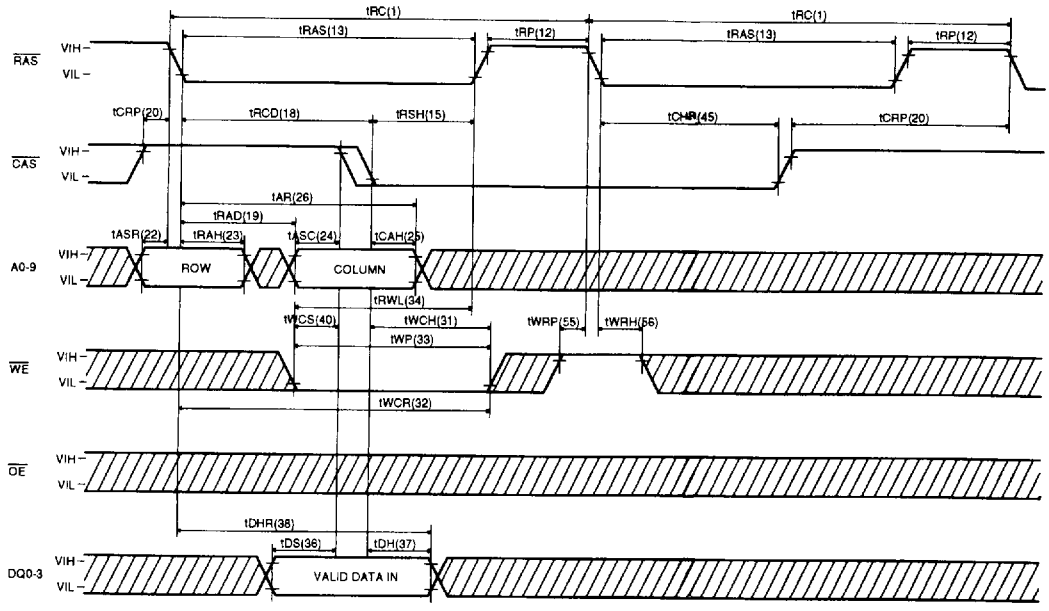



NOTE : A0-9 and $\overline{OE}$ = "H" or "L"

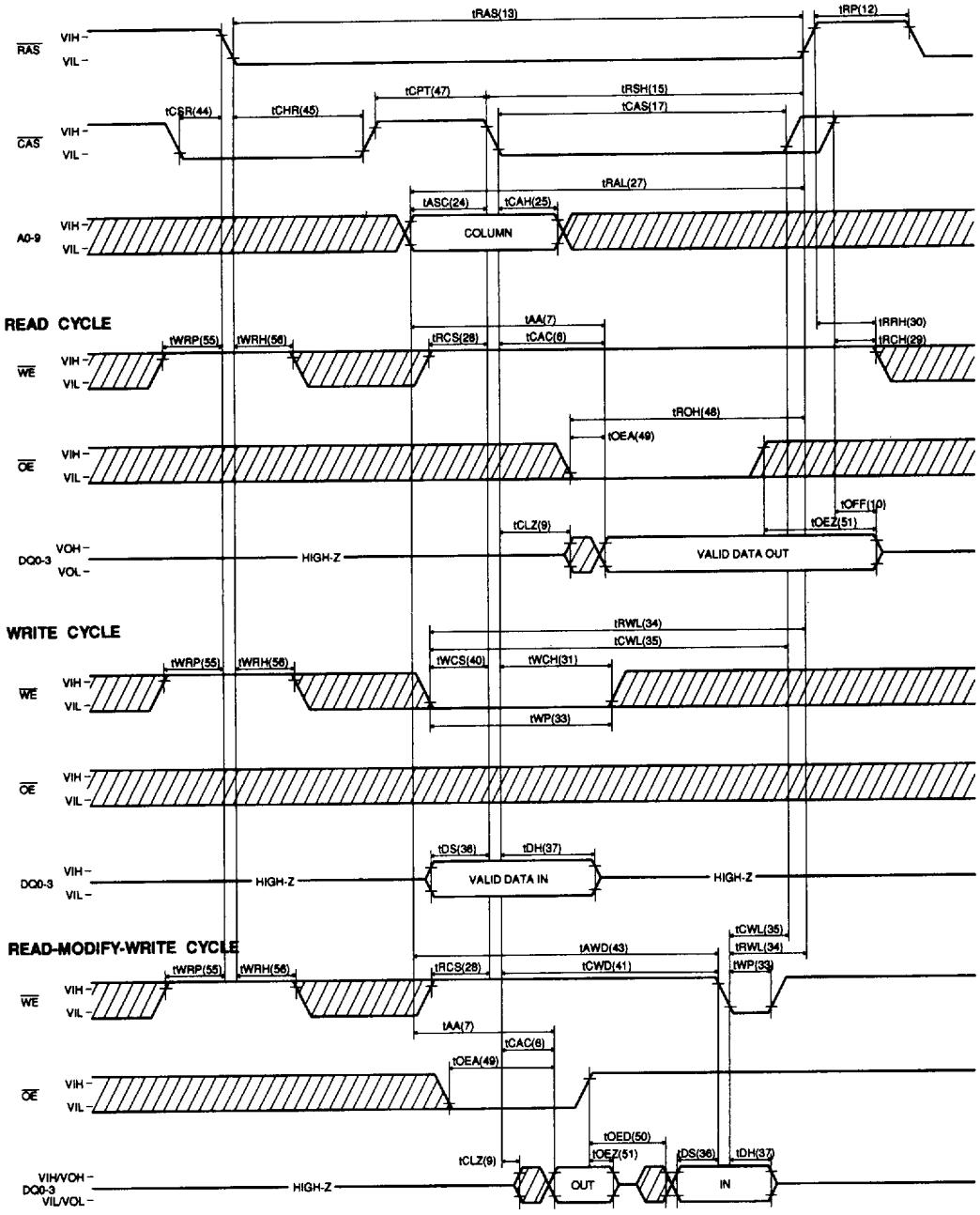
## HIDDEN REFRESH CYCLE (READ)



## HIDDEN REFRESH CYCLE (WRITE)



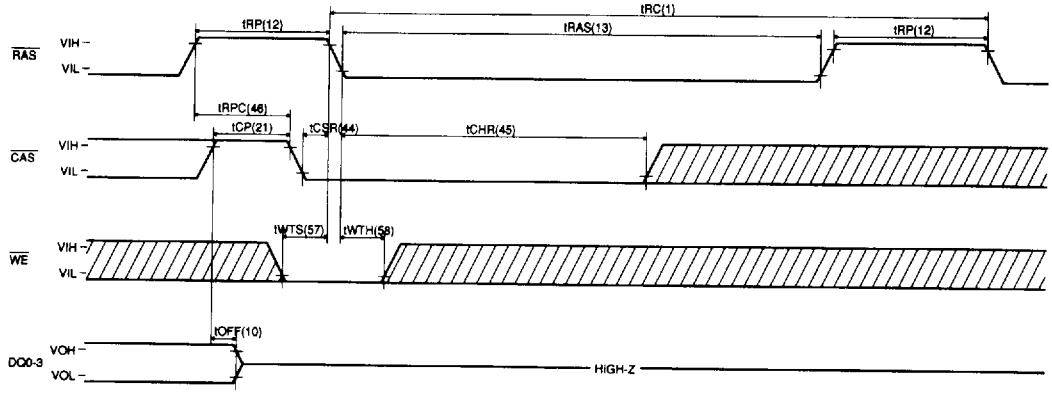
## CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



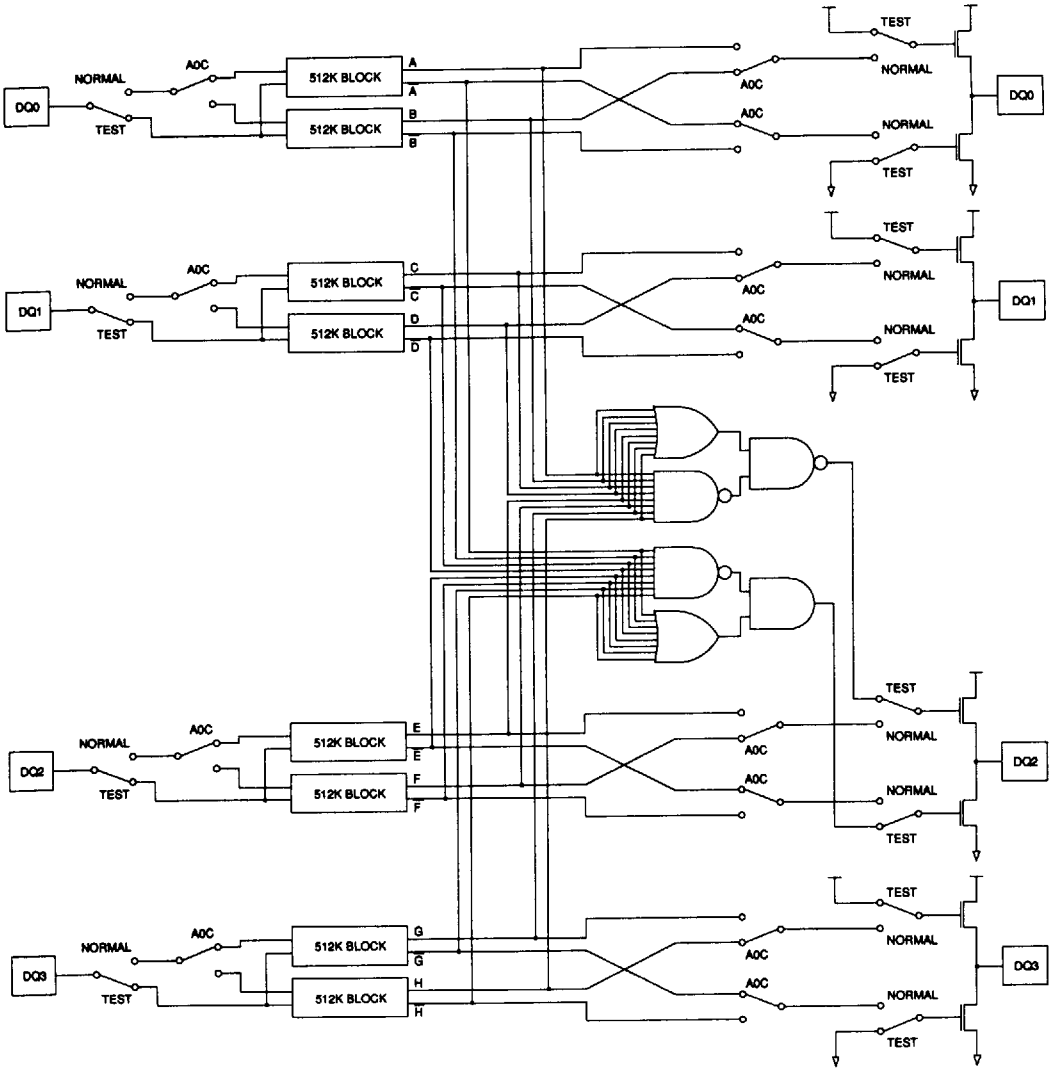
## TEST MODE

The HY514400A is a DRAM organized 1,048,576 x 4-bit. It is internally organized 524,288 x 8-bit. In Test Mode, data are written into 8 sectors (Each is composed of 512K bits) in parallel and retrieved the same way. Column address A0 is not used. If, upon reading, all 8-bit data from 8 sectors are equal (all "1"s or "0"s), the DQ2 pin indicates a "1". If they are not equal, the DQ2 pin indicates a "0". The DQ0, DQ1 and DQ3 pins always indicate a "1" in Test Mode Read cycles. The diagram below shows the timing of the HY514400A to enter Test Mode. In Test Mode, the 1Mx4 DRAM can be tested as if it were a 512Kx4 DRAM. $\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$ cycle (Test Mode In Cycle) puts the HY514400A into Test Mode. $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycle puts it back into Normal Mode. In Test Mode, $\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$ cycle shall be used for the refresh operation. The Test Mode function reduces test time.(1/2 in case of N test pattern)

### TEST MODE IN CYCLE

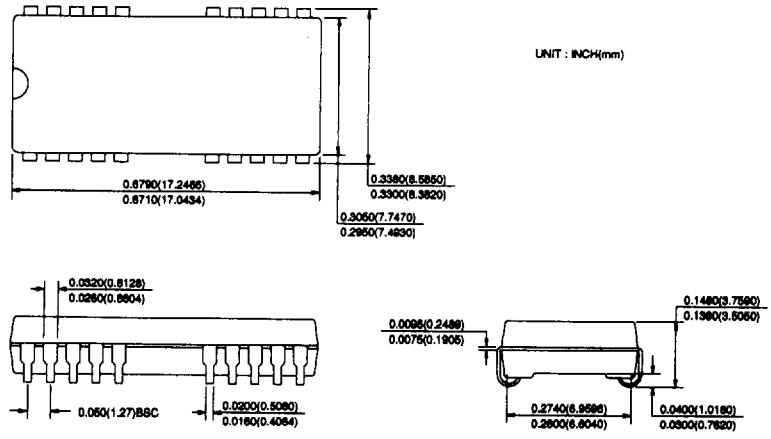


## BLOCK DIAGRAM IN TEST MODE



## PACKAGE INFORMATION

**300 mil 20/26 pin Small Outline J-form Package (J)**



## ORDERING INFORMATION

| PART NO | SPEED | POWER | PACKAGE |
|---|---|---|---|
| HY514400J | 70/80/10 | | SOJ |