PRELIMINARY PRODUCT SPECIFICATION

430MHz-950MHz Single Chip RF Transceiver   nRF903

FEATURES

- True single chip GMSK/GFSK transceiver
- 433MHz, 868MHz and 915MHz LPRD-bands compatible
- Multi-channel operation
- Easy 14-bit configuration
- 0 to 76.8kbit/s data rate
- Reliable communication due to superior adjacent channel selectivity
- No Manchester encoding of data required
- Few external components required
- Standby- and power down-mode

APPLICATIONS

- Alarm and Security Systems
- Automatic Meter Reading (AMR)
- Home Automation
- Remote Control
- Surveillance
- Wireless Handsfree
- Automotive
- Telemetry
- Toys
- Wireless Communications

GENERAL DESCRIPTION

nRF903 is a true single chip multichannel UHF transceiver designed to operate in the unlicensed 433MHz, 868MHz and 915MHz LPRD- (Low Power Radio Device) bands. It features both GMSK (Gaussian Minimum Shift Keying) and GFSK (Gaussian Frequency Shift Keying) modulation and demodulation capability at an effective bit rate of 76.8kbit/s for 153.6kHz channel bandwidths. Transmit power can be adjusted to a maximum of 10dBm. Antenna interface is differential and suited for low cost PCB-antennas. All necessary configuration data is programmed by a 14-bit configuration word via a Serial Peripheral Interface (SPI). Multi-channel operation and excellent receiver selectivity makes nRF903 suitable for wireless links where high-reliability is a key requirement.

nRF903 operates from a single +3V DC supply and features power down- and standby-modes which makes power saving easy and efficient.

As a primary application, the transceiver is intended for UHF radio equipment in compliance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220-1 V1.2.1. and the US Federal Communications Commission (FCC) standard CFR47.

QUICK REFERENCE DATA

| Parameter	Value	Unit
Frequency bands	433.05 - 434.87 868 - 870 902-928	MHz
Bit rate	0 -76.8	kbit/s
Modulation	GMSK/GFSK	
Frequency deviation	±19.2	kHz
Max. RF output power @ 180Ω, 3V	10	dBm
Sensitivity @ 180Ω, BR=76.8 kbit/s, BER<10^{-3}	-100	dBm
Adjacent channel selectivity	>50	dB
Supply voltage	2.7 – 3.3	V
Number of channels	170	-

Table 1. nRF903 quick reference data.

ORDERING INFORMATION

Type number	Description	Version
nRF903-IC	32 pin TQFP	A
nRF903-EVKIT	Evaluation kit with nRF903 IC	1.0

Table 2. nRF903 ordering information.

BLOCK DIAGRAM
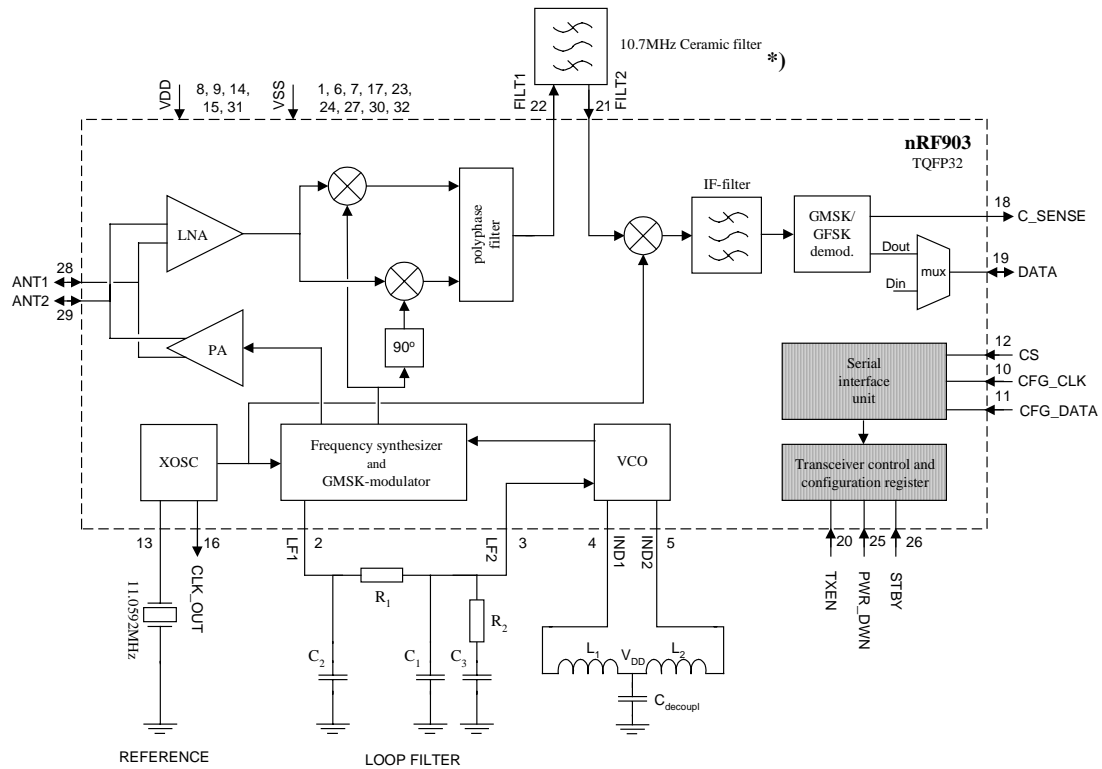
*) The external filter may be replaced with a 10nF capacitor at the expense of receiver performance (see page 13)

Figure 1. nRF903 block diagram with external components.

PRELIMINARY PRODUCT SPECIFICATION

nRF903 Single Chip RF Transceiver

PIN FUNCTIONS

Pin	Name	Pin function	Description
1	VSS	Ground	Ground (0V)
2	LF1	Output	Frequency synthesiser PLL loopfilter connection #1
3	LF2	Input	Frequency synthesiser PLL loopfilter connection #2
4	IND1	Input	External inductor for VCO
5	IND2	Input	External inductor for VCO
6	VSS	Ground	Ground (0V)
7	VSS	Ground	Ground (0V)
8	VDD	Power	Power supply (+3.0V DC)
9	VDD	Power	Power supply (+3.0V DC)
10	CFG_CLK	Input	Clock for programming mode (input)
11	CFG_DATA	Input	Serial input for transceiver configuration data
12	CS	Input	Chip select CS = "0" transceiver normal operating mode CS = "1" transceiver programming mode
13	XC1	Input	Crystal oscillator input (11.0592MHz)
14	VDD	Power	Power supply (+3.0V DC)
15	VDD	Power	Power supply (+3.0V DC)
16	CLK_OUT	Output	Full swing clock for external microcontroller Output frequency is set by 2 bits in the configuration word f_{CLK_OUT}=11.0592MHz/n, where n is 1,2,4 or 8
17	VSS	Ground	Ground (0V)
18	C_SENSE	Output	Carrier sense
19	DATA	Bidirectional	Transmitted/received data
20	TXEN	Input	Select transmit/receive mode TXEN = "0" Receive mode TXEN = "1" Transmit mode
21	FILT2	Input	Input from 1st IF filter (external, 10.7MHz) to IF-amplifier
22	FILT1	Output	IF output to 1st IF filter (external, 10.7MHz)
23	VSS	Ground	Ground (0V)
24	VSS	Ground	Ground (0V)
25	PWR_DWN	Input	Power down mode Refer to Table 5. for mode setup
26	STBY	Input	Standby mode Refer to Table 5. for mode setup
27	VSS	Ground	Ground (0V)
28	ANT1	Bidirectional	Antenna terminal
29	ANT2	Bidirectional	Antenna terminal
30	VSS	Ground	Ground (0V)
31	VDD	Power	Power supply (+3.0V DC)
32	VSS	Ground	Ground (0V)

Table 3. nRF903 pin functions.

nRF903 Single Chip RF Transceiver

ELECTRICAL SPECIFICATIONS

Conditions: VDD = +3V DC, VSS = 0V, T_A= -40°C to +85°C

Symbol	Parameter (condition)	Min.	Typ.	Max.	Units
VDD	Supply voltage	2.7	3	3.3	V
VSS	Ground		0		V
t	Operating temperature range	-40	27	+85	°C
I_{DD}	Total current consumption:				
	Receive mode : 433MHz		18.5		mA
	: 868-928MHz		22.5		mA
	Transmit mode @ -8 dBm RF power : 433MHz		16		mA
	: 868-928MHz		25		mA
	Transmit mode @ 10 dBm RF power : 433MHz		31.5		mA
	: 868-928MHz		41		mA
	Standby mode		200		µA
	Power-down mode			1	µA
#CH	Number of available channels with fixed inductor [1]	170			
	Modulation type		GFSK/GMSK		
Δf	Frequency deviation		±19.2		kHz
BR	Bit rate	0		76.8	kbit/s
t_j	Demodulated data jitter			±2.5	µs
t_{start}	Startup-time			5	ms
$t_{RX/TX}$	Switching time (RX to TX, and TX to RX)			1.5	ms
P_{RF}	Max. RF output power @ 180Ω load		10		dBm
	Sensitivity @ 180Ω, BR=76.8kbit/s, BER < 10^{-3}		-100		dBm
CH_{BW}	Channel spacing		153.6		kHz
f_{res}	Frequency synthesizer resolution		153.6		kHz
ACS	Adjacent channel selectivity (ETSI definition) [2]	50			dB
MIS	Mirror image suppression	28	35		dB
ACP_{GMSK}	Adjacent channel power (76.8kbit/s)			-40	dBc
DR	Dynamic range		90		dB
P_{C_SENSE}	Carrier sense input power trigger level		-106		dBm
f_{IF1}	1st IF frequency		10.7136		MHz
f_{IF2}	2nd IF frequency		345.6		kHz
BW_{IF}	IF noise bandwidth		130		kHz
f_{XTAL}	Crystal frequency		11.0592		MHz
	Crystal reference frequency stability requirement				
	@ 433MHz, BR = 76.8kbit/s			±40	ppm
	@ 868-928MHz, BR = 76.8kbit/s			±20	ppm
f_{uP_CLK}	External micro-controller clock output frequency [3]	1.3824		11.0592	MHz
Z_I	Recommended antenna port differential impedance		180		Ω
	Spurious emission [4]	Compliant with ETSI EN 300-220-1 V1.2.1 And FCC CFR47			

Table 4. nRF0903 electrical specifications.

1): Use must be according to ETSI- and FCC frequency regulations

2): Refer to chapter *Adjacent channel selectivity (ACS)* on page 17 for definition

3): f_{uP_CLK} may be set to 1.3824MHz, 2.7648MHz, 5.5296MHz or 11.0592MHz depending on configuration word

4): Antenna and matching network must be according to recommendations

ABSOLUTE MAXIMUM RATINGS

Supply voltages

VDD... - 0.3V to +6V

VSS 0V

Input voltage

V_I...................................- 0.3V to VDD + 0.3V

Output voltage

V_O ....- 0.3V to VDD + 0.3V

Power dissipation

P_D (T_A=25°C)...300mW

Temperatures

Operating Temperature....... …. -40°C to +85°C

Storage Temperature…... ...... -55°C to +125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!

Electrostatic Sensitive Device

Observe Precaution for handling

PIN ASSIGNMENT
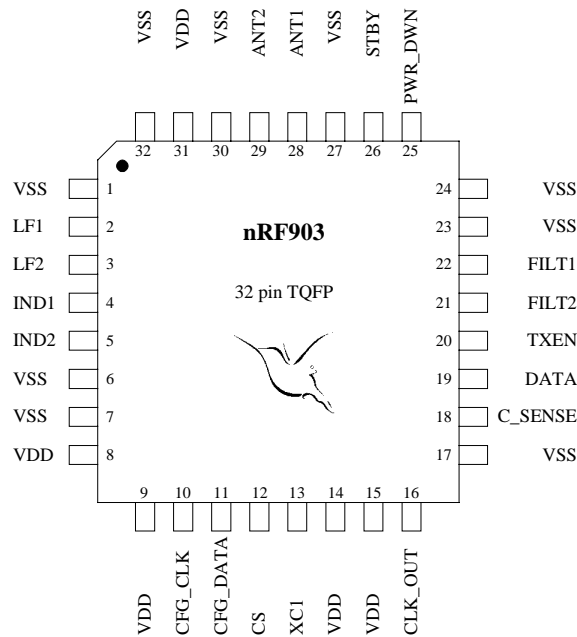
Figure 2. nRF903 pin assignment.

PACKAGE OUTLINE

nRF903, 32 pin TQFP. (Dimensions in mm.)
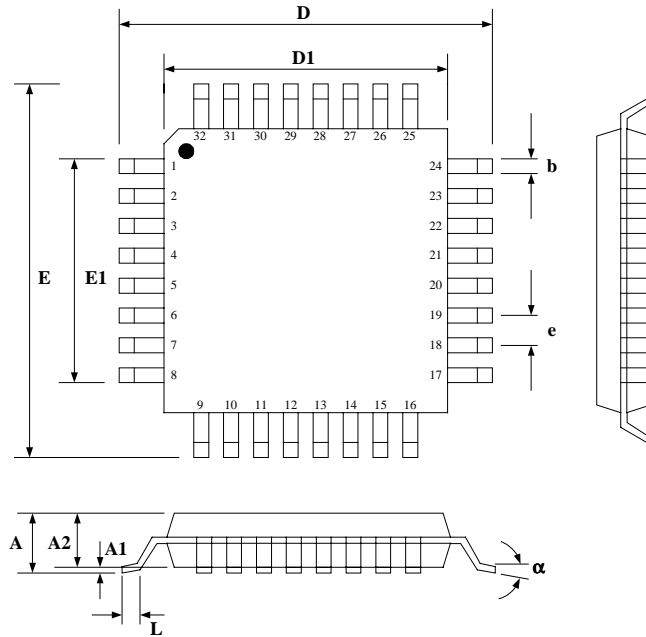
Package Type		E1/D1	E/D	A	A1	A2	e	b	L	α	Copl.
32 pin TQFP	**Min**	7.00	9.00		0.05	1.35	0.80	0.30	0.45	0°	
	Max			1.60	0.15	1.45		0.45	0.75	7°	0.10

Figure 3. TQFP32 Package outline.

APPLICATION INFORMATION

User interface
Figure 4 shows the user interface of nRF903. It consists of a total of 7 digital input/output pins. The interface is divided into two main functions; configuration and mode-control.

In addition to these 7 pins, two extra signals are available; C_SENSE and CLK_OUT.
C_SENSE is '0' when no carrier is detected in the received channel, '1' when a carrier with power level > -106dBm is detected. CLK_OUT is the full-swing 11.0592MHz reference frequency divided by 1,2,4 or 8.
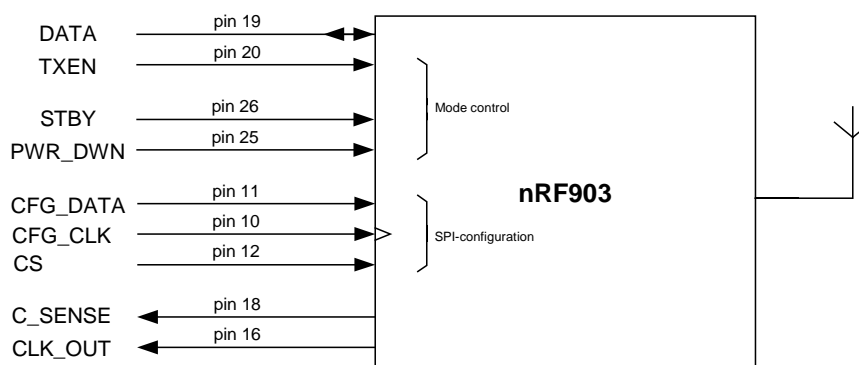
Figure 4. nRF903 user interface

Configuration is performed by clocking a 14-bit configuration word into a shift-register (see Table 6).
These 14 bits are decoded into the corresponding frequency band, channel, output power and output clock frequency. The Serial Peripheral Interface (SPI) consists of the pins CFG_DATA, CFG_CLK and CS. Once configured, these pins are not used unless one or more of the parameters above need to be changed.

Modes of operation
Mode-control is set by the pins TXEN, STBY and PWR_DWN. Table 5 shows the operating mode according to signal settings.

nRF903 operating mode	STBY	PWR_DWN	TXEN
Normal operation: Receive mode	0	0	0
Normal operation: Transmit mode	0	0	1
Power-down mode: No circuitry active	0	1	X
Standby mode: Only XOSC- and Pin 16 (CLK_OUT) active. CLK_OUT frequency is 11.0592MHz before configuration	1	0	X
Default mode∗: SPI-unit override, 868MHz, Receive mode, Channel #0, 1.3824MHz output clock frequency	1	1	0
Default mode∗: SPI-unit override, 868MHz, Transmit mode, Channel #0, 10dBm output power, 1.3824MHz output clock frequency	1	1	1

∗: See chapter *Transceiver configuration*, page 9

Table 5. nRF903 operational mode as a function of external signals STBY, PWR_DWN and TXEN.

Transceiver configuration

A total of 4 parameters are set by the user in an internal 14-bit configuration register. Table 6 shows the contents of the register. Bit 13 is the most significant bit (MSB).

Bit	Parameter	Symbol	Description	#bit
0-1	Frequency band	FB	"00" Frequency band = 433.92 ± 0.87 MHz "01" Frequency band = 869 ± 1 MHz "10" Frequency band = 915 ± 13 MHz "11" Not in use	2
2-9	Channel center position (Channel number)	CH	$f_{centre\_433MHz} = 433.152 \cdot 10^6 + CH \cdot 153.6 \cdot 10^3$ [Hz] $f_{centre\_868MHz} = 868.1856 \cdot 10^6 + CH \cdot 153.6 \cdot 10^3$ [Hz] $f_{centre\_915MHz} = 902.0928 \cdot 10^6 + CH \cdot 153.6 \cdot 10^3$ [Hz]	8
10-11	Output power	P_{OUT}	Output power setting Output power $\approx$ -8dBm + 6dBm $\cdot$ P_{OUT} [dBm]	2
12-13	µP-external clock frequency output	$f_{µP\_clk}$	"00" µP system clock = $f_{X\text{-}tal}$ MHz "01" µP system clock = $f_{X\text{-}tal}$/2 MHz "10" µP system clock = $f_{X\text{-}tal}$/4 MHz "11" µP system clock = $f_{X\text{-}tal}$/8 MHz	2
Total configuration data package size				14

Table 6. nRF903 Configuration word

Transceiver parameters are clocked into the data shift register in the internal configuration unit by using the three-pin serial interface consisting of CS, CFG_CLK and CFG_DATA. Chip select (CS) is used to enable the transceiver configuration mode. Figure 5 illustrates the serial interface block diagram.
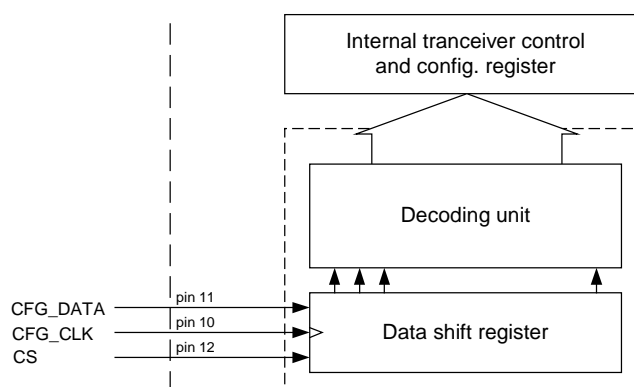

Figure 5. Serial Pheripheral Interface (SPI) for chip configuration

During configuration, CS is activated and the configuration word is clocked in with the MSB first. After the configuration word has been clocked into the shift register, CS is deactivated and the new configuration setup is initialised.

Timing diagram is shown in Figure 6. CFG_DATA bitrate may not exceed 1Mbps.

Once configured, device behaviour is set by the external signals TXEN, PWR_DWN, STBY and DATA (DATA is an input pin in transmit-mode, output in receive-mode).

Configuration may be performed in all modes except standby- and power down mode.

Register contents is still valid after power down and standby mode operation. Configuration data is lost only when supply voltage has been removed.
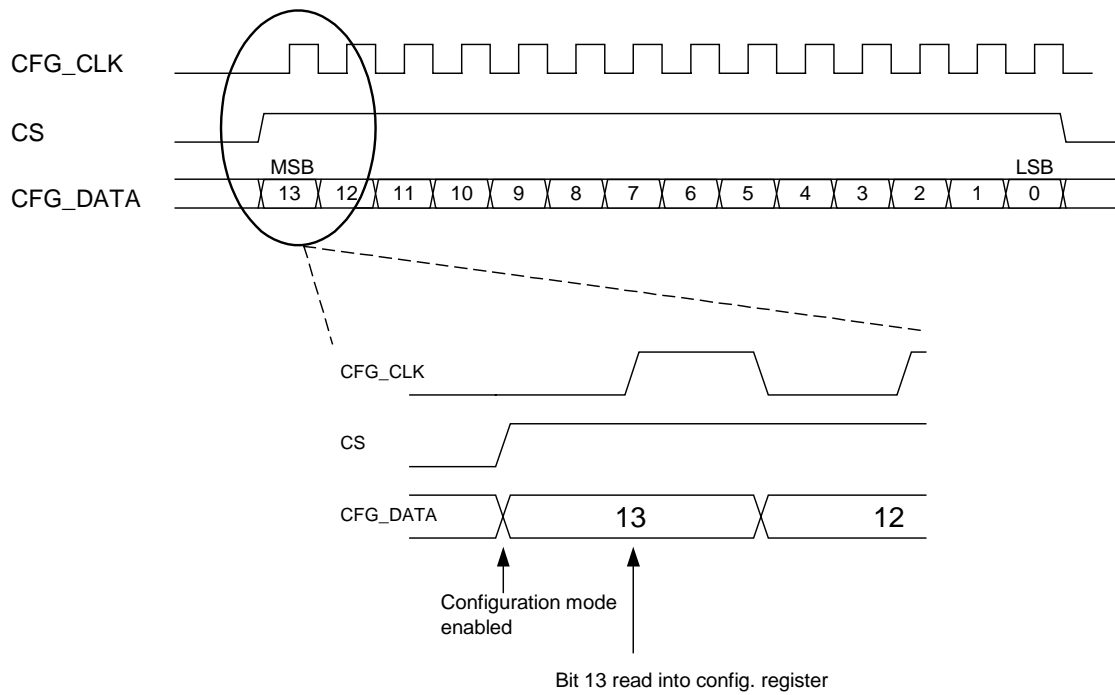

Figure 6. Timing diagram for chip configuration

A preprogrammed channel (868.1856MHz) is available without using the SPI-configuration procedure. While in default mode (ref. Table 5.), the 868.1856MHz channel is activated with maximum power setting and an output clock frequency of 1.3284MHz. This feature has been included to ease debugging of micro-controller software.

Configuration example:

A 868MHz system module is to be designed. The operating channel of the unit is channel #5. The transceiver units are operating within a small confined area. System channel organisation and ETSI frequency allocations are shown in Figure 7.
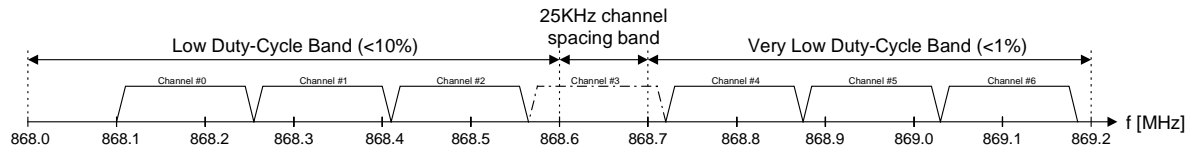

Figure 7. 868MHz LPRD-band, channel organisation

The same crystal is shared by the micro-controller and transceiver. When applying power, nRF903 is set to Standby-mode (STBY = '1', PWR_DWN = '0'), a 11.0592MHz system clock is then available to the micro-controller at the CLK_OUT-pin after 0.9 ms (see Table 13).

The micro-controller then sets the transceiver to normal operation, receive mode (STBY = '0', PWR_DWN = '0', TXEN = '0') for configuration (Receive mode is chosen during configuration in order to avoid unintentional transmission at an unwanted frequency).

The configuration word is calculated as follows (refer to Table 6);

1. Setting frequency band:
   The system operates in the 868MHz LPRD-band, and FB is thus set to 01_b.

2. Calculating channel frequency location:
   The center frequency of Channel #5 is 868.9536MHz.
   CH is found by solving for CH in the equation given in Table 6;
   $$CH = (f_{centre\_868MHz} - 868.1856 \cdot 10^6)/ 153.6 \cdot 10^3$$
   CH=5 (0000101_b)

3. Setting output power
   The operational range is limited, and the output power is therefore reduced to a minimum in order to minimise current consumption in transmit mode. P_{out} is set to 0 (00_b), resulting in an output power of -8dBm.

4. Setting the external microprocessor frequency
   A microprocessor that can perform all system functions at a system clock frequency of at least 4MHz is used. $f_{\mu P\_clk}$ is therefore set to 01_b, resulting in a clock frequency of 5.5296MHz.

   The resulting 14-bit configuration word is then;
   ($01\ 00\ 0000101\ 01_b$) where MSB is the leftmost bit.

The configuration word is clocked in according to Figure 6. On the falling edge of CS, the internal decoding unit sets the frequency synthesiser to the wanted frequency. 4.1ms must be allowed for the synthesiser to stabilise before data may be demodulated (see Table 13).

Timing information

Table 13 contains the critical timing information for the nRF903 transceiver.

The listed values in Table 13 assume the device has been configured. Configuration time is equal to $(14 \cdot 1/f_{CFG\_DATA})$. This time must be added if the device is configured when the operation mode changes below are initiated.

Mode/operation			Max.	Unit
Power down∗	→	Receive	5.0	ms
Standby	→	Receive	4.1	ms
Power down∗	→	Transmit	5.0	ms
Standby	→	Transmit	4.1	ms
Transmit	→	Receive	1.5	ms
Receive	→	Transmit	1.5	ms
Power down∗	→	Standby	0.9	ms
f_{CFG_DATA}			1	MHz
t_{jitter} (Recovered data)			±2.5	μs

*: Same as applying power (VDD) when set to Receive/Transmit/Standby-mode

Table 13. Timing data for nRF903

Power down (Standby) →   Receive:
The time required for correct demodulated data to appear at the DATA-pin when the device is set from power down (standby) mode to receive mode.

Power down (Standby) →   Transmit:
The time required for a correct transmitted data spectrum to appear at the ANT1- and ANT2-pins when the device is set from power down (standby) mode to transmit mode.

Transmit   →   Receive:
The time required for correct demodulated data to appear at the DATA-pin when the device is set from transmit mode to receive mode.

Receive   →   Transmit:
The time required for a correct transmitted data spectrum to appear at the ANT1- and ANT2-pins when the device is set from receive mode to transmit mode.

Power down   →   Standby:
The time required until a stable reference clock signal is available at the CLK_OUT-pin when the device is set from power down mode to standby mode.

f_{CFG_DATA}:
Configuration clock frequency. May be chosen arbitrary.

t_{jitter}:
Transition flank peak jitter of demodulated data

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Antenna input/output

The ANT1 and ANT2 pins provide RF input to the LNA (Low Noise Amplifier) when nRF903 is in receive mode, and RF output from the PA (Power Amplifier) when nRF903 is in transmit mode. The antenna connection to nRF903 is differential and the recommended load impedance at the antenna port is 180Ω.

Figure 14 shows a typical application schematic with a differential loop antenna on a Printed Circuit Board (PCB). The output stage (PA) consists of two open collector transistors in a differential pair configuration. VDD to the PA must be supplied through the collector load. When connecting a differential loop antenna to the ANT1/ANT2 pins, VDD should be supplied through the centre of the loop antenna as shown in Figure 14.

A single ended antenna or 50Ω test instrument may be connected to nRF903 by using a differential to single ended matching network (BALUN) as shown in Figure 8.
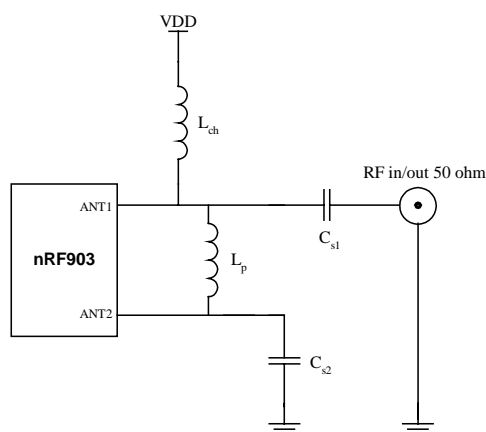
Figure 8. Connecting the nRF903 to a single ended antenna by using a differential to single-ended matching network.

The RF-choke inductor to VDD in Figure 8, needs to have a Self Resonance Frequency (SRF) above the transmit/receive frequency to be effective. Suitable component values are listed in Table 7.

Frequency band [MHz]	L_p [nH]	L_{ch} [nH]	C_{s1} [pF]	C_{s2} [pF]
433.92 ± 0.87	27	68	10	10
869 ± 1 915 ± 13	10	39	3.3	3.3

Table 7. Single-ended matching network components values for nRF903

An additional notch filter (L and C) at the 50Ω RF input/output may be necessary dependent on the application requirements. For 433MHz use, see application note nAN400-05.
(868/915MHz use; application note not currently available)

A single ended antenna may also be connected to nRF903 using an 4:1 impedance RF transformer. The RF transformer must have a centre tap at the primary side for VDD supply.

PLL loop filter

The synthesizer loopfilter is an external, single-ended third order lag-lead filter as shown in Figure 9. The recommended filter component values are listed in Table 8.
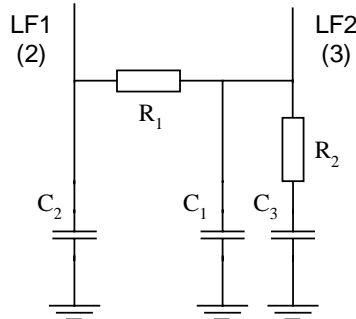

Figure 9. Loopfilter configuration

Frequency band [MHz]	C_1 [pF]	C_2 [pF]	C_3 [nF]	R_1 [kΩ]	R_2 [kΩ]
433.92 ± 0.87	180	12	0.82	1200	180
869 ± 1 915 ± 13	330	22	1.5	560	100

Table 8. Loopfilter components values for nRF903

RF output power

Output power is set by bit 10 and 11 in the configuration word (Ref. Table 6.). A total of 4 different settings are available; 10dBm, 4dBm, -2dBm and -8dBm.

Figure 10 shows the total chip DC current consumption plotted as a function of power level setting and frequency band. Antenna matching according to recommendations is assumed.
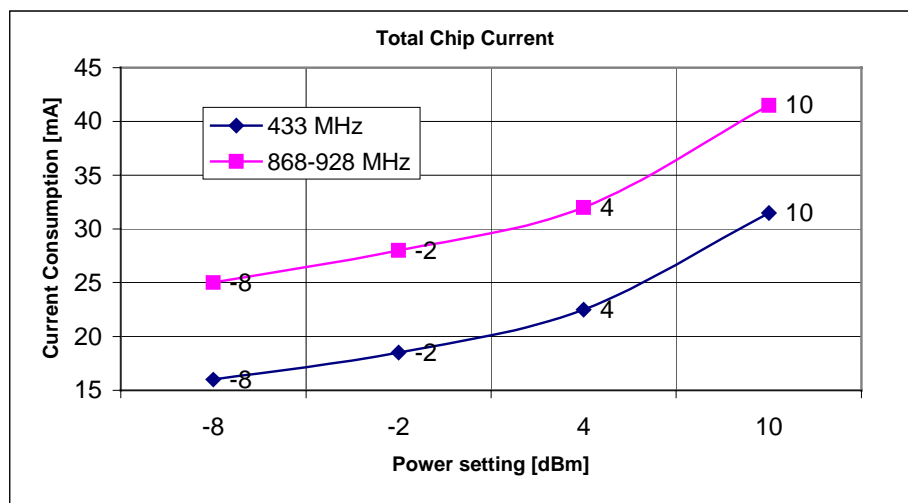

Figure 10. Total current consumption vs. power setting (typical values)

Critical components

Below are listed suggested components and vendors for the most critical external components for nRF903. It should be noted that these are suggestions only, and that other vendors may offer compatible components. Availability, price and delivery times may differ for the different vendors.

Inductors (L$_1$, L$_2$)

Operated in the 433 MHz range, the following 39nH (±2%) inductors (0603) are suitable for use with nRF903.

Vendors	WWW address	Part. no., 39 nH inductors, 0603 size
Pulse	www.pulseeng.com	PE-0603CD390GTT
Coilcraft	www.coilcraft.com	0603CS-39NXGBC
muRata	www.murata.com	LQW1608A39NG00

Table 9a. Vendors and part no. for suitable inductors (433MHz operation).

Operated in the 868/915MHz range, the following 6.8nH inductors (0603) are suitable for use with nRF903. The Pulse and Coilcraft inductors have ±2% tolerance, whilst the Murata inductor has ±0.2nH tolerance.

Vendors	WWW address	Part. no., 6.8 nH inductors, 0603 size
Pulse	www.pulseeng.com	PE-0603CD060GTT
Coilcraft	www.coilcraft.com	0603CS-6N8XGBC
muRata	www.murata.com	LQW1608A6N8C00

Table 9b. Vendors and part no. for suitable inductors (868/915MHz operation).

10.7MHz Ceramic filter

The external 1st IF-filter is a piezoelectric ceramic filter with 330Ω input/output impedance. Center frequency should be positioned at 10.7MHz, and bandwidth should not be less than the channel spacing. 180kHz is a suitable bandwidth. Note that variations in absolute center frequency and bandwidth may differ for different vendors.

Vendors	WWW address	Part. no. 10.7MHz filter, 180kHz bandwidth
muRata	www.murata.com	SFECV10.7MS3S-A-TC (SMD-package)
TDK	www.tdk.co.jp	FFE1070MS (Through-mount)

Table 10. Vendors and part no. for suitable 10.7MHz ceramic filters.

This filter may be replaced with a 10nF capacitor between the FILT1- and FILT2-pins, at the expense of sensitivity (approx. 3dB degradation) and adjacent channel selectivity. In this case, only the internal (second) IF-filter is used. *Note that the image frequency resulting from the second mixing will then appear in the baseband.* This image is centered at 691kHz above the signal of interest.

Table 11 shows the degradation of receiver ACS without the use of the ceramic filter. Degradation will be more evident for channels spaced further from the center channel.

ACS definition	0 ppm frequency offset		20 ppm frequency offset	
	Upper channel [dB]	Lower channel [dB]	Upper channel [dB]	Lower channel [dB]
ETSI	11.3	15.2	7.8	10.8
Real$_*$	0.9	6.2	1.3	4.3

*: 868/915 MHz, GMSK signal, 76.8 kbit/s, 19.2 kHz deviation

Table 11. ACS degradation without external ceramic 10.7 MHz filter (typical)

11.0592MHz Crystal reference

When specifying crystal, keep in mind that the frequency deviation requirement is ±20ppm for 868/915MHz operation and ±40ppm for 433MHz operation. This accounts for both frequency tolerance ($\Delta f/f$) and temperature variations in the crystal frequency.

Example; For a 868MHz system, a crystal frequency tolerance ($\Delta f/f$) of ±15ppm, leaves ±5ppm for drift due to temperature variations.

As temperature characteristics are closely related to crystal cost, it is advisable not to exaggerate the crystal specification. Note that it is *the maximum relative difference between the receiver and transmitter reference frequency* that set the crystal oscillator requirement. If the transmitter and receiver will not be operating at opposite temperature extremes at the same time (maximum difference), the requirements towards temperature characteristics may be relaxed accordingly.

The key parameters for the nRF903 crystal reference is as follows;

f_c=11.0592MHz

$C_{0,max}$=7pF

C_L=12pF (Note that PCB routing load must be included in C_L)

ESR_{max}=60Ω

Vendors	WWW address	Part. no., SMD-package
Epson	www.epson-electronics.de	MA-406H SA-315H / 315HZ
Raltron	www.raltron.com	H10S
Golledge	www.golledge.com	GSX-2
Fox Electronics	www.foxonline.com	FD
Jauch	www.jauch.de	JXS 75

Table 12. Vendors and part no. for suitable 11.0592MHz crystals

Data modulation

The DATA pin is the input to the digital modulator of the transmitter while in TX-mode, and demodulated data output while in receive-mode. The input signal to this pin should be standard CMOS logic levels at data rates up to 76.8kbit/s. No encoding of data is required.

The demodulated digital output data appear at the DATA-pin at standard CMOS logic levels.

nRF903 uses GMSK/GFSK modulation of data for optimum modulation bandwidth efficiency. This type of modulation is an enhanced version of FSK in which each of the two logic levels corresponds to a frequency value;

$$DATA_{FSK} = \text{``1''} \rightarrow f_{'1'} = f_{centre} + \Delta f$$
$$DATA_{FSK} = \text{``0''} \rightarrow f_{'0'} = f_{centre} - \Delta f$$

In Gaussian Frequency Shift Keying (GFSK), the data is filtered through a gaussian filter before modulating the carrier. Figure 11 shows the general principle. This results in a narrower power spectrum of the modulated signal, which in turn allows a higher bitrate to be transfered in the same channel bandwidth. Figure 12 shows the difference between a 76.8kbit/s GMSK- and FSK-spectrum.

Gaussian Minimum Shift Keying (GMSK) is the term used for a GFSK signal where the bitrate is four times the frequency deviation.
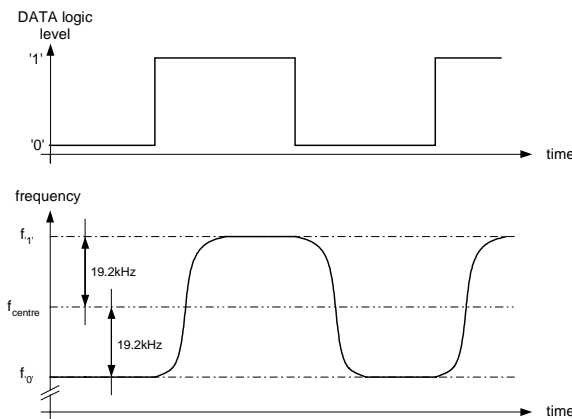

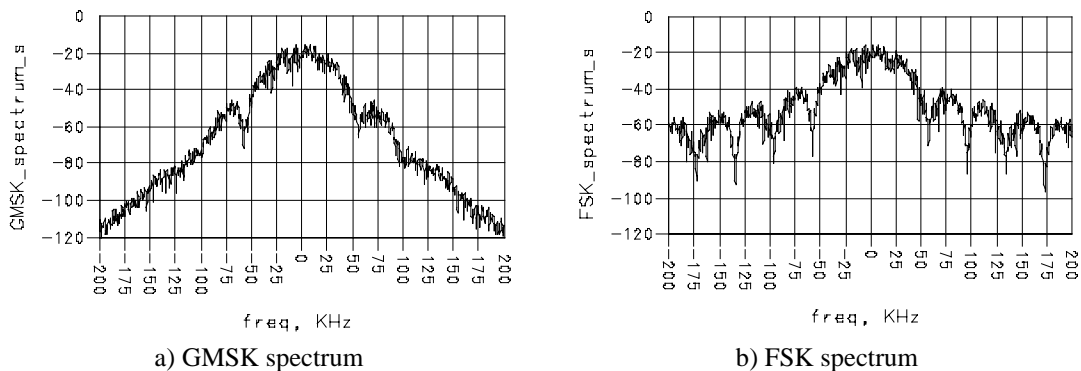Figure 11. Principle of Gaussian filtering of transmitted data

a) GMSK spectrum   b) FSK spectrum

Figure 12. Power Density Spectrum (PDS) of a GMSK- and FSK-signal
($\Delta f = 19.2kHz$, BR = 76.8kbit/s, $BT_{GMSK} = 0.5$)

Mirror image suppression

A cost-saving feature of the nRF903 transceiver is on-chip mirror image cancellation. All heterodyne receivers have a mirror image frequency for a given channel, which may cause in-band interference.

The nRF903 mirror image frequency is always positioned 21.4MHz below the received channel, regardless of channel number or frequency band. As the nRF903 mirror image is attenuated by use of an on-chip quadrature cancellation technique, a costly external SAW/crystal-filter may be avoided.

Typical attenuation of the mirror image frequency is 35dB.

Adjacent channel selectivity (ACS)

nRF903 is a true multi-channel transceiver, enabling simultaneous operation of nRF903 devices in the same environment. This is possible due to high-Q filtering of the received channel to attenuate the interference resulting from neighbouring channels.

Channel filtering is performed by the external 10.7MHz filter combined with an internal band-pass filter.

The adjacent channel selectivity of the receiver is defined by ETSI *as the ability to demodulate a received signal at the sensitivity limit, with the presence of a sine component centered in the adjacent channel* (see Figure 13). Note that the ETSI definition is merely ment as a comparative figure. The *system* ACS is always lower, as the adjacent channel is not likely to be a sine component, but a modulated spectrum.
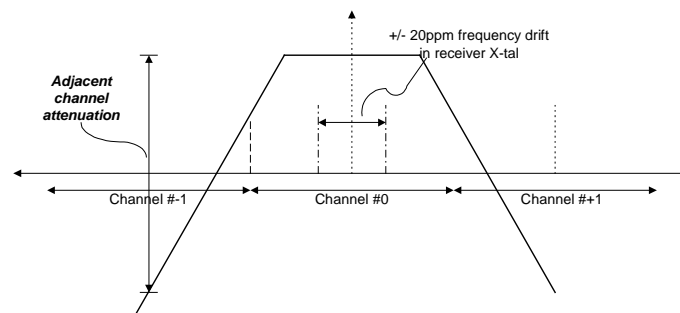

Figure 13. Adjacent channel power attenuation obtained due to IF-filter passband characteristic (ETSI-def.)

For comparison, the adjacent channel selectivity results for the nRF903 receiver is shown in Table 14. Both the upper and lower adjacent channels are listed due to the filter transfer function not being symmetric. If the datarate is reduced, performance will be further enhanced due to reduced bandwidth of the transmitted signal. ACS improves for channels spaced further away from the received channel.

Reference frequency stability is a parameter that influences the resulting ACS. Deviation from the ideal frequency will result in a corresponding deviation of the transmitted center frequency for a transmitter, and an IF offset for the receiver. This will appear as an offset in the the IF-filter center frequency (see Figure 13).

ACS definition	0 ppm frequency offset		20 ppm frequency offset	
	Upper channel [dB]	Lower channel [dB]	Upper channel [dB]	Lower channel [dB]
ETSI	-51.1	-66.4	-40.0	-50.5
Real*	-37.4	-35.0	-27.0	-25.4

*: 868/915MHz, GMSK signal, 76.8kbit/s, 19.2kHz deviation

Table 14. Adjacent channel selectivity for the nRF903 receiver

NOTE:

20ppm frequency deviation corresponds to approx. 20kHz for the 868/915MHz frequency bands, whilst only 10kHz at 433MHz. The ACS-performance listed in Table 14 will thus be much better for 433MHz operation as the channel bandwidth is identical for all three frequency bands. This implies that a ±40ppm crystal may be used for 433MHz operation and still achive the same performance as listed in Table 14.

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APPLICATION SCHEMATIC
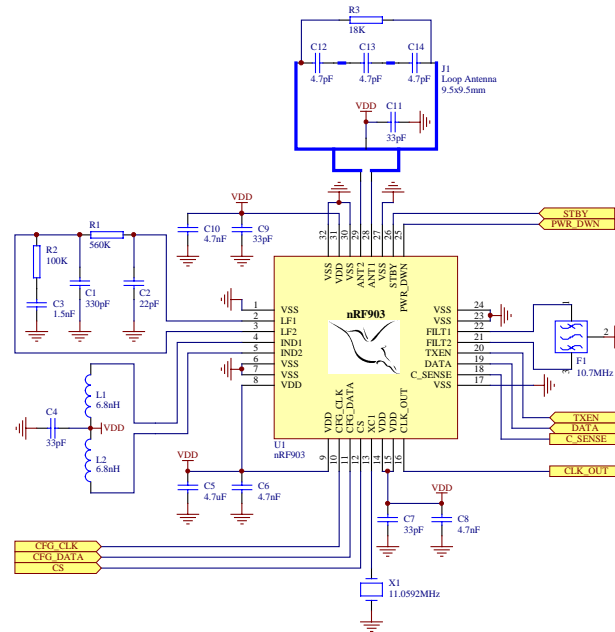
Figure 14. nRF903 application schematic.

Component	Description	Size	Value	Tol.	Units
C1	X7R ceramic chip capacitor, (PLL loop filter); @ 433MHz @ 868-928MHz	0603	330	±10%	pF
C2	X7R ceramic chip capacitor, (PLL loop filter); @ 433MHz @ 868-928MHz	0603	22	±10%	pF
C3	X7R ceramic chip capacitor, (PLL loop filter); @ 433MHz @ 868-928MHz	0603	1.5	±10%	nF
C4	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C5	Tantalum chip capacitor, (Supply decoupling)	3216	4.7	±20%	μF
C6	X7R ceramic chip capacitor, (Supply decoupling)	0603	4.7	±10%	nF
C7	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C8	X7R ceramic chip capacitor, (Supply decoupling)	0603	4.7	±10%	nF
C9	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C10	X7R ceramic chip capacitor, (Supply decoupling)	0603	4.7	±10%	nF
C11	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C12	NP0 ceramic chip capacitor, (Antenna tuning)∗	0603	4.7	±0.1	pF
C13	NP0 ceramic chip capacitor, (Antenna tuning) ∗	0603	4.7	±0.1	pF
C14	NP0 ceramic chip capacitor, (Antenna tuning) ∗	0603	4.7	±0.1	pF
L1	VCO inductor (see critical components section); Q>40 @ 433MHz Q>40 @ 868-928MHz	0603	39 6.8	±2%	nH
L2	VCO inductor (see critical components section); Q>40 @ 433MHz Q>40 @ 868-928MHz	0603	39 6.8	±2%	nH
R1	0.1W chip resistor, (PLL loop filter) @ 433MHz @ 868-928MHz	0603	560	±1%	kΩ
R2	0.1W chip resistor, (PLL loop filter) @ 433MHz @ 868-928MHz	0603	100	±1%	kΩ
R3	0.1W chip resistor, (Antenna Q reduction) ∗	0603	18	±1%	kΩ
F1	Ceramic filter (see critical components section)	-	10.7		MHz
X1	Crystal (see critical components section)	-	11.0592		MHz

Table 15. Recommended External Components.

*: 868MHz operation (For 433MHz and 915MHz use, please refer to application notes nAN400-05 and nAN900-02)

PCB layout and decoupling guidelines

A well-designed PCB is necessary to achieve good RF performance. A PCB with a minimum of two layers including a ground plane is recommended for optimum performance.

The nRF903 DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors, see Table 15. It is preferable to mount a large surface mount capacitor (e.g. 2.2µF ceramic) in parallel with the smaller value capacitors. The nRF903 supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF903 IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes in or close to the VSS pads. Preferably one via hole should be used for each VSS pin.

Full swing digital data or control signals should not be routed close to the PLL loop filter components, the external VCO inductors or the power supply lines.

The VCO inductors placement is important. Optimum placement of the VCO inductors yields a PLL loop filter voltage of 1.1 ± 0.2V, which can be measured at LF2 (pin 3). Figure 15 shows the recommended layout and inductor placement for a PCB compatible with all three frequency bands. For 915MHz operation, the inductors should be placed according to Figure 15 a., and for 433MHz and 868MHz operation as shown in Figure 15 b.
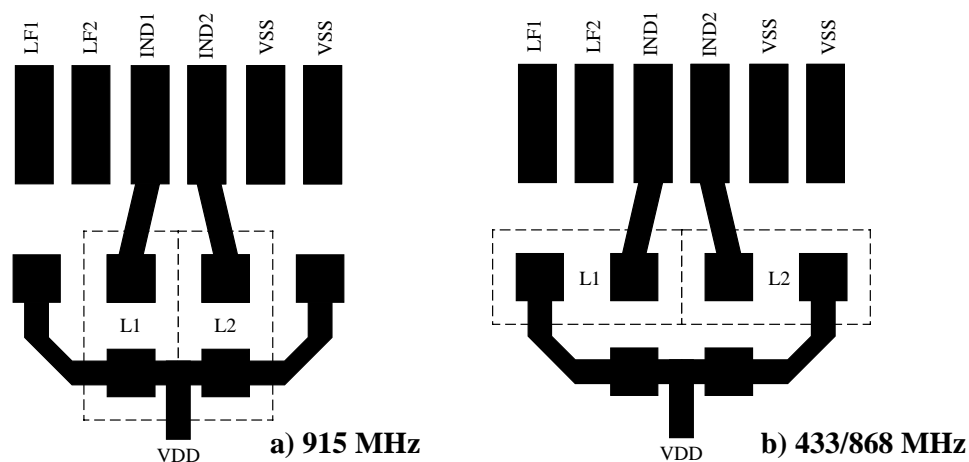

Figure 15. Inductor placement for 915MHz and 433/868MHz operation.

PCB layout example

Figure 16 shows a PCB layout example for the application schematic in Figure 14.
A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a continuous ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane. There is no ground plane beneath the antenna.
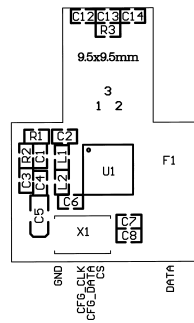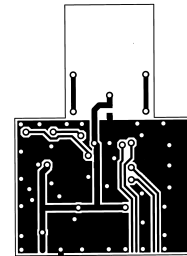
a) Top silk screen
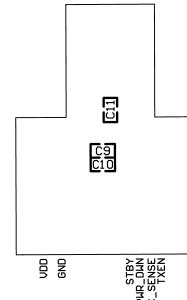
b) Bottom silk screen
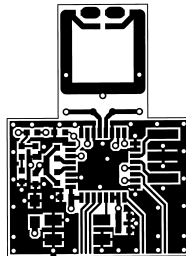
c) Top view

d) Bottom view

Figure 16. PCB layout (example) for nRF903 with loop antenna.

DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications. Nordic VLSI ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 16. Definitions**.**

Nordic VLSI ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic VLSI does not assume any liability arising out of the application or use of any product or circuits described herein.

LIFE SUPPORT APPLICATIONS

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Product specification: Revision Date: 05.02.2001.

Datasheet order code: 050201nRF903

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