SPT104

DC TO 1.1GHz LINEAR AMPLIFIER

FEATURES

- –3dB bandwidth of 1.1 GHz
- 325psec rise and fall times
- 14dB gain, 50Ω input and output
- Low distortion, linear phase
- 1.4:1 VSWR (output, DC-1.1 GHz)
- Direct replacement for CLC104

APPLICATIONS

- Digital and wideband analog communications
- Radar, IF and RF processors
- Fiber optic drivers and receivers
- Photomultiplier preamplifiers

GENERAL DESCRIPTION

The SPT104 linear amplifier represents a significant advance in linear amplifiers. Proprietary design techniques have yielded an amplifier with 14dB of gain and a –3dB bandwidth of DC to 1100MHz. Gain flatness to 750MHz of ±0.4dB coupled with excellent VSWR and phase linearity gives outstanding pulse fidelity and low signal distortion.

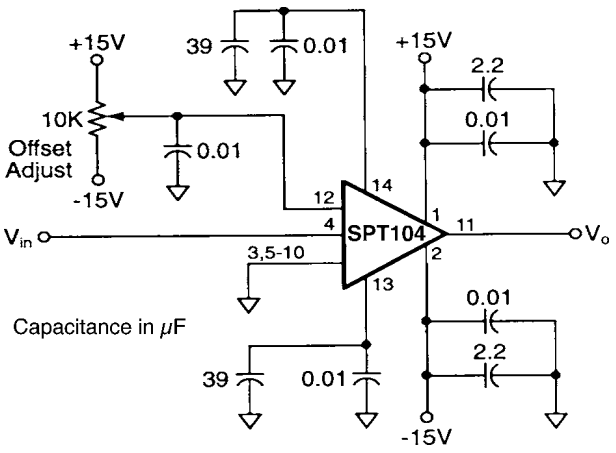
Designed for 50Ω systems, the SPT104 is very easy to use, requiring only properly bypassed power supplies for operation. This translates to time and cost savings in all stages of design and production.

Fast rise time, low overshoot and linear phase make the SPT104 ideal for high-speed pulse amplification. These properties plus low distortion combine to produce an amplifier well suited to many communications applications. With a 1.1GHz bandwidth, the SPT104 can handle the fastest digital traffic, even when the demodulation scheme or the digital coding format requires that DC be maintained. It is also ideal for traditional video amplifier applications such as radar or wideband analog communications systems.

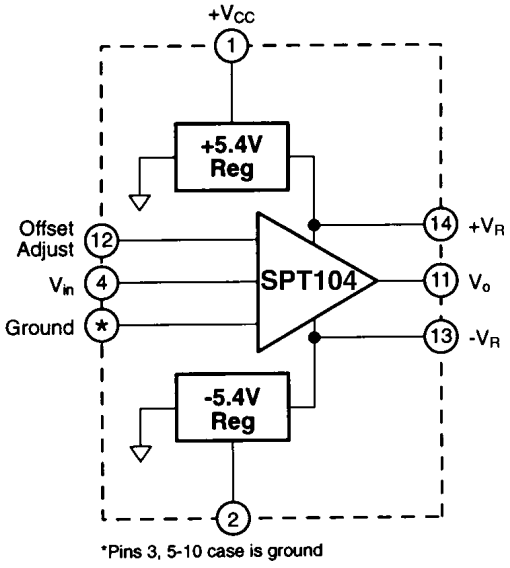
These same characteristics make the SPT104 an excellent choice for use in fiber optics systems, on either the transmitting or receiving end of the fiber. The low group delay distortion insures that pulse integrity will be maintained. As a photomultiplier tube pre-amp, its fast response and quick overload recovery provide for superior system performance.

The SPT104 is constructed using thin film resistor/bipolar transistor technology, and is available in the following versions:

SPT104AI	–25 °C to +85 °C	14-pin double-wide DIP



Basic Circuit Diagram



Equivalent Circuit Diagram

Signal Processing Technologies, Inc.

4755 Forge Road, Colorado Springs, Colorado 80907, USA

Phone: (719) 528-2300 FAX: (719) 528-2370 Website: http://www.spt.com E-Mail: sales@spt.com

SPT104 ELECTRICAL CHARACTERISTICS (T_A = +25 °C, V_{CC} = ±15V, R_L = 50Ω, R_S = 50Ω; unless specified)

PARAMETERS	CONDITIONS	TYP	MIN & MAX RATINGS		UNITS	SYM
Ambient Temperature		+25°C	Min	Max		
FREQUENCY DOMAIN RESPONSE						
† -3dB bandwidth	0dBm out	1100	1000		MHz	SSBW
	10dBm out	1050			MHz	SSBW
† non-inverting gain (note 1)	@ 100MHz	14.2	13.8	14.9	dB	
† gain flatness	DC - 750MHz	±0.4	-0.6	+0.6	dB	
linear phase deviation	DC - 600MHz	1.5		3	°	LPD
group delay		600			ps	GD
reverse isolation						
	DC - 750MHz	40			dB	RINI
	750MHz - 1100MHz	35			dB	RIIN
input return loss	DC - 750MHz	18			dB	
	750MHz - 1100MHz	11			dB	
output return loss	DC - 750MHz	17			dB	
	750MHz - 1100MHz	10			dB	
TIME DOMAIN RESPONSE						
rise and fall time	1V step	325		375	ps	TRS
(10% to 90%)	2V step	375		450	ps	TRL
settling time to 0.8%	1V step	1.2			ns	TS
overshoot	1V step	3			%	OS
overload recovery	V_{inpeak} = ±0.5V	1.2		1.6	ns	OR
NOISE AND DISTORTION RESPONSE						
† 2nd harmonic distortion	0dBm, 100MHz	47			-dBc	HD2
† 3rd harmonic distortion	0dBm, 100MHz	53			-dBc	HD3
† 2nd harmonic distortion	10dBm, 100MHz	40	30		-dBc	HD2
† 3rd harmonic distortion	10dBm, 100MHz	43	35		-dBc	HD3
3rd order intermodulation intercept	100MHz	26			+dBm	
2-tone, 1MHz separation	500MHz	17				
equivalent input noise voltage	10Hz to 1200MHz	55			dB	
noise figure		11			dB	
usable dynamic range	100MHz	71			dB	
	500MHz	65			dB	
STATIC, DC PERFORMANCE						
input bias current	note 2	80		280	µA	IBN
input bias current (drift)	note 2	0.6		2.0	µA/°C	IBN
output offset voltage	note 3	50		250	mV	
output offset voltage (drift)	note 3	375		625	µV/°C	
* supply current	no load	54		60	mA	ICC
supply rejection ratio	1KHz	55			dB	PSRR

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

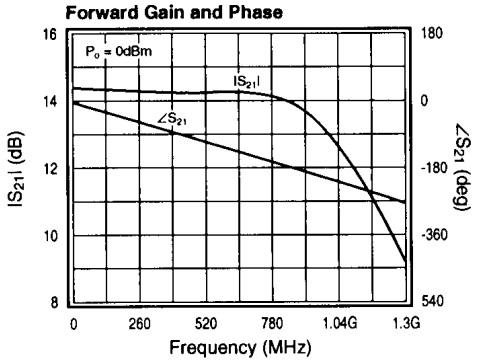
V_{CC}	±9V to ±16V
I_O	±40mA
input voltage	±0.5V
junction temperature	+175°C
operating temperature	AI: -25°C to +85°C
storage temperature	-65°C to +150°C

Notes

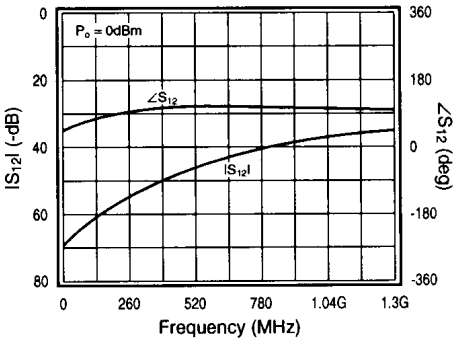
1. Nominal gain only - gain variation over temperature is ±0.1dB.
2. Input offset voltage = (input bias current) x (R_S || 50Ω).
3. Output offset can be adjusted to zero with an external potentiometer – see “Reducing DC Offset”.
4. * AI 100% tested at 25°C.
   † AI Sample tested at 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25 °C, V_{CC} = ±15V, R_L = 50Ω, R_S = 50Ω; unless specified)

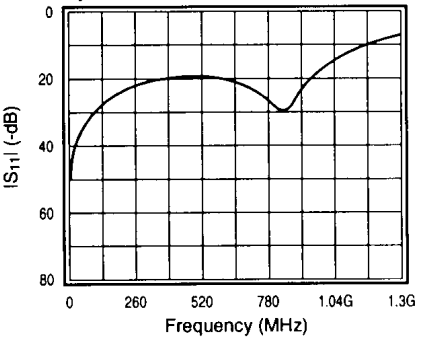
Forward Gain and Phase



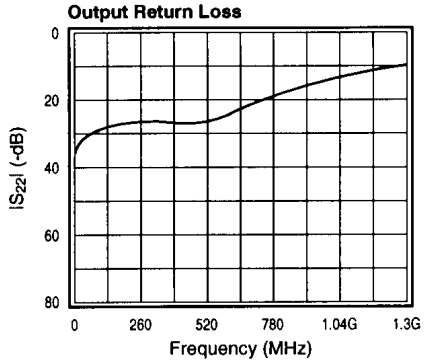
Reverse Gain and Phase



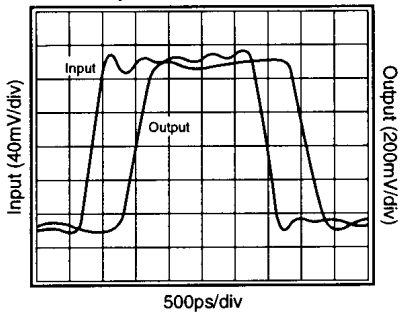
Input Return Loss



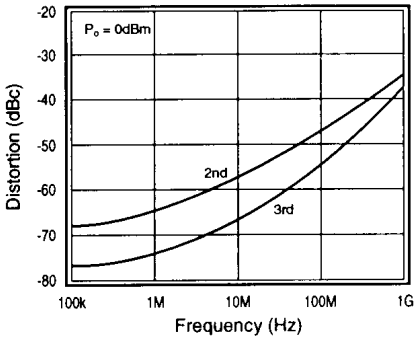
Output Return Loss



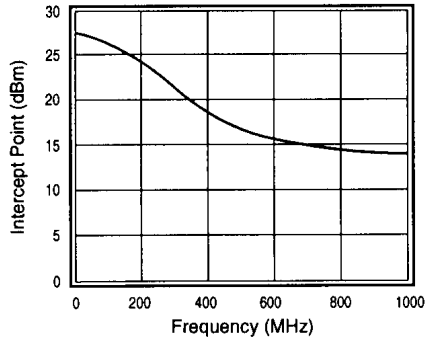
Pulse Response



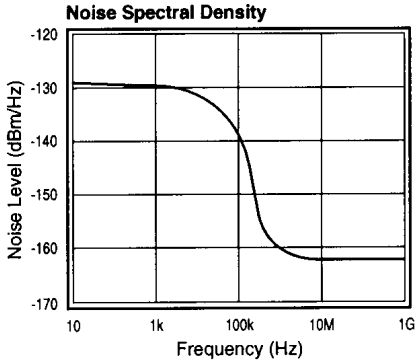
2nd and 3rd Harmonic Distortion



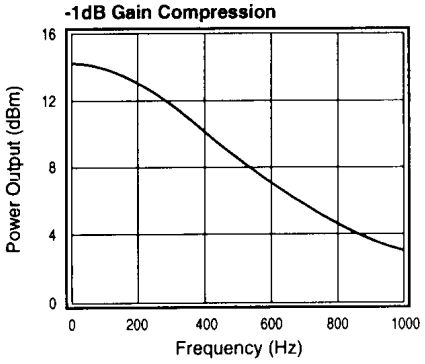
2-Tone, 3rd Order Intermod. Intercept



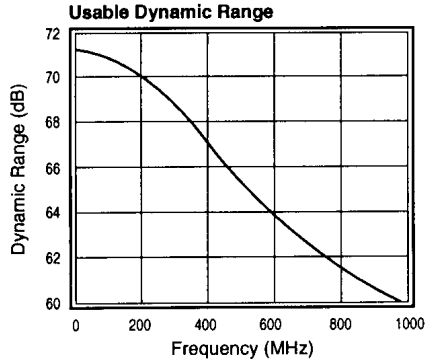
Noise Spectral Density



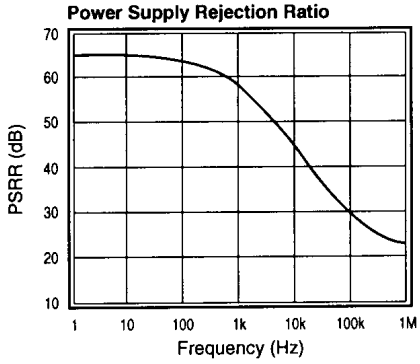
-1dB Gain Compression



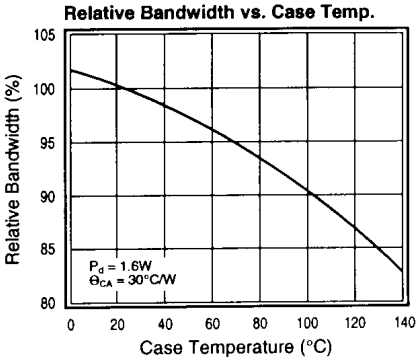
Usable Dynamic Range



Power Supply Rejection Ratio



Relative Bandwidth vs. Case Temp.



PC Board Layout Considerations

Proper layout of printed circuit boards is important to achieve optimum performance of a circuit operating in the 1GHz frequency range. Use of microstripline is recommended for all signal-carrying paths and low resistance, low inductance signal return and bypass paths should be used. To keep the impedance of these paths low, use as much ground plane as possible. Ground plane also serves to increase the flow of heat out of the package.

The SPT104 has three types of connections: signal paths (input and output), DC inputs (supplies and offset adjust), and grounds. 50Ω microstrip is recommended for connection to the input (pin 4) and output (pin 11). Microstrip on a doublesided PC board consists of a ground plane on one side of the board and a constant-width signal-carrying trace on the other side of the board. For 1/16" G10 or FR-4 PC board material, a 0.1" wide trace will have a 50Ω characteristic impedance. The ground plane beneath the signal trace must extend at least one trace width on either side of the trace. Also, all traces (including ground) should be kept at least one trace width from the signal-carrying traces.

To keep power supply noise and oscillations from appearing at the amplifier output, all supply pins should be capacitively bypassed to ground. The power supply pins (1 and 2) are the inputs to a pair of voltage regulators whose outputs are at pins 13 and 14. It is recommended that 0.01µF or larger ceramic capacitors be connected from pins 1, 2, 13 and 14 to ground, within 0.2" of the pins. A 1µF or larger solid tantalum capacitor to ground is required within 3" of pins 1 and 2, and for good low frequency performance, solid tantalum capacitors of at least 15µF should be connected from pins 13 and 14 to ground within 3" of the pins. Use 0.025" or wider traces for the supply lines. The offset adjust pin (12) also requires bypassing; a 0.01µF or larger ceramic capacitor to ground within 0.2" of the pin is recommended.

Grounding is the final layout consideration. Pins 3 and 5-10 should all be connected to a ground plane which should cover as much of one side of the board around the amplifier as possible.

Reducing DC Offset

DC offset of the SPT104 may be adjusted by applying a DC voltage to the amplifier's offset adjust pin (12). The simplest method is shown in Figure 1. Using this method of offset adjust it is possible to vary the output offset by approximately ±400mV. This simple adjustment has no effect on the offset drift characteristics of the SPT104.

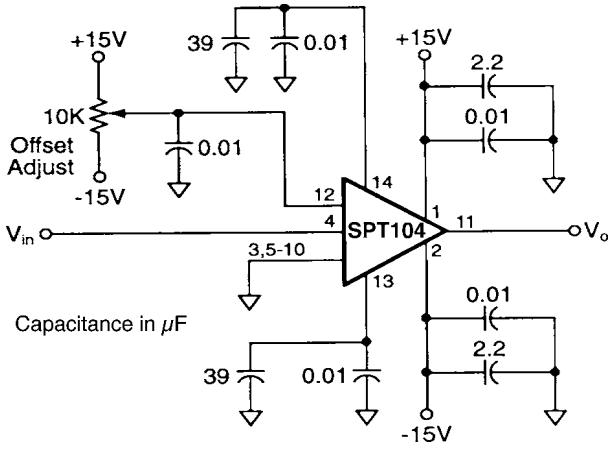


Figure 1: Basic Circuit

If lower offset and offset drift are required, a low frequency op amp may be used in conjunction with the SPT104 in a composite configuration. The suggested circuit appears in Figure 2. Its method of operation is to compare an attenuated version of the output signal to the input signal and apply a correcting voltage at the offset adjust pin. A compensation capacitor C_S reduces the bandwidth of the op amp correction circuit to limit the op amp's effect on the SPT104 to frequencies below f_{45}, the frequency at which the op amp has 45dB of open loop gain. Using an LM108, f_{45} is about 7Hz with C_S = 0.1µF. Thus the op amp can correct DC and low frequency errors below f_{45}, without affecting SPT104 performance above f_{45}. Also note that the noise performance of the op amp will dominate below f_{45}.

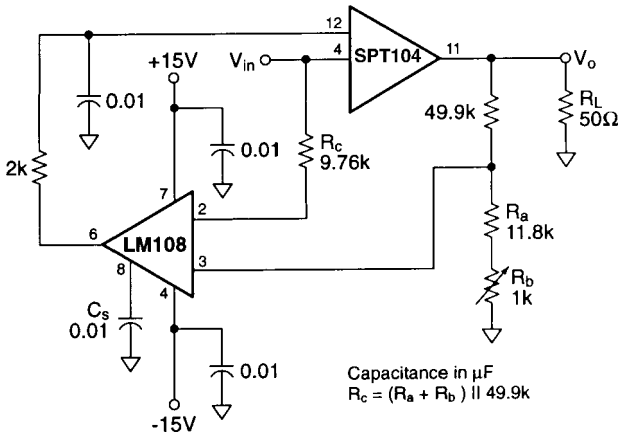


Figure 2: Composite Amplifier

With an LM108 op amp in this composite configuration, input offset is typically 2mV and drift is 15mV/°C. At frequencies well below f_{45}, the composite gain is equal to $(1 + 49.9k/(R_a + R_b))$ and the output impedance is very low. As

the signal frequency increases beyond f_{45}, the op amp loses influence and the SPT104 gain and output impedance dominate. To ensure a smooth transition and matched gain at all frequencies, adjust R_b for a minimum op amp output swing with a $0.1V_{PP}$ sinewave input (to the SPT104) at the frequency f_{45}. Since the SPT104 has a 50Ω output impedance, its output voltage is a function of the load impedance ($A_V \simeq 10R_L/(R_L + 50)$), whereas the gain of the composite amplifier at low frequencies and DC is relatively independent of the load impedance, due to the high open-loop gain of the op amp. Thus, to avoid gain mismatching and phase non-linearity, use the composite amplifier only if the load impedance is constant from DC to at least $10(f_{45})$.

Use of a composite amplifier reduces input offset voltage and its corresponding drift, but has no effect on input bias current. This current is converted to an input voltage by the resistance to ground seen at the amplifier input and the voltage appears, amplified, at the output. Typical input offset voltage due to the bias current is 2mV and input offset drift is approximately 15mV/°C.

Thermal Considerations

The SPT104 case must be maintained at or below 140°C. Note that because of the amplifier design, power dissipation remains fairly constant, independent of the load or drive level. Therefore, standard derating is not possible. There are two ways to keep the case temperature low. The first is to keep the amount of power dissipated inside the package to a minimum and the second is to get the heat out of the package quickly by reducing the thermal resistance from case to ambient.

A large portion of the heat dissipated inside the package is in the voltage regulators. At the minimum +9V supply level the regulators dissipate 390mW and at the maximum ±16V supply level they dissipate 1.2W.

The amplifier itself dissipates a fairly constant 600mW (55mA x 10.8V). Reducing the power dissipation of the internal regulators will go far towards reducing the internal junction temperatures without impacting the performance. Reducing either the input supply voltages (on pins 1 and 2) and/or shunting the regulator current through external resistors (from pins 1 to 14 and pins 2 to 13) are both effective means towards significantly reducing the internal power dissipation. A minimum voltage across the regulator of 3.6V and a minimum regulator current of 10mA will satisfy the regulator dropout voltage and current limits.

Given the maximum anticipated power supply voltages, the shunt resistor should be calculated to yield a 35mA current from that voltage to the regulated voltage of 5.4V. This will leave 10mA through the regulator at the minimum quiescent current of 45mA. The regulator input voltages may be reduced directly by dropping the voltage supplies, or, if that option is not available, using either a zener or resistive dropping element in series with the supply. If a series dropping element is used, the decoupling capacitors must appear on pins 1 and 2 of the SPT104. Figure 3 shows two possible power reduction circuits from fixed ±15V supplies.

Several methods of decreasing the thermal resistance from case to ambient are possible. With no heat paths other than still air at 25°C, the thermal resistance from case to ambient for the SPT104 is about 40°C/W. When placed in a printed circuit board with all ground pins soldered into a ground plane 1" X 1.5", the thermal resistance drops to about 30°C/W. In this configuration, the case rise will be 30°C for 9V supplies and 50°C for 16V supplies. This results in maximum allowable ambient temperatures of 110°C and 90°C, respectively. If higher operating temperatures are required, heat sinking of the package is recommended.

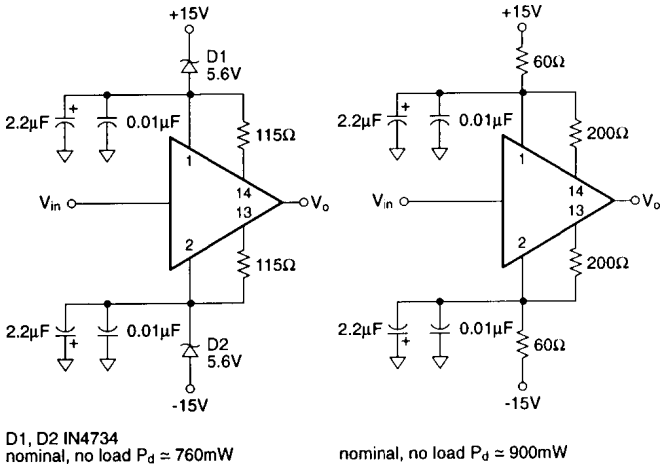


Figure 3: Reducing Power Dissipation

Package Dimensions