CMOS 8-Bit Microcontroller

# TMP88CK48N, TMP88CM48N
# TMP88CK48F, TMP88CM48F

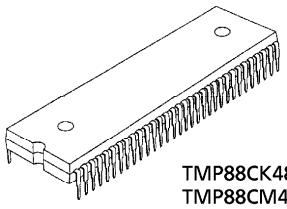
TMP88CK48N, TMP88CM48N, TMP88CK48F, and TMP88CM48F, are high-speed and high-function 8-bit single-chip microcomputers whose built-in features include large-capacity RAM, multi-function timer/counter, and 10-bit AD converter, serial interface (UART/I2C bus). They are equipped with 3 phase brushless DC sensorless/sensor motor control, and AC motor inverter control.

| Part No. | ROM | RAM | Package | OTP MCU |
|---|---|---|---|---|
| TMP88CK48N | 24 Kbytes | 1 Kbytes | P-SDIP64-750-1.78 | TMP88PS49N |
| TMP88CK48F | | | P-QFP64-1420-1.00A | TMP88PS49F |
| TMP88CM48N | 32 Kbytes | | P-SDIP64-750-1.78 | TMP88PS49N |
| TMP88CM48F | | | P-QFP64-1420-1.00A | TMP88PS49F |

## Features

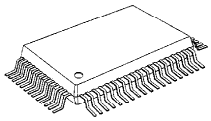
- ◆8-bit single-chip microcomputer TLCS-870/X series microcomputer
- ◆Interrupt sources: 24 (6 external, 18 Internal)
- ◆I/O ports: 56 pins
  - Large-current output: 8 pins (typ. 20 mA), LED direct drive
- ◆16-bit timer/counter: 2 channels
  - Timer, event counter, programmable pulse generator (PPG) output, pulse width measurement, external trigger timer, window mode
- ◆8-bit Timer/Counter: 2 channels
  - Timer, event counter, capture (pulse width/duty measurement), pulse width modulation (PWM) output, programmable divider output (PDO) mode
- ◆Time base timer (interrupt frequency: 1 to 16384 Hz)
- ◆Watchdog timer
- ◆Divider output function (frequency: 1 to 8 kHz)
- ◆Programmable motor driver (PMD): 1 channel
  - Rotor position: minimum resolution of 250 ns for detecting rotor position
  - Motor control timer, timer capture function
  - Overload protection function
    DC overload protection function
    AC overload protection function (Can halt counter in 3-phase PWM output circuit)
  - Protection circuit for malfunction (urgent halt)
  - Automatic direction change, automatic position detection start
- ◆High-speed PWM output: 1 channel
  - Cycle: 32 kHz, 64 kHz, 128 kHz
  - Resolution: 8-bit, 7-bit, 6-bit mode selectable

P-SDIP64-750-1.78



TMP88CK48N
TMP88CM48N
TMP88PS49N

P-QFP64-1420-1.00A



TMP88CK48F
TMP88CM48F
TMP88PS49F

980910EBP1

◆Serial interface
- 8-bit SIO/I2C bus
- Universal asynchronous receiver transmitter (UART)

◆10-bit successive approximation type AD converter
- Analog input: 16 channels
- Conversion time: 11.5 μs / 46 μs (at 16 MHz operation)

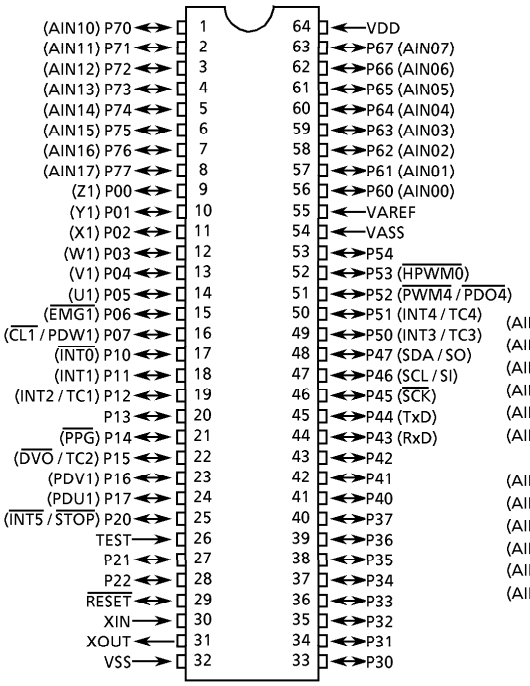
◆Low power dissipation operation (2 modes)
- STOP mode:Stops oscillation (battery or capacitor backup). Port output hold or high impedance selectable
- IDLE mode:Stops CPU but continues operation of peripheral hardware. Released by interrupt (restarts CPU)

◆Operating voltage: 4.5 to 5.5 V at 16 MHz operation

◆Emulation pod: BM88CM49N0A

## Pin Assignments

P-SDIP64-750-1.78

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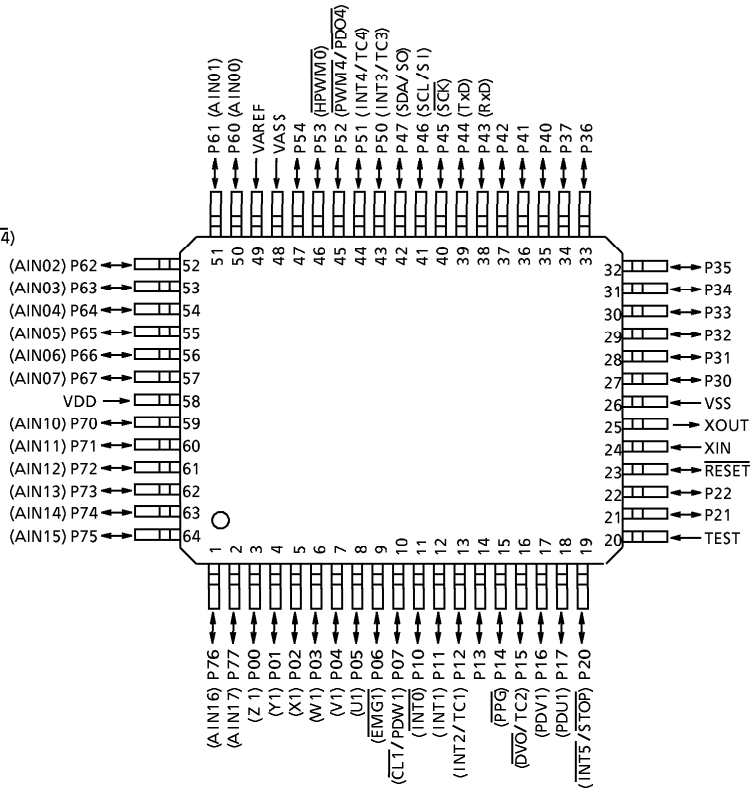
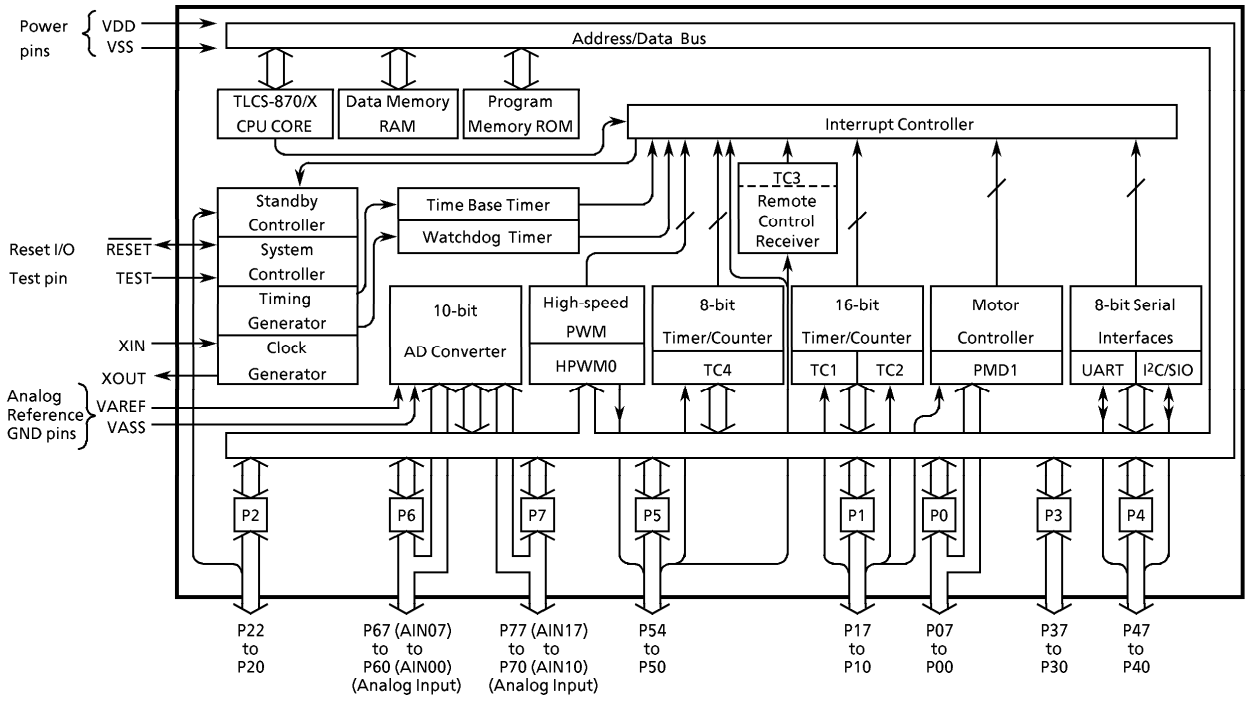



## Block Diagram



## Pin Function

| Pin Name | I/O | Function | |
|---|---|---|---|
| P07 ($\overline{CL1}$/PDW1) | I/O (Input) | 8-bit programmable I/O port (tri state) Input or output specifiable in units of bits. When using pins for motor control circuit, set accordingly using P0CR, then MDCR to 1. | Overload protection input 1/motor control circuit W1-phase position detection input |
| P06 ($\overline{EMG1}$) | | | Motor control circuit malfunction detection input 1 |
| P05 (U1) | I/O (Output) | | Motor control circuit U1-/V1-/W1-phase output |
| P04 (V1) | | | |
| P03 (W1) | | | |
| P02 (X1) | I/O (Output) | | Motor control circuit X1-/ Y1-/Z1-phase output |
| P01 (Y1) | | | |
| P00 (Z1) | | | |
| P17 (PDU1) | I/O (Input) | 8-bit programmable I/O port (tri state) Input or output specifiable units of bits. When using pins for motor control circuit, timer/counter input, or external interrupt input, set them to input mode. When using pins for PPG output, divider output, or PWM output/PDO output, set them to output mode. | Motor control circuit U1-phase position detection input |
| P16 (PDV1) | | | Motor control circuit V1-phase position detection input |
| P15 ($\overline{DVO}$/TC2) | II/O (Output/Input) | | Divider output or Timer/Counter 2 input |
| P14 ($\overline{PPG}$) | I/O (Output) | | Programmable pulse generator output |
| P13 | | | — |
| P12 (INT2/TC1) | I/O (Input) | | External interrupt input 2 or Timer/Counter 1 input |
| P11 (INT1) | | | External interrupt input 1 |
| P10 ($\overline{INT0}$) | | | External interrupt input 0 |
| P22 | I/O | 3-bit I/O port When using pins for input port, external interrupt input, or STOP mode release input, set output latches to 1. | — |
| P21 | | | — |
| P20 ($\overline{INT5}$/$\overline{STOP}$) | I/O (Input) | | External interrupt input 5 or STOP mode release signal input |
| P37 | I/O (Output) | 8-bit I/O port (large-current output) When using pins for motor control circuit input, set output latches to 1, then MDCR2 to 1. | — |
| P36 | | | |
| P35 | | | |
| P34 | | | |
| P33 | | | |
| P32 | | | |
| P31 | | | |
| P30 | | | |
| P47 (SDA/SO) | I/O (I/O/Output) | 8-bit I/O port When using pins for motor control circuit input, UART/I2C/SIO, set output latches to 1. | I2C/SIO I/O |
| P46 (SCL/SI) | I/O (I/O/Input) | | |
| P45 ($\overline{SCK}$) | I/O (I/O) | | |
| P44 (TxD) | I/O (Input) | | UART data input |
| P43 (RxD) | I/O (Output) | | UART data output |
| P42 | I/O | | — |
| P41 | | | |
| P40 | | | |
| P54 | I/O | 5-bit input/output port with latch. When using pins for input port, HPWM output, PWM output/PDO output, external interrupt input, or timer/counter input, set output latches to 1. | — |
| P53 ($\overline{HPWM0}$) | I/O (Output) | | high-speed PWM output |
| P52 ($\overline{PWM4}$/$\overline{PDO4}$) | | | 8-BIT PWM output 4 or, 8-bit programmable divider output 4 |
| P51 (INT4/TC4) | I/O (Input) | | External interrupt 4 input or timer / counter 4 input |
| P50 (INT3/TC3) | | | External interrupt 3 input or timer / counter 3 input |

| Pin Name | Input/Output | Function | |
|---|---|---|---|
| P67 (AIN07)<br>to P60 (AIN00) | I/O (Input) | 8-bit programmable I/O port (tri state)<br>Input or output specifiable in units of bits.<br>When using pins for analog input, set to input mode using P6CR and ADCCR. | AD converter analog input |
| P77 (AIN17)<br>to P70 (AIN10) | I/O (Input) | 8-bit programmable I/O port (tri state)<br>Input or output specifiable in units of bits.<br>When using pins for analog input, set to input mode using P7CR and ADCCR. | AD converter analog input |
| XIN, XOUT | Input, Output | High-frequency oscillator connecting pins. For external clock input, input to XIN and leave XOUT open. | |
| $\overline{\text{RESET}}$ | I/O | Reset signal input, watchdog timer output, address trap reset output, system clock reset output | |
| TEST | Input | Shipment test pin, fix to "L" level. | |
| VDD, VSS | Power Supply | + 5 V, 0 V (GND) | |
| VAREF, VASS | | Analog reference voltage for AD conversion. Reference GND. | |

## Operation

### 1. CPU Core Functions

The CPU core consists of the CPU, system clock control circuit, and interrupt control circuit. This chapter describes the CPU core, program memory, data memory and the reset circuit.

### 1.1 Memory Address Map

The TMP88CK48/M48 memory consists of four blocks: ROM, RAM, special function registers (SFR) and Data buffer registers (DBR). They are all mapped to a 1 Mbyte address space. Figure 1-1 shows the TMP88CK48/M48 memory address map. There are 16 general-purpose registers mapped to the RAM address space.

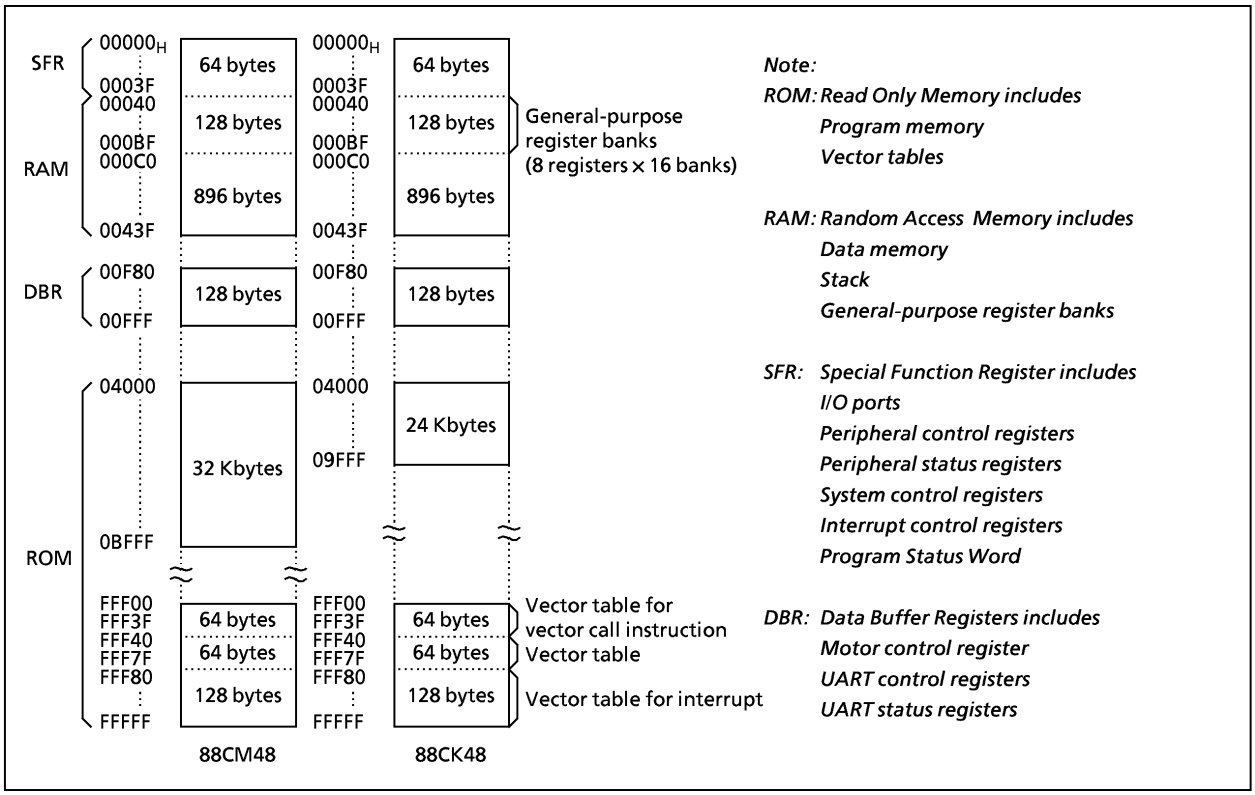



Figure 1-1. Memory Address Maps

## Electrical Characteristics

### Absolute Maximum Ratings ($V_{SS}$ = 0 V)

| Parameter | Symbol | Pins | Ratings | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | – 0.3 to 6.5 | V |
| Input Voltage | $V_{IN}$ | | – 0.3 to $V_{DD}$ + 0.3 | V |
| Output Voltage | $V_{OUT1}$ | Port P21, P22, $\overline{RESET}$, Tri-state port | – 0.3 to $V_{DD}$ + 0.3 | V |
| | $V_{OUT2}$ | Port P20, Sink open drain port | – 0.3 to 5.5 | V |
| Output Current | $I_{OUT1}$ | Ports P1, P2, P4, P5, P6, P7 | 3.2 | mA |
| | $I_{OUT2}$ | Port P0 | 20 | |
| | $I_{OUT3}$ | Port P3 | 30 | |
| Output Current | $\Sigma I_{OUT1}$ | Ports P1, P2, P4, P5, P6, P7 | 120 | mA |
| | $\Sigma I_{OUT2}$ | Port P0 | 60 | |
| | $\Sigma I_{OUT3}$ | Port P3 | 120 | |
| Power Dissipation [Topr = 70°C] | PD | TMP88CK48N/TMP88CM48N | 600 | mW |
| | | TMP88CK48F/TMP88CM48F | 350 | |
| Soldering Temperature (time) | Tsld | | 260 (10 s) | °C |
| Storage Temperature | Tstg | | – 55 to 125 | °C |
| Operating Temperature | Topr | | – 40 to 85 | °C |

*Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.*

### Recommended Opeating Conditions ($V_{SS}$ = 0 V, Topr = – 40 to 85°C)

| Parameter | Symbol | Pins | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | fc = 16 MHz | NORMAL mode | 4.5 | 5.5 | V |
| | | | | IDLE mode | | | |
| | | | | STOP mode | | | |
| Input High Voltage | $V_{IH1}$ | Except hysteresis input | $V_{DD} \geqq 4.5$ V | | $V_{DD} \times 0.70$ | $V_{DD}$ | V |
| | $V_{IH2}$ | Hysteresis input | | | $V_{DD} \times 0.75$ | | |
| | $V_{IH3}$ | | $V_{DD} < 4.5$ V | | $V_{DD} \times 0.90$ | | |
| Input Low Voltage | $V_{IL1}$ | Except hysteresis input | $V_{DD} \geqq 4.5$ V | | 0 | $V_{DD} \times 0.30$ | V |
| | $V_{IL2}$ | Hysteresis input | | | | $V_{DD} \times 0.25$ | |
| | $V_{IL3}$ | | $V_{DD} < 4.5$ V | | | $V_{DD} \times 0.10$ | |
| Clock Frequency | fc | XIN, XOUT | $V_{DD}$ = 4.5 to 5.5 V | | 8.0 | 16.0 | MHz |

*Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.*

*Note 2: Clock frequency fc: The condition of supply voltage range is the value in NORMAL and IDLE modes.*

## D.C. Characteristics

($V_{SS}$ = 0 V, Topr = – 40 to 85°C)

| Parameter | Symbol | Pins | Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Hysteresis Voltage | $V_{HS}$ | Hysteresis inputs | | – | 0.9 | – | V |
| Input Current | $I_{IN1}$ | TEST | $V_{DD}$ = 5.5 V<br>$V_{IN}$ = 5.5 V/0 V | – | – | ± 2 | μA |
| | $I_{IN2}$ | Sink open drain, Tri-state ports | | | | | |
| | $I_{IN3}$ | $\overline{RESET}$, $\overline{STOP}$ | | | | | |
| Input Resistor (*) | $R_{IN}$ | TEST with pull-down | | 20 | 70 | 170 | kΩ |
| | | $\overline{RESET}$ | | 90 | 220 | 510 | |
| Output Leakage Current | $I_{OL}$ | Sink open drain, Tri-state ports | $V_{DD}$ = 5.5 V, $V_{OUT}$ = 5.5 V/0 V | – | – | ± 2 | μA |
| Output High Voltage | $V_{OH}$ | Tri-state ports | $V_{DD}$ = 4.5 V, $I_{OH}$ = – 0.7 mA | 4.1 | – | – | V |
| Output Low Current | $I_{OL1}$ | Except XOUT, Ports P0, P3. | $V_{DD}$ = 4.5 V, $V_{OL}$ = 0.4 V | – | 1.6 | – | mA |
| | $I_{OL2}$ | Port P0 | $V_{DD}$ = 4.5 V, $V_{OL}$ = 1.0 V | 6 | 10 | – | |
| | $I_{OL3}$ | Port P3 | | – | 20 | – | |
| Supply Current in NORMAL Mode | | | $V_{DD}$ = 5.5 V<br>$V_{IN}$ = 5.3 V/0.2 V<br>fc = 16.0 MHz | – | 20 | 32 | mA |
| Supply Current in IDLE Mode | | | | – | 10 | 16 | mA |
| Supply Current in STOP Mode | | | $V_{DD}$ = 5.5 V<br>$V_{IN}$ = 5.3 V/0.2 V | – | 0.5 | 20 | μA |

*Note 1: Typical values show those at Topr = 25°C, $V_{DD}$ = 5 V.*

*Note 2: Input Current $I_{IN1}$, $I_{IN3}$; The current through registor is not included, when the input resistor (pull-up or pull-down) is contained.*

*Note 3: IDD except $I_{REF}$.*

## AD Conversion Characteristics

(Topr = – 40 to 85°C)

| Parameter | Symbol | Conditions | Min | Typ. | Max | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | ADCDR1 | ADCDR2 | | |
| | | | | | | ACK = 0 | ACK = 1 | |
| Analog Reference Voltage | $V_{AREF}$ | $V_{AREF}$ – $V_{ASS}$ ≧ 3.5 V | $V_{DD}$ – 1.0 | — | $V_{DD}$ | | | V |
| | $V_{ASS}$ | | $V_{SS}$ | — | 1.0 | | | |
| Analog Input Voltage | $V_{AIN}$ | | $V_{ASS}$ | — | $V_{AREF}$ | | | V |
| Analog Supply Current | $I_{REF}$ | $V_{AREF}$ = 5.5 V,<br>$V_{ASS}$ = 0.0 V | — | 0.5 | 1.0 | | | mA |
| Non-Linearity Error | | $V_{DD}$ = 5.0 V, $V_{SS}$ = 0.0 V<br>$V_{AREF}$ = 5.000 V<br>$V_{ASS}$ = 0.000 V | — | — | ± 1 | ± 3 | ± 2 | LSB |
| Zero Point Error | | | — | — | ± 1 | ± 3 | ± 2 | |
| Full Scale Error | | | — | — | ± 1 | ± 3 | ± 2 | |
| Total Error | | | — | — | ± 2 | ± 6 | ± 4 | |

*Note 1: ADCDR1: 8-bit AD conversion result (1LSB = $\Delta V_{AREF}$/256)*
*ADCDR2: 10-bit AD conversion result (1LSB = $\Delta V_{AREF}$/1024)*

*Note 2: Total error includes all errors except quantization error.*

## A.C. Characteristics

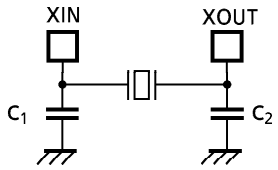
($V_{SS}$ = 0 V, $V_{DD}$ = 4.5 to 5.5 V, Topr = – 40 to 85°C)

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Machine Cycle Time | tcy | NORMAL mode | 0.25 | – | 0.5 | μs |
| | | IDLE mode | | | | |
| High Level Clock Pulse Width | $t_{WCH}$ | For external clock operation (XIN input) | 31.25 | – | 62.5 | ns |
| Low Level Clock Pulse Width | $t_{WCL}$ | | | | | |

## Recommended Oscillating Conditions

($V_{SS}$ = 0 V, $V_{DD}$ = 4.5 to 5.5 V, Topr = – 40 to 85°C)

| Parameter | Oscillator | Oscillation Frequency | Recommended Oscillator | Recommended Constant | |
|---|---|---|---|---|---|
| | | | | $C_1$ | $C_2$ |
| High-frequency Oscillation | Ceramic Resonator | 16 MHz | MURATA CSA16.00MXZ | 5 pF | 5 pF |
| | | | MURATA CST16.00MXW | built-in 5 pF | built-in 5 pF |



High-frequency Oscillation

*Note: An electrical shield by metal shield on the surface of IC package should be recommendable in order to prevent the device from the high electric fieldstress applied from CRT (Cathode Ray Tube) for continuous reliable operation.*