

**16 M-BIT DYNAMIC RAM**  
**2 M-WORD BY 8-BIT, HYPER PAGE MODE**

**DESCRIPTION**

The  $\mu$ PD4216805 is a 2 097 152 words by 8 bits dynamic CMOS RAM with optional hyper page mode. Hyper page mode is a kind of the page mode and is useful for the read operation. The  $\mu$ PD4216805 is packed in 28-pin plastic TSOP(II) and 28-pin plastic SOJ.

**FEATURES**

- Hyper page mode
- 2 097 152 words by 8 bits organization
- Single +5.0 V $\pm$ 10 % power supply
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- 4 096 refresh cycles /64 ms

| Part number        | Access time (MAX.) | R/W cycle time (MIN.) | Hyper page mode cycle time (MIN.) |
|--------------------|--------------------|-----------------------|-----------------------------------|
| $\mu$ PD4216805-50 | 50 ns              | 84 ns                 | 20 ns                             |
| $\mu$ PD4216805-60 | 60 ns              | 104 ns                | 25 ns                             |
| $\mu$ PD4216805-70 | 70 ns              | 124 ns                | 30 ns                             |

**ORDERING INFORMATION**

| Part number                                   | Access time (MAX.) | Package   | Refresh  |
|---|--------------------|---|--|
| $\mu$ PD4216805G5-50                          | 50 ns              | 28-pin Plastic TSOP (II)<br>(400 mil)             | CAS before RAS refresh<br>RAS only refresh<br>Hidden refresh |
| $\mu$ PD4216805G5-60                          | 60 ns              |   |  |
| $\mu$ PD4216805G5-70                          | 70 ns              |   |  |
| <del><math>\mu</math>PD4216805G5-50-7KD</del> | <del>50 ns</del>   | <del>28-pin Plastic TSOP (II)<br/>(400 mil)</del> |  |
| <del><math>\mu</math>PD4216805G5-60-7KD</del> | <del>60 ns</del>   | <del>Reverse bent</del>                           |  |
| <del><math>\mu</math>PD4216805G5-70-7KD</del> | <del>70 ns</del>   |   |  |
| $\mu$ PD4216805LE-50                          | 50 ns              | 28-pin Plastic SOJ<br>(400 mil)                   |  |
| $\mu$ PD4216805LE-60                          | 60 ns              |   |  |
| $\mu$ PD4216805LE-70                          | 70 ns              |   |  |

**QUALITY GRADE**

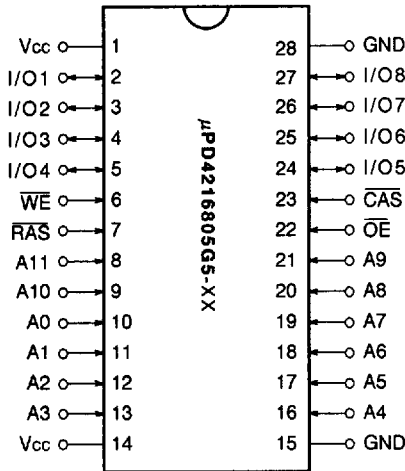
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

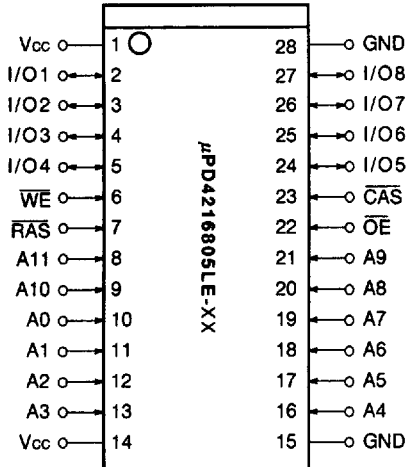
The information in this document is subject to change without notice.

PIN CONFIGURATIONS (Marking side)

28-pin Plastic TSOP (II) (400 mil)

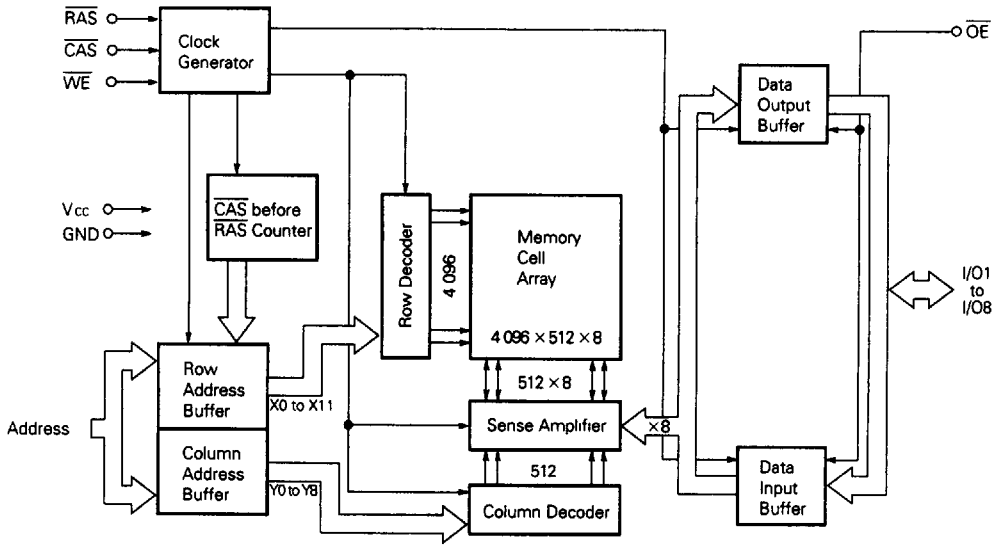


28-pin Plastic SOJ (400 mil)



- A0 to A11 : Address Inputs
- I/O1 to I/O8 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- Vcc : Power Supply
- GND : Ground

BLOCK DIAGRAM



**INPUT/OUTPUT PIN FUNCTIONS**

The μPD4216805 has input pins  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ ,  $\overline{OE}$ , A0 to A11 and input/output pins I/O1 to I/O8.

| Pin name                                    | Input/Output | Function  |
|---|--------------|---|
| $\overline{RAS}$<br>(Row address strobe)    | Input        | $\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line.<br>It refreshes memory cell array of one line selected by the row address.<br>It also selects the following function.<br>• $\overline{CAS}$ before $\overline{RAS}$ refresh   |
| $\overline{CAS}$<br>(Column address strobe) |              | $\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.  |
| A0 to A11<br>(Address inputs)               |              | Address bus.<br>Input total 21-bit of address signal, upper 12-bit and lower 9-bit in sequence (address multiplex method).<br>Therefore, one word is selected from 2 097 152-word by 8-bit memory cell array.<br>In actual operation, latch row address by specifying row address and activating $\overline{RAS}$ .<br>Then, switch the address bus to column address and activate $\overline{CAS}$ .<br>Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated.<br>Therefore, the address input setup time ( $t_{ASR}$ , $t_{ASC}$ ) and hold time ( $t_{RAH}$ , $t_{CAH}$ ) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$ . |
| $\overline{WE}$<br>(Write enable)           |              | Write control signal.<br>Write operation is executed by activating $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ .  |
| $\overline{OE}$<br>(Output enable)          |              | Read control signal.<br>Read operation can be executed by activating $\overline{RAS}$ , $\overline{CAS}$ and $\overline{OE}$ .<br>If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device.<br>Therefore, read operation cannot be executed.   |
| I/O1 to I/O8<br>(Data inputs/outputs)       | Input/Output | 8-bit data bus.<br>I/O1 to I/O8 are used to input/output data.  |

**ELECTRICAL SPECIFICATIONS** Notes1, 2

**ABSOLUTE MAXIMUM RATINGS**

| Parameter                          | Symbol           | Condition | Rating       | Unit |
|------------------------------------|------------------|-----------|--------------|------|
| Voltage on any pin relative to GND | V <sub>T</sub>   |           | -1.0 to +7.0 | V    |
| Supply voltage                     | V <sub>CC</sub>  |           | -1.0 to +7.0 | V    |
| Output current                     | I <sub>O</sub>   |           | 50           | mA   |
| Power dissipation                  | P <sub>D</sub>   |           | 1            | W    |
| Operating temperature              | T <sub>Opt</sub> |           | 0 to +70     | °C   |
| Storage temperature                | T <sub>Stg</sub> |           | -55 to +125  | °C   |

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

| Parameter                | Symbol          | Condition | MIN. | TYP. | MAX.                 | Unit |
|--------------------------|-----------------|-----------|------|------|----------------------|------|
| Supply voltage           | V <sub>CC</sub> |           | 4.5  | 5.0  | 5.5                  | V    |
| High level input voltage | V <sub>IH</sub> |           | 2.4  |      | V <sub>CC</sub> +1.0 | V    |
| Low level input voltage  | V <sub>IL</sub> |           | -1.0 |      | +0.8                 | V    |
| Ambient temperature      | T <sub>a</sub>  |           | 0    |      | 70                   | °C   |

**CAPACITANCE (T<sub>a</sub> = +25 °C , f = 1 MHz)**

| Parameter                     | Symbol           | Test condition   | MIN. | TYP. | MAX. | Unit |
|-------------------------------|------------------|------------------|------|------|------|------|
| Input capacitance             | C <sub>I1</sub>  | A0 to A11        |      |      | 5    | pF   |
|                               | C <sub>I2</sub>  | RAS, CAS, WE, OE |      |      | 7    | pF   |
| Data Input/Output capacitance | C <sub>I/O</sub> | I/O1 to I/O8     |      |      | 7    | pF   |

**DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)**

| Parameter   | Symbol            | Test condition  | MIN.                     | MAX. | Unit | Notes   |
|---|-------------------|---|--------------------------|------|------|---------|
| Operating current   | I <sub>CC1</sub>  | $\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling<br>$t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$<br>$I_o = 0 \text{ mA}$  | t <sub>RAC</sub> = 50 ns | 100  | mA   | 3,4,7   |
|   |                   |   | t <sub>RAC</sub> = 60 ns | 90   |      |         |
|   |                   |   | t <sub>RAC</sub> = 70 ns | 80   |      |         |
| Standby current   | I <sub>CC2</sub>  | $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$<br>$\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$<br>$I_o = 0 \text{ mA}$ | I <sub>o</sub> = 0 mA    | 2    | mA   |         |
|   |                   |   | I <sub>o</sub> = 0 mA    | 1    |      |         |
| $\overline{\text{RAS}}$ only refresh current                              | I <sub>CC3</sub>  | $\overline{\text{RAS}}$ Cycling<br>$\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$<br>$t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$<br>$I_o = 0 \text{ mA}$                          | t <sub>RAC</sub> = 50 ns | 100  | mA   | 3,4,5,7 |
|   |                   |   | t <sub>RAC</sub> = 60 ns | 90   |      |         |
|   |                   |   | t <sub>RAC</sub> = 70 ns | 80   |      |         |
| Operating current<br>(Hyper page mode)                                    | I <sub>CC4</sub>  | $\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.})$<br>$\overline{\text{CAS}}$ Cycling<br>$t_{\text{HPC}} = t_{\text{HPC}}(\text{MIN.})$<br>$I_o = 0 \text{ mA}$                        | t <sub>RAC</sub> = 50 ns | 100  | mA   | 3,4,6   |
|   |                   |   | t <sub>RAC</sub> = 60 ns | 90   |      |         |
|   |                   |   | t <sub>RAC</sub> = 70 ns | 80   |      |         |
| $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$<br>refresh current | I <sub>CC5</sub>  | $\overline{\text{RAS}}$ Cycling<br>$t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$<br>$I_o = 0 \text{ mA}$   | t <sub>RAC</sub> = 50 ns | 100  | mA   | 3,4     |
|   |                   |   | t <sub>RAC</sub> = 60 ns | 90   |      |         |
|   |                   |   | t <sub>RAC</sub> = 70 ns | 80   |      |         |
| Input leakage current   | I <sub>I(L)</sub> | $V_i = 0 \text{ to } 5.5 \text{ V}$<br>all other pins not under test = 0 V  | -10                      | +10  | μA   |         |
| Output leakage current  | I <sub>O(L)</sub> | $V_o = 0 \text{ to } 5.5 \text{ V}$<br>Output is disabled (Hi-Z)  | -10                      | +10  | μA   |         |
| High level output voltage   | V <sub>OH</sub>   | I <sub>o</sub> = -5.0 mA  | 2.4                      |      | V    |         |
| Low level output voltage  | V <sub>OL</sub>   | I <sub>o</sub> = +4.2 mA  |                          | 0.4  | V    |         |

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted) Notes 8, 9 (1/2)

| Parameter  | Symbol            | t <sub>RAC</sub> = 50 ns |        | t <sub>RAC</sub> = 60 ns |        | t <sub>RAC</sub> = 70 ns |        | Unit | Notes  |
|--|-------------------|--------------------------|--------|--------------------------|--------|--------------------------|--------|------|--------|
|  |                   | MIN.                     | MAX.   | MIN.                     | MAX.   | MIN.                     | MAX.   |      |        |
| Read / Write Cycle Time  | t <sub>RC</sub>   | 84                       |        | 104                      |        | 124                      |        | ns   |        |
| Read Modify Write Cycle Time   | t <sub>RWC</sub>  | 107                      |        | 133                      |        | 157                      |        | ns   |        |
| Access Time from $\overline{\text{RAS}}$                                 | t <sub>RAC</sub>  |                          | 50     |                          | 60     |                          | 70     | ns   | 10, 11 |
| Access Time from $\overline{\text{CAS}}$                                 | t <sub>CAC</sub>  |                          | 13     |                          | 15     |                          | 18     | ns   | 10, 11 |
| Access Time from Column Address  | t <sub>AA</sub>   |                          | 25     |                          | 30     |                          | 35     | ns   | 10, 11 |
| Access Time from $\overline{\text{CAS}}$ Precharge                       | t <sub>ACP</sub>  |                          | 27     |                          | 35     |                          | 40     | ns   | 11     |
| Access Time from $\overline{\text{OE}}$                                  | t <sub>OEA</sub>  |                          | 13     |                          | 15     |                          | 18     | ns   | 11     |
| $\overline{\text{RAS}}$ to Column Address Delay Time                     | t <sub>RAD</sub>  | 9                        | 25     | 12                       | 30     | 12                       | 35     | ns   | 10     |
| $\overline{\text{CAS}}$ to Data Setup Time                               | t <sub>CLZ</sub>  | 0                        |        | 0                        |        | 0                        |        | ns   | 11     |
| $\overline{\text{OE}}$ to Data Setup Time                                | t <sub>OLZ</sub>  | 0                        |        | 0                        |        | 0                        |        | ns   | 11     |
| $\overline{\text{OE}}$ to Data Delay Time                                | t <sub>OED</sub>  | 10                       |        | 13                       |        | 15                       |        | ns   |        |
| Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$            | t <sub>OEZ</sub>  | 0                        | 10     | 0                        | 13     | 0                        | 15     | ns   | 12, 18 |
| $\overline{\text{OE}}$ Hold Time   | t <sub>OEH</sub>  | 0                        |        | 0                        |        | 0                        |        | ns   |        |
| $\overline{\text{OE}}$ Lead Time Referenced to $\overline{\text{RAS}}$   | t <sub>OES</sub>  | 0                        |        | 0                        |        | 0                        |        | ns   |        |
| Transition Time (Rise and Fall)  | t <sub>T</sub>    | 1                        | 50     | 1                        | 50     | 1                        | 50     | ns   |        |
| $\overline{\text{RAS}}$ Precharge Time                                   | t <sub>RP</sub>   | 30                       |        | 40                       |        | 50                       |        | ns   |        |
| $\overline{\text{RAS}}$ Pulse Width                                      | t <sub>RAS</sub>  | 50                       | 10 000 | 60                       | 10 000 | 70                       | 10 000 | ns   |        |
| $\overline{\text{RAS}}$ Hold Time  | t <sub>RSH</sub>  | 7                        |        | 10                       |        | 12                       |        | ns   |        |
| $\overline{\text{CAS}}$ Pulse Width                                      | t <sub>CAS</sub>  | 7                        | 10 000 | 10                       | 10 000 | 12                       | 10 000 | ns   |        |
| $\overline{\text{CAS}}$ Hold Time  | t <sub>CSH</sub>  | 35                       |        | 40                       |        | 50                       |        | ns   |        |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time            | t <sub>RCD</sub>  | 11                       | 37     | 14                       | 45     | 14                       | 52     | ns   | 10     |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time        | t <sub>CRP</sub>  | 5                        |        | 5                        |        | 5                        |        | ns   | 13     |
| $\overline{\text{CAS}}$ Precharge Time                                   | t <sub>CPN</sub>  | 7                        |        | 10                       |        | 10                       |        | ns   |        |
| $\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time      | t <sub>RPC</sub>  | 5                        |        | 5                        |        | 5                        |        | ns   |        |
| $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge | t <sub>RHCP</sub> | 27                       |        | 35                       |        | 40                       |        | ns   |        |
| Row Address Setup Time   | t <sub>ASR</sub>  | 0                        |        | 0                        |        | 0                        |        | ns   |        |
| Row Address Hold Time  | t <sub>RAH</sub>  | 7                        |        | 10                       |        | 10                       |        | ns   |        |
| Column Address Setup Time  | t <sub>ASC</sub>  | 0                        |        | 0                        |        | 0                        |        | ns   |        |
| Column Address Hold Time   | t <sub>CAH</sub>  | 7                        |        | 10                       |        | 12                       |        | ns   |        |
| Column Address Lead Time Referenced to $\overline{\text{RAS}}$           | t <sub>RAL</sub>  | 25                       |        | 30                       |        | 35                       |        | ns   |        |
| Read Command Setup Time  | t <sub>RCS</sub>  | 0                        |        | 0                        |        | 0                        |        | ns   |        |
| Read Command Hold Time Referenced to $\overline{\text{RAS}}$             | t <sub>RRH</sub>  | 0                        |        | 0                        |        | 0                        |        | ns   | 14     |
| Read Command Hold Time Referenced to $\overline{\text{CAS}}$             | t <sub>RCH</sub>  | 0                        |        | 0                        |        | 0                        |        | ns   | 14     |
| $\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{CAS}}$   | t <sub>WCH</sub>  | 7                        |        | 10                       |        | 10                       |        | ns   | 15     |
| $\overline{\text{WE}}$ Pulse Width                                       | t <sub>WP</sub>   | 7                        |        | 10                       |        | 10                       |        | ns   | 15     |
| Data-in Setup Time   | t <sub>DS</sub>   | 0                        |        | 0                        |        | 0                        |        | ns   | 16     |
| Data-in Hold Time  | t <sub>DH</sub>   | 7                        |        | 10                       |        | 10                       |        | ns   | 16     |
| Write Command Setup Time   | t <sub>WCS</sub>  | 0                        |        | 0                        |        | 0                        |        | ns   | 17     |
| $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time             | t <sub>CWD</sub>  | 27                       |        | 32                       |        | 37                       |        | ns   | 17     |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time             | t <sub>RWD</sub>  | 64                       |        | 77                       |        | 89                       |        | ns   | 17     |
| Column Address to $\overline{\text{WE}}$ Delay Time                      | t <sub>AWD</sub>  | 39                       |        | 47                       |        | 54                       |        | ns   | 17     |

(2/2)

| Parameter  | Symbol           | t <sub>RAC</sub> = 50 ns |      | t <sub>RAC</sub> = 60 ns |      | t <sub>RAC</sub> = 70 ns |      | Unit | Notes |
|--|------------------|--------------------------|------|--------------------------|------|--------------------------|------|------|-------|
|  |                  | MIN.                     | MAX. | MIN.                     | MAX. | MIN.                     | MAX. |      |       |
| WE Lead Time Referenced to $\overline{\text{RAS}}$ | t <sub>RWL</sub> | 7                        |      | 10                       |      | 12                       |      | ns   |       |
| WE Lead Time Referenced to CAS                     | t <sub>CWL</sub> | 7                        |      | 10                       |      | 12                       |      | ns   |       |
| CAS Setup Time for CAS before RAS Refresh          | t <sub>CSR</sub> | 5                        |      | 5                        |      | 5                        |      | ns   |       |
| CAS Hold Time for CAS before RAS Refresh           | t <sub>CHR</sub> | 10                       |      | 10                       |      | 10                       |      | ns   |       |
| WE Setup Time                                      | t <sub>WSR</sub> | 10                       |      | 10                       |      | 10                       |      | ns   |       |
| WE Hold Time                                       | t <sub>WHR</sub> | 15                       |      | 15                       |      | 15                       |      | ns   |       |
| Refresh Time                                       | t <sub>REF</sub> |                          | 64   |                          | 64   |                          | 64   | ms   |       |

**HYPER PAGE MODE**

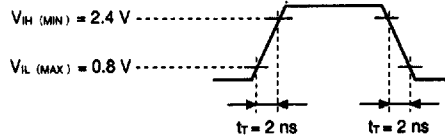
| Parameter   | Symbol             | t <sub>RAC</sub> = 50 ns |         | t <sub>RAC</sub> = 60 ns |         | t <sub>RAC</sub> = 70 ns |         | Unit | Notes  |
|---|--------------------|--------------------------|---------|--------------------------|---------|--------------------------|---------|------|--------|
|   |                    | MIN.                     | MAX.    | MIN.                     | MAX.    | MIN.                     | MAX.    |      |        |
| Read / Write Cycle Time                                   | t <sub>HPC</sub>   | 20                       |         | 25                       |         | 30                       |         | ns   |        |
| RAS Pulse Width   | t <sub>RASP</sub>  | 50                       | 125 000 | 60                       | 125 000 | 70                       | 125 000 | ns   |        |
| CAS Pulse Width   | t <sub>HCAS</sub>  | 7                        | 10 000  | 10                       | 10 000  | 12                       | 10 000  | ns   |        |
| CAS Precharge Time  | t <sub>CP</sub>    | 7                        |         | 10                       |         | 10                       |         | ns   |        |
| CAS Precharge to WE Delay Time                            | t <sub>CPWD</sub>  | 41                       |         | 52                       |         | 59                       |         | ns   | 17     |
| Read Modify Write Cycle Time                              | t <sub>HPRWC</sub> | 52                       |         | 66                       |         | 75                       |         | ns   |        |
| Data Output Hold Time                                     | t <sub>DHC</sub>   | 5                        |         | 5                        |         | 5                        |         | ns   |        |
| Output Buffer Turn-off Delay from WE                      | t <sub>WEZ</sub>   | 0                        | 10      | 0                        | 13      | 0                        | 15      | ns   | 12, 18 |
| WE Pulse Width  | t <sub>WPZ</sub>   | 7                        |         | 10                       |         | 10                       |         | ns   | 18     |
| Output Buffer Turn-off Delay from $\overline{\text{RAS}}$ | t <sub>OFR</sub>   | 0                        | 10      | 0                        | 13      | 0                        | 15      | ns   | 12, 18 |
| Output Buffer Turn-off Delay from $\overline{\text{CAS}}$ | t <sub>OFC</sub>   | 0                        | 10      | 0                        | 13      | 0                        | 15      | ns   | 12, 18 |

- Notes**
1. All voltages are referenced to GND.
  2. After power up, wait more than 100 μs and then, execute eight  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  or  $\overline{\text{RAS}}$  only refresh cycles as dummy cycles to initialize internal circuit.
  3. t<sub>CC1</sub>, t<sub>CC3</sub>, t<sub>CC4</sub> and t<sub>CC5</sub> depend on cycle rates ( t<sub>RAC</sub> and t<sub>HPC</sub> ).
  4. Specified values are obtained with outputs unloaded.
  5. t<sub>CC3</sub> is measured assuming that all column address inputs are held at either high or low.
  6. t<sub>CC4</sub> is measured assuming that all column address inputs are switched only once during each hyper page cycle.
  7. t<sub>CC1</sub> and t<sub>CC3</sub> are measured assuming that address can be changed once or less during  $\overline{\text{RAS}} \leq V_{IL(MAX)}$  and  $\overline{\text{CAS}} \geq V_{IH(MIN)}$ .

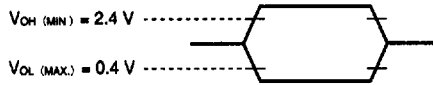


- Notes**
8. AC measurements assume  $t_r = 2 \text{ ns}$ .
  9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows :

| Input Conditions  | Access Time                   | Access Time from $\overline{\text{RAS}}$       |
|---|-------------------------------|--|
| $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$ | $t_{\text{RAC}}(\text{MAX.})$ | $t_{\text{RAC}}(\text{MAX.})$                  |
| $t_{\text{RAD}} > t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$    | $t_{\text{AA}}(\text{MAX.})$  | $t_{\text{RAD}} + t_{\text{AA}}(\text{MAX.})$  |
| $t_{\text{RCD}} > t_{\text{RCD}}(\text{MAX.})$  | $t_{\text{CAC}}(\text{MAX.})$ | $t_{\text{RCD}} + t_{\text{CAC}}(\text{MAX.})$ |

$t_{\text{RAD}}(\text{MAX.})$  and  $t_{\text{RCD}}(\text{MAX.})$  are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time ( $t_{\text{RAC}}$ ,  $t_{\text{AA}}$  or  $t_{\text{CAC}}$ ) is to be used for finding out when output data will be available. Therefore, the input conditions  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{MAX.})$  and  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX.})$  will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12.  $t_{\text{OFC}}(\text{MAX.})$ ,  $t_{\text{OFR}}(\text{MAX.})$ ,  $t_{\text{WEZ}}(\text{MAX.})$ , and  $t_{\text{OEZ}}(\text{MAX.})$  define the time when the output achieves the condition of Hi-Z and is not referenced to  $V_{\text{OH}}$  or  $V_{\text{OL}}$ .
13.  $t_{\text{CRP}}(\text{MIN.})$  requirement is applied for  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  cycles preceded by any cycles.
14. Either  $t_{\text{TRCH}}(\text{MIN.})$  or  $t_{\text{TRRH}}(\text{MIN.})$  should be met in read cycles.
15.  $t_{\text{WP}}(\text{MIN.})$  is applied for late write cycles or read modify write cycles. In early write cycles,  $t_{\text{WCH}}(\text{MIN.})$  should be met.
16.  $t_{\text{DS}}(\text{MIN.})$  and  $t_{\text{DH}}(\text{MIN.})$  are referenced to the  $\overline{\text{CAS}}$  falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the  $\overline{\text{WE}}$  falling edge.
17. If  $t_{\text{WCs}} \geq t_{\text{WCs}}(\text{MIN.})$ , the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If  $t_{\text{RWd}} \geq t_{\text{RWd}}(\text{MIN.})$ ,  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{MIN.})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{MIN.})$  and  $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{MIN.})$ , the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
18. To make I/Os to Hi-Z in read cycle, it is necessary to control  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$  as follows. The effective specification depends on state of each signal.

(1)  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ : inactive (at the end of read cycle)

$\overline{\text{WE}}$ : inactive,  $\overline{\text{OE}}$ : active

$t_{\text{OFC}}$  is effective when  $\overline{\text{RAS}}$  is inactivated before  $\overline{\text{CAS}}$  is inactivated.

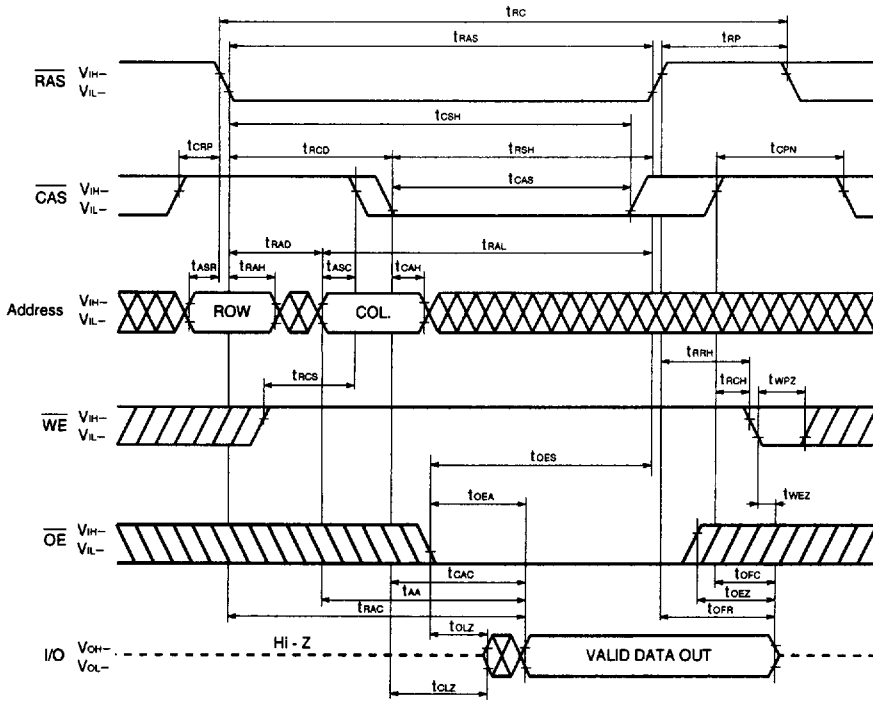
$t_{\text{OFR}}$  is effective when  $\overline{\text{CAS}}$  is inactivated before  $\overline{\text{RAS}}$  is inactivated.

(2) Both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are active or either  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$  is active (in read cycle)

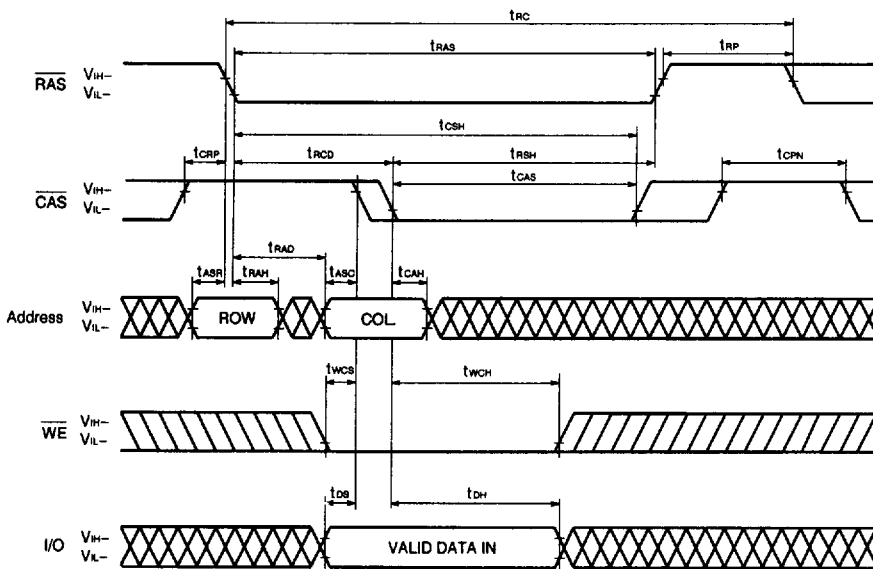
$\overline{\text{WE}}$ : active,  $\overline{\text{OE}}$ : active... $t_{\text{WEZ}}$ ,  $t_{\text{WPZ}}$  are effective.

$\overline{\text{WE}}$ : inactive,  $\overline{\text{OE}}$ : inactive... $t_{\text{OEZ}}$  is effective.

READ CYCLE



EARLY WRITE CYCLE



Remark  $\overline{OE}$  = Don't Care



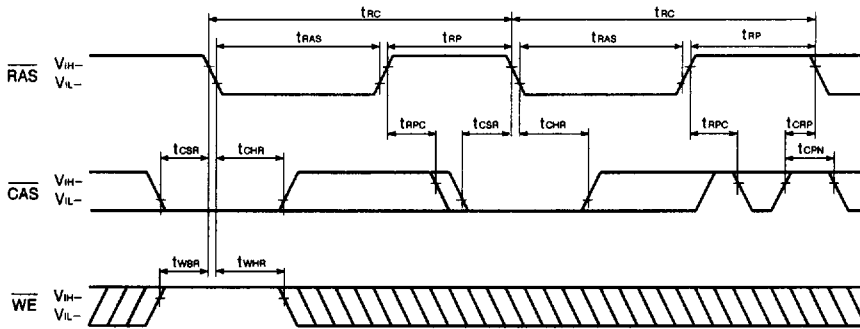






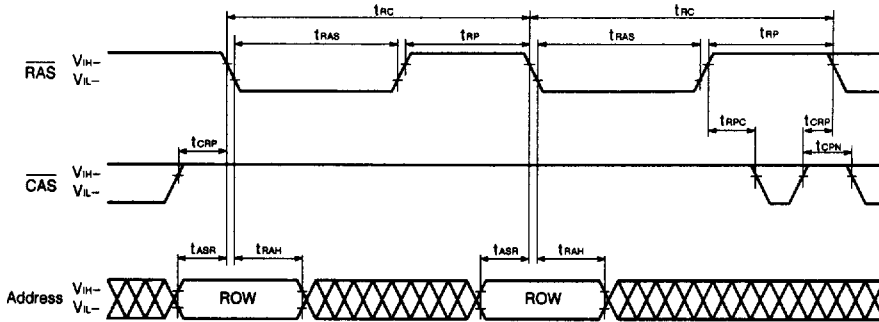


**CAS BEFORE RAS REFRESH CYCLE**



Remark Address,  $\overline{OE}$  = Don't care I/O = Hi - Z

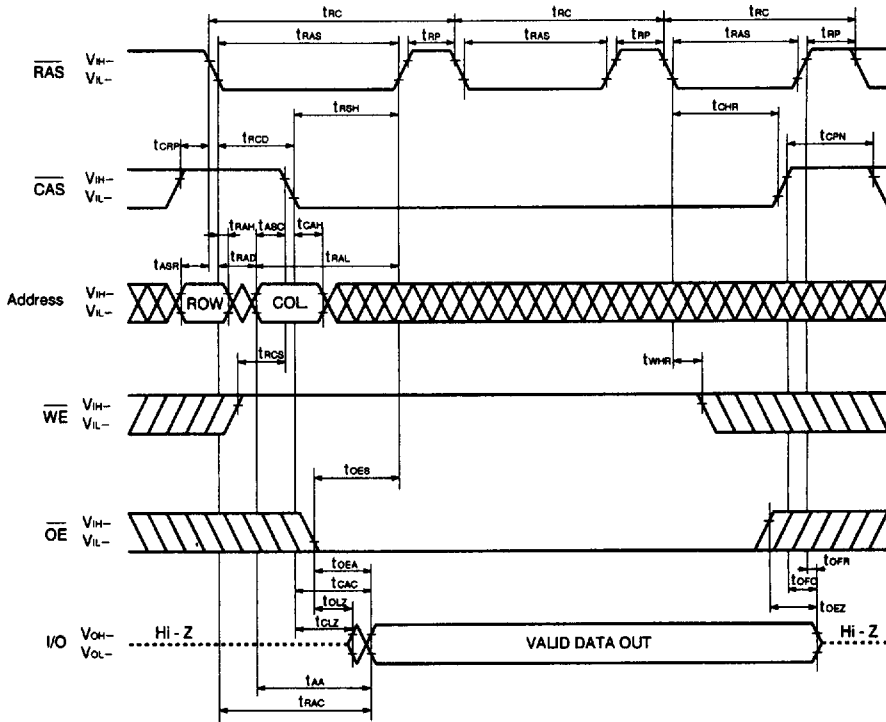
**RAS ONLY REFRESH CYCLE,**



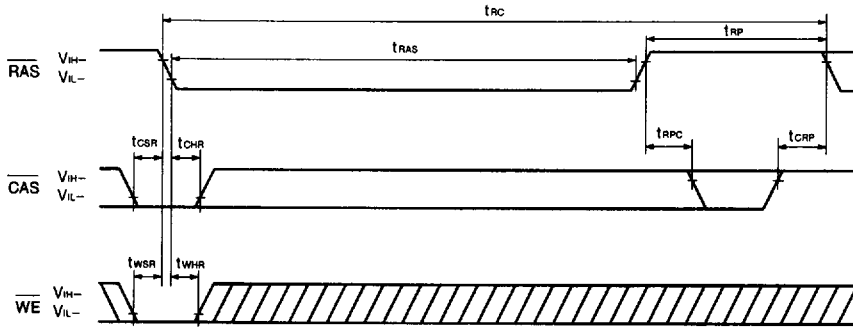
Remark  $\overline{WE}$ ,  $\overline{OE}$  = Don't care I/O = Hi - Z



HIDDEN REFRESH CYCLE



**TEST MODE SET CYCLE ( $\overline{\text{WE}}$ ,  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH CYCLE)**



Remark Address,  $\overline{\text{OE}}$  = Don't care I/O = Hi - Z

**TEST MODE**

TEST MODE is fast test function. On using this mode, test time is reduced to 1/2. In this TEST MODE, internal organization is 1 M words by 16 bits apparently. Don't care about the input levels of the column address input A0.

**1. How to enter TEST MODE**

Through TEST MODE SET CYCLE ( $\overline{\text{WE}}$ ,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle), the device enters TEST MODE.

**2. Write / Read in TEST MODE**

Write data of "1" or "0" through I/O1 to I/O8 by controlling address except for above-mentioned address. Each input data through each I/O write 2 bits at once. And read through I/O1 to I/O8 to check written data. In case of writing each 2 bits rightly, each I/O data is "1". But wrong, the data is "0".

**3. Refresh in TEST MODE**

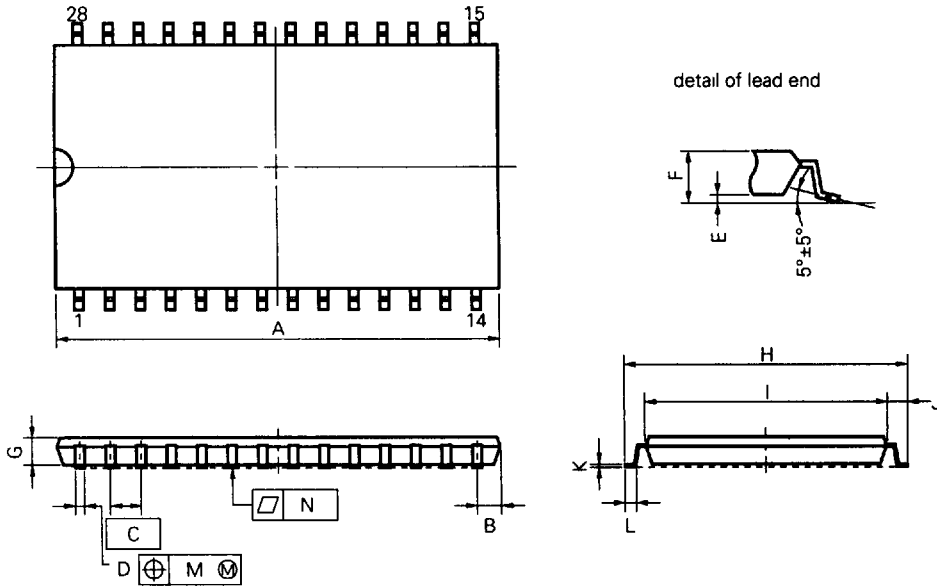
Use normal read cycle or  $\overline{\text{WE}}$ ,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle.

**4. How to exit from TEST MODE**

Through  $\overline{\text{RAS}}$  only refresh cycle or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle, the device exits from TEST MODE.

PACKAGE DRAWINGS

28 PIN PLASTIC TSOP(III) (400 mil)



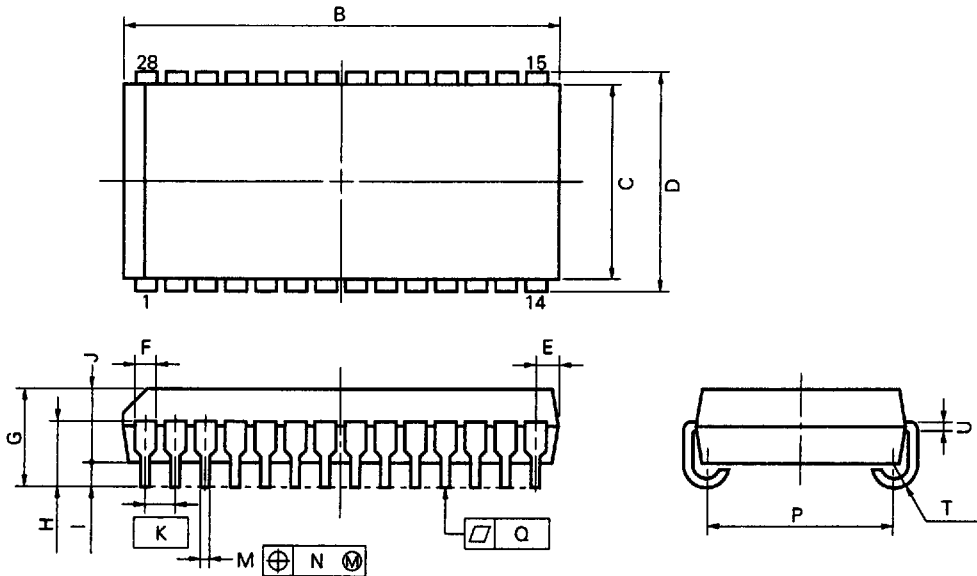
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7JD2-1

| ITEM | MILLIMETERS                               | INCHES                                      |
|------|---|---|
| A    | 18.81 MAX.                                | 0.741 MAX.                                  |
| B    | 1.15 MAX.                                 | 0.046 MAX.                                  |
| C    | 1.27 (T.P.)                               | 0.050 (T.P.)                                |
| D    | 0.40±0.10                                 | 0.016 <sup>+0.004</sup> / <sub>-0.005</sub> |
| E    | 0.05±0.05                                 | 0.002±0.002                                 |
| F    | 1.1 MAX.                                  | 0.044 MAX.                                  |
| G    | 0.97                                      | 0.038                                       |
| H    | 11.76±0.2                                 | 0.463±0.008                                 |
| I    | 10.16±0.1                                 | 0.400±0.004                                 |
| J    | 0.8±0.2                                   | 0.031 <sup>+0.009</sup> / <sub>-0.008</sub> |
| K    | 0.125 <sup>+0.10</sup> / <sub>-0.05</sub> | 0.005 <sup>+0.004</sup> / <sub>-0.002</sub> |
| L    | 0.5±0.1                                   | 0.020 <sup>+0.004</sup> / <sub>-0.005</sub> |
| M    | 0.21                                      | 0.009                                       |
| N    | 0.10                                      | 0.004                                       |

28 PIN PLASTIC SOJ (400 mil)



**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P28LE-400A1

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|--|---|
| B    | 18.67 <sup>+0.2</sup> <sub>-0.35</sub> | 0.735 <sup>+0.008</sup> <sub>-0.013</sub> |
| C    | 10.16                                  | 0.400                                     |
| D    | 11.18±0.2                              | 0.440 <sup>+0.008</sup> <sub>-0.007</sub> |
| E    | 1.08±0.15                              | 0.043 <sup>+0.006</sup> <sub>-0.007</sub> |
| F    | 0.74                                   | 0.029                                     |
| G    | 3.5±0.2                                | 0.138 <sup>+0.008</sup> <sub>-0.007</sub> |
| H    | 2.545±0.2                              | 0.100±0.008                               |
| I    | 0.8 MIN.                               | 0.031 MIN.                                |
| J    | 2.6                                    | 0.102                                     |
| K    | 1.27 (T.P.)                            | 0.050 (T.P.)                              |
| M    | 0.40±0.10                              | 0.016 <sup>+0.004</sup> <sub>-0.005</sub> |
| N    | 0.12                                   | 0.005                                     |
| P    | 9.40±0.20                              | 0.370 <sup>+0.008</sup> <sub>-0.007</sub> |
| Q    | 0.10                                   | 0.004                                     |
| T    | R 0.85                                 | R 0.033                                   |
| U    | 0.20 <sup>+0.10</sup> <sub>-0.08</sub> | 0.008 <sup>+0.004</sup> <sub>-0.002</sub> |

**RECOMMENDED SOLDERING CONDITIONS**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD4216805.

**TYPE OF SURFACE MOUNT DEVICE**

$\mu$ PD4216805G5 : 28-pin Plastic TSOP(III) (400 mil)

$\mu$ PD4216805LE : 28-pin Plastic SOJ (400 mil)