

## 54ACT573

### Octal Latch with TRI-STATE® Outputs

#### General Description

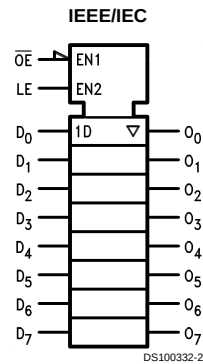
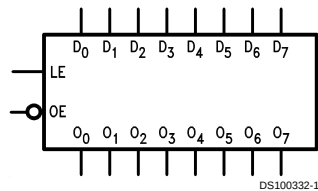
The 'ACT573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ( $\overline{OE}$ ) inputs.

The 'ACT573 is functionally identical to the 'ACT373 but has inputs and outputs on opposite sides.

#### Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT373
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 'ACT573 has TTL-compatible inputs
- Standard Military Drawing (SMD)  
— 'ACT573: 5962-87664

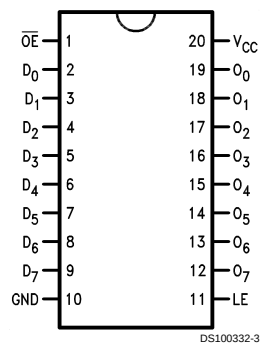
#### Logic Symbols



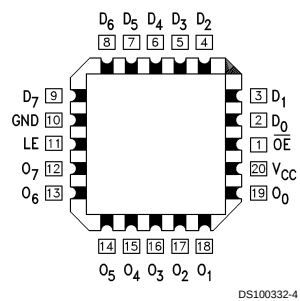
| Pin Names       | Description                   |
|-----------------|-------------------------------|
| $D_0$ – $D_7$   | Data Inputs                   |
| LE              | Latch Enable Input            |
| $\overline{OE}$ | TRI-STATE Output Enable Input |
| $O_0$ – $O_7$   | TRI-STATE Latch Outputs       |

## Connection Diagrams

Pin Assignment for DIP  
and Flatpak



Pin Assignment for LCC



## Functional Description

The 'ACT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are enabled. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

## Truth Table

| Inputs          |    |   | Outputs |
|-----------------|----|---|---------|
| $\overline{OE}$ | LE | D | $O_n$   |
| L               | H  | H | H       |
| L               | H  | L | L       |
| L               | L  | X | $O_0$   |
| H               | X  | X | Z       |

H = HIGH Voltage

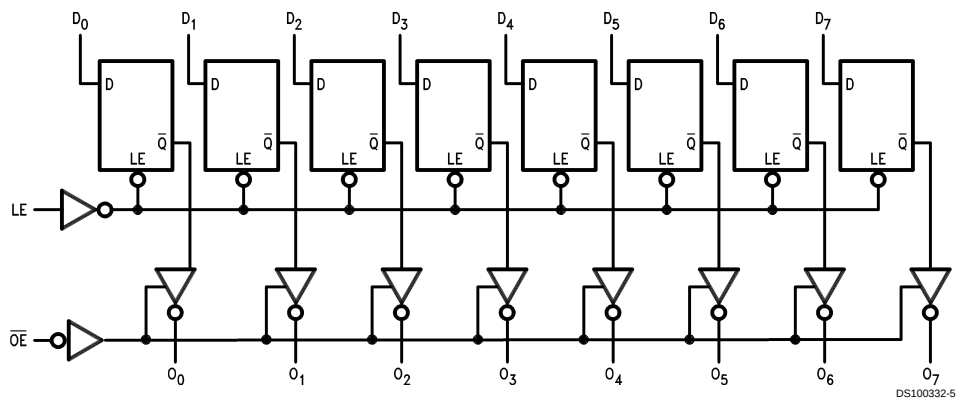
L = LOW Voltage

Z = High Impedance

X = Immaterial

$O_0$  = Previous  $O_0$  before HIGH-to-LOW transition of Latch Enable

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DS100332-5

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

|                                                                        |                          |
|------------------------------------------------------------------------|--------------------------|
| Supply Voltage ( $V_{CC}$ )                                            | -0.5V to +7.0V           |
| DC Input Diode Current ( $I_{IK}$ )                                    |                          |
| $V_I = -0.5V$                                                          | -20 mA                   |
| $V_I = V_{CC} + 0.5V$                                                  | +20 mA                   |
| DC Input Voltage ( $V_I$ )                                             | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Diode Current ( $I_{OK}$ )                                   |                          |
| $V_O = -0.5V$                                                          | -20 mA                   |
| $V_O = V_{CC} + 0.5V$                                                  | +20 mA                   |
| DC Output Voltage ( $V_O$ )                                            | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Source or Sink Current ( $I_O$ )                             | ±50 mA                   |
| DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ ) | ±50 mA                   |
| Storage Temperature ( $T_{STG}$ )                                      | -65°C to +150°C          |

Junction Temperature ( $T_J$ )

CDIP

175°C

**Recommended Operating Conditions**

|                                                 |                 |
|-------------------------------------------------|-----------------|
| Supply Voltage ( $V_{CC}$ )                     |                 |
| 'ACT                                            | 4.5V to 5.5V    |
| Input Voltage ( $V_I$ )                         | 0V to $V_{CC}$  |
| Output Voltage ( $V_O$ )                        | 0V to $V_{CC}$  |
| Operating Temperature ( $T_A$ )                 |                 |
| 54ACT                                           | -55°C to +125°C |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) |                 |
| 'ACT Devices                                    |                 |
| $V_{IN}$ from 0.8V to 2.0V                      |                 |
| $V_{CC}$ @ 4.5V, 5.5V                           | 125 mV/ns       |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

**DC Characteristics for 'ACT Family Devices**

| Symbol    | Parameter                               | $V_{CC}$<br>(V) | 54ACT                      | Units              | Conditions                                                             |
|-----------|-----------------------------------------|-----------------|----------------------------|--------------------|------------------------------------------------------------------------|
|           |                                         |                 | $T_A =$<br>-55°C to +125°C |                    |                                                                        |
|           |                                         |                 | Guaranteed Limits          |                    |                                                                        |
| $V_{IH}$  | Minimum High Level Input Voltage        | 4.5             | 2.0                        | V                  | $V_{OUT} = 0.1V$                                                       |
|           |                                         | 5.5             | 2.0                        |                    | or $V_{CC} - 0.1V$                                                     |
| $V_{IL}$  | Maximum Low Level Input Voltage         | 4.5             | 0.8                        | V                  | $V_{OUT} = 0.1V$                                                       |
|           |                                         | 5.5             | 0.8                        | or $V_{CC} - 0.1V$ |                                                                        |
| $V_{OH}$  | Minimum High Level Output Voltage       | 4.5             | 4.4                        | V                  | $I_{OUT} = -50 \mu A$                                                  |
|           |                                         | 5.5             | 5.4                        |                    |                                                                        |
|           |                                         | 4.5             | 3.70                       | V                  | (Note 2)<br>$V_{IN} = V_{IL}$ or $V_{IH}$<br>$I_{OH} = -24 \text{ mA}$ |
|           |                                         | 5.5             | 4.70                       |                    | $-24 \text{ mA}$                                                       |
| $V_{OL}$  | Maximum Low Level Output Voltage        | 4.5             | 0.1                        | V                  | $I_{OUT} = 50 \mu A$                                                   |
|           |                                         | 5.5             | 0.1                        |                    |                                                                        |
|           |                                         | 4.5             | 0.50                       | V                  | (Note 2)<br>$V_{IN} = V_{IL}$ or $V_{IH}$<br>$I_{OL} = 24 \text{ mA}$  |
|           |                                         | 5.5             | 0.50                       |                    | $24 \text{ mA}$                                                        |
| $I_{IN}$  | Maximum Input Leakage Current           | 5.5             | ±1.0                       | μA                 | $V_I = V_{CC}, GND$                                                    |
| $I_{OZ}$  | Maximum TRI-STATE Leakage Current       | 5.5             | ±5.0                       | μA                 | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$                          |
| $I_{CCT}$ | Maximum $I_{CC}/Input$                  | 5.5             | 1.6                        | mA                 | $V_I = V_{CC} - 2.1V$                                                  |
| $I_{OLD}$ | (Note 3) Minimum Dynamic Output Current | 5.5             | 50                         | mA                 | $V_{OLD} = 1.65V \text{ Max}$                                          |
| $I_{OHD}$ |                                         | 5.5             | -50                        | mA                 | $V_{OHD} = 3.85V \text{ Min}$                                          |

## DC Characteristics for 'ACT Family Devices (Continued)

| Symbol          | Parameter                           | V <sub>CC</sub><br>(V) | 54ACT                               | Units | Conditions                                  |
|-----------------|-------------------------------------|------------------------|-------------------------------------|-------|---------------------------------------------|
|                 |                                     |                        | T <sub>A</sub> =<br>–55°C to +125°C |       |                                             |
|                 |                                     |                        | Guaranteed<br>Limits                |       |                                             |
| I <sub>CC</sub> | Maximum Quiescent<br>Supply Current | 5.5                    | 80.0                                | μA    | V <sub>IN</sub> = V <sub>CC</sub><br>or GND |

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics

| Symbol           | Parameter                                             | V <sub>CC</sub><br>(V)<br>(Note 5) | 54ACT                                                         |      | Units | Fig.<br>No. |
|------------------|-------------------------------------------------------|------------------------------------|---------------------------------------------------------------|------|-------|-------------|
|                  |                                                       |                                    | T <sub>A</sub> = –55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |      |       |             |
|                  |                                                       |                                    | Min                                                           | Max  |       |             |
| t <sub>PLH</sub> | Propagation Delay<br>D <sub>m</sub> to O <sub>n</sub> | 5.0                                | 1.5                                                           | 13.5 | ns    |             |
| t <sub>PHL</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 5.0                                | 1.5                                                           | 13.5 | ns    |             |
| t <sub>PLH</sub> | Propagation Delay<br>LE to O <sub>n</sub>             | 5.0                                | 1.5                                                           | 13.0 | ns    |             |
| t <sub>PHL</sub> | Propagation Delay<br>LE to O <sub>n</sub>             | 5.0                                | 1.5                                                           | 12.0 | ns    |             |
| t <sub>PZH</sub> | Output Enable Time                                    | 5.0                                | 1.5                                                           | 11.5 | ns    |             |
| t <sub>PZL</sub> | Output Enable Time                                    | 5.0                                | 1.5                                                           | 11.0 | ns    |             |
| t <sub>PHZ</sub> | Output Disable Time                                   | 5.0                                | 1.5                                                           | 13.5 | ns    |             |
| t <sub>PLZ</sub> | Output Disable Time                                   | 5.0                                | 1.5                                                           | 10.5 | ns    |             |

**Note 5:** Voltage Range 5.0 is 5.0V ±0.5V

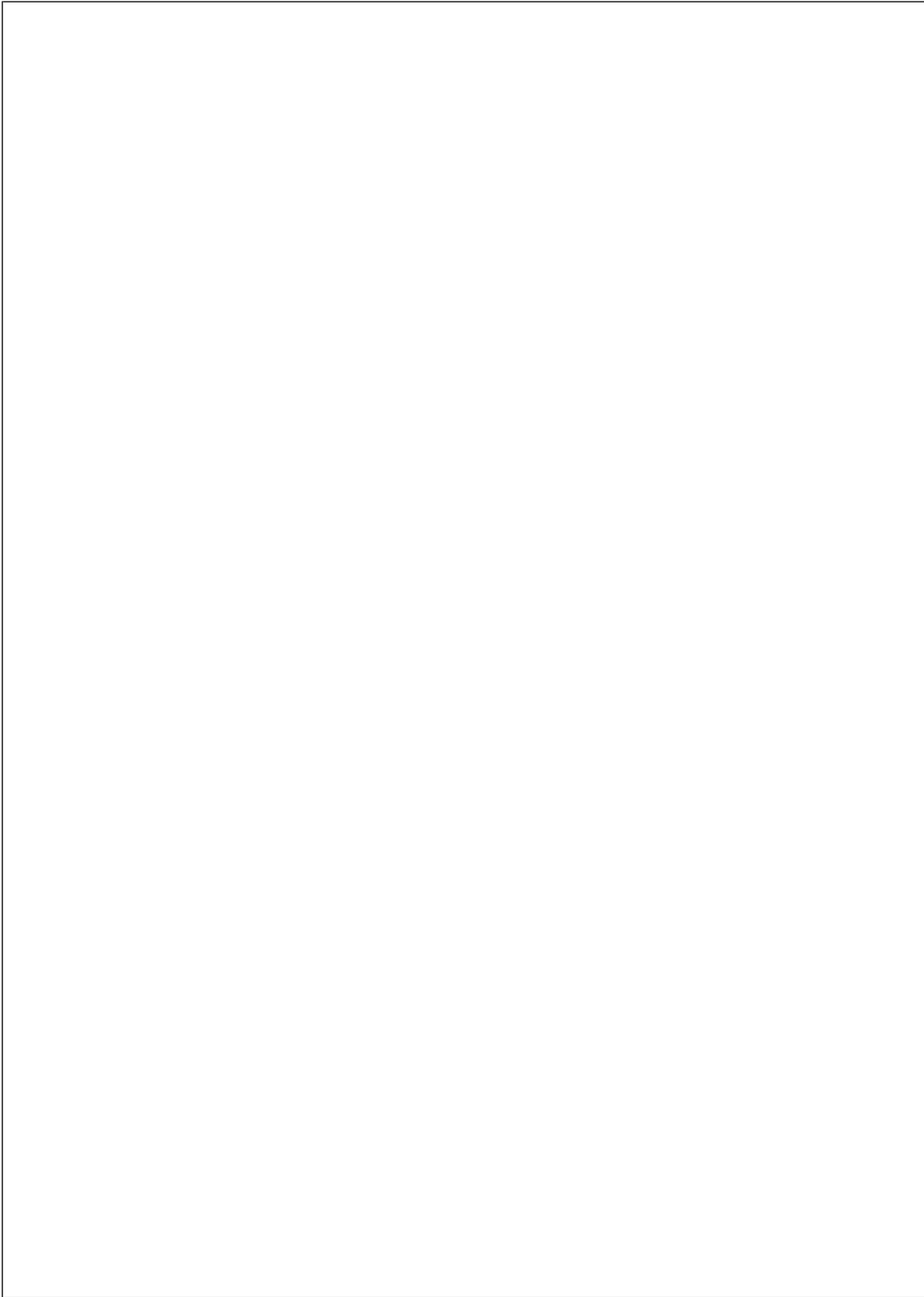
## AC Operating Requirements

| Symbol         | Parameter                                       | V <sub>CC</sub><br>(V)<br>(Note 6) | 54ACT                                                         | Units | Fig.<br>No. |
|----------------|-------------------------------------------------|------------------------------------|---------------------------------------------------------------|-------|-------------|
|                |                                                 |                                    | T <sub>A</sub> = –55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |       |             |
|                |                                                 |                                    | Guaranteed<br>Minimum                                         |       |             |
| t <sub>s</sub> | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | 5.0                                | 4.5                                                           | ns    |             |
| t <sub>h</sub> | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE  | 5.0                                | 1.0                                                           | ns    |             |
| t <sub>w</sub> | LE Pulse Width, HIGH                            | 5.0                                | 5.0                                                           | ns    |             |

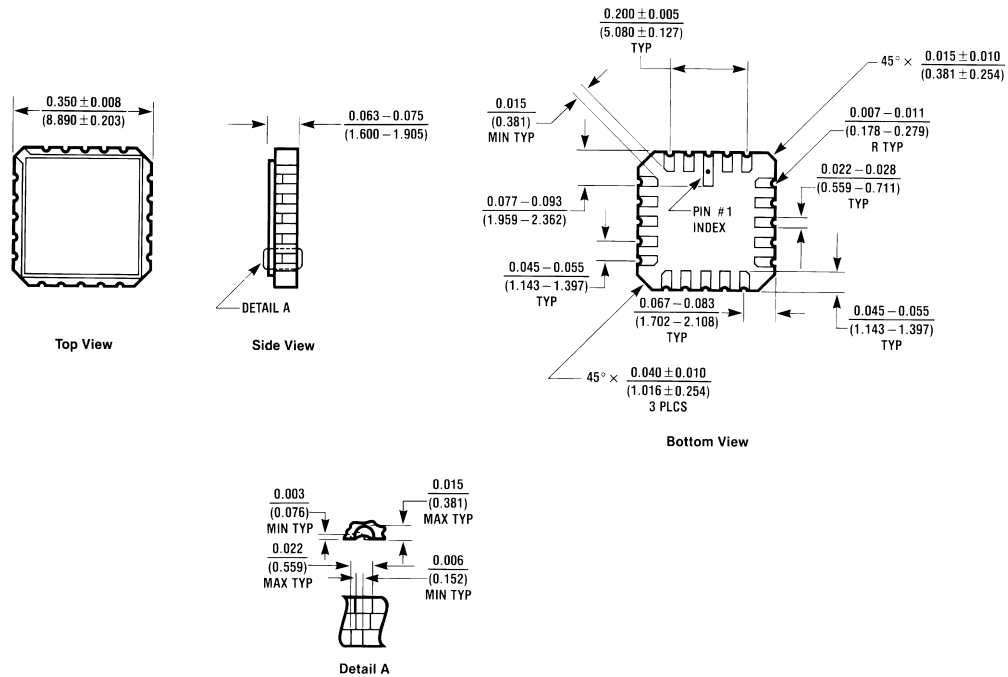
**Note 6:** Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

| Symbol   | Parameter                        | Typ  | Units | Conditions             |
|----------|----------------------------------|------|-------|------------------------|
| $C_{IN}$ | Input Capacitance                | 5.0  | pF    | $V_{CC} = \text{OPEN}$ |
| $C_{PD}$ | Power Dissipation<br>Capacitance | 25.0 | pF    | $V_{CC} = 5.0V$        |



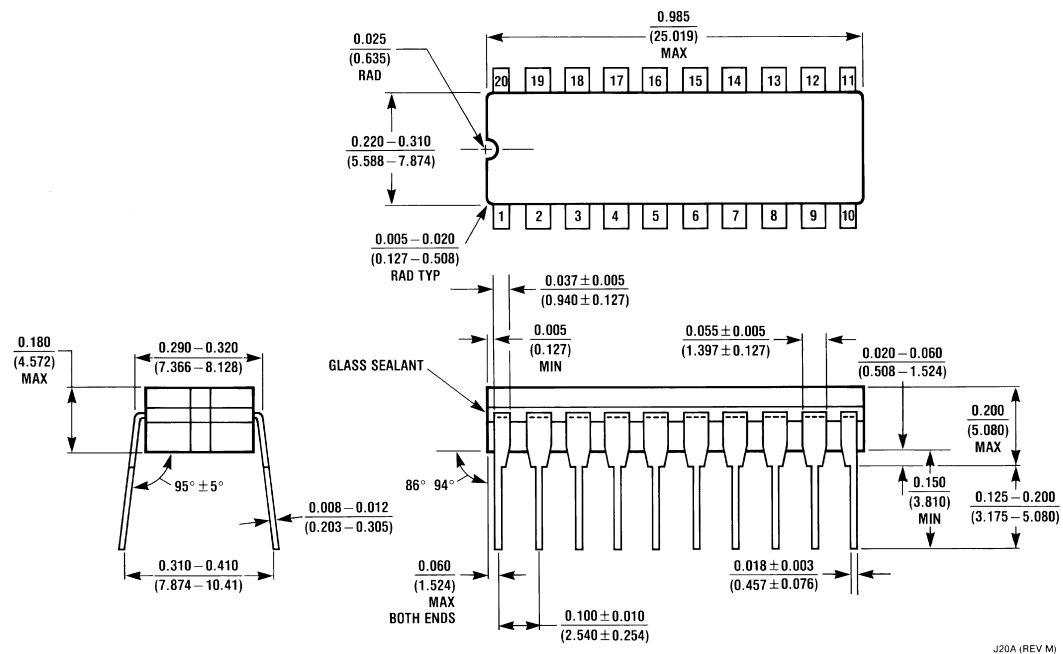
**Physical Dimensions** inches (millimeters) unless otherwise noted



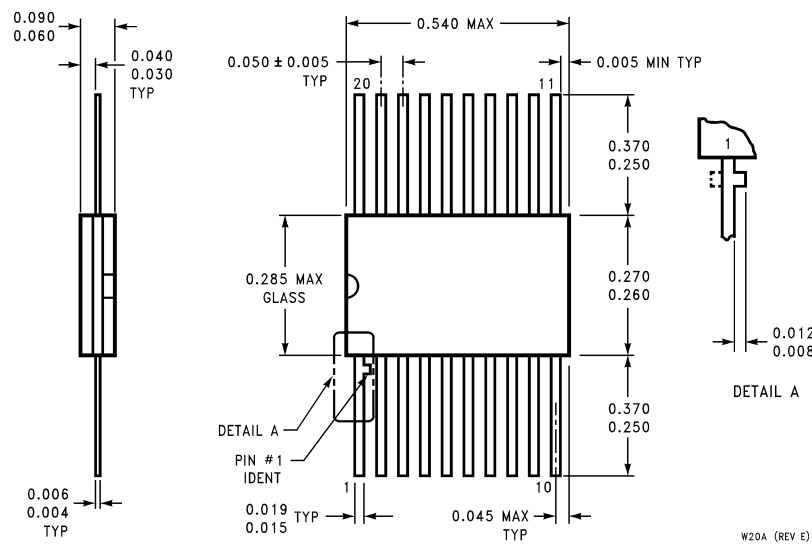
E20A (REV D)

**20 Terminal Ceramic Leadless Chip Carrier (L)  
NS Package Number E20A**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

**20-Lead Ceramic Dual-In-Line Package (D)**  
**NS Package Number J20A**



**20-Lead Ceramic Flatpak (F)**  
**NS Package Number W20A**

