Am99C641/Am99CL641

65,536 x 1 Static Read/Write Random-Access Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

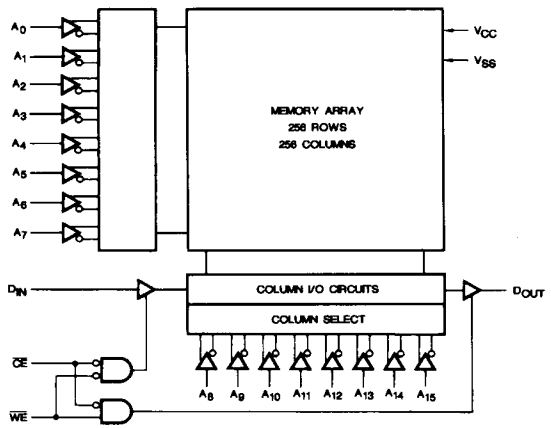
- High-performance CMOS circuit design and process
- High Speed – access times as fast as 25 ns
- Single 5-V ±10% power-supply operation
- Low power – 550 mW active
  110 mW TTL – Standby
- 2 V data retention for battery back up applications
- Fully static — no clocks or timing signals required
- Standard 22-pin slim (0.300 inch) DIP, (plastic and ceramic), and 22-pin rectangular ceramic leadless chip carriers.

GENERAL DESCRIPTION

The Am99C641 is a high-performance, Static CMOS, read/write random-access memory organized as 65,536 words with 1 bit per word. The Am99C641 features single 5-V operation with automatic power-down capability. All inputs and outputs are fully TTL–compatible. There are separate data input and output pins which, along with the two control signals $\overline{CE}$ and $\overline{WE}$, provide ease of expansion in large memory-array applications.

In addition to low TTL-level standby power, this device offers a low CMOS-level standby power of 1.65 mW and a low data retention current of 0.1 mA with V_{CC} at 2 V.

BLOCK DIAGRAM



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Publication # 07438 Rev. D Amendment /0
Issue Date: June 1987

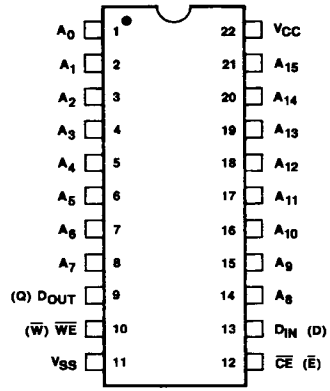
PRODUCT SELECTOR GUIDE

Family Part No.			Am99C641/Am99CL641				
Ordering Part No.			-25	-35	-45	-55	-70
Access Time (ns)			25	35	45	55	70
	Symbol	Power*					
Commercial (C) Devices: 0 to +70°C	I_{CC} (mA)	S	120	110	100	90	85
		L	100	90	85	80	80
	I_{SB1} (mA)	S	55	45	40	40	40
		L	20	20	20	20	20
	I_{SB2} (mA)	S	20	20	20	20	20
		L	10	10	10	10	10
	I_{SB3} (mA)	S	15	15	15	15	15
		L	0.3	0.3	0.3	0.3	0.3
	I_{CCDR} (mA) @ 2 V	S	–	–	–	–	–
		L	0.1	0.1	0.1	0.1	0.1
Extended Commercial (E) and Military (M) Devices -55 to +125°C	I_{CC} (mA)	S	–	120	110	100	95
		L	–	100	95	90	90
	I_{SB1} (mA)	S	–	50	45	45	45
		L	–	20	20	20	20
	I_{SB2} (mA)	S	–	30	30	30	30
		L	–	15	15	15	15
	I_{SB3} (mA)	S	–	20	20	20	20
		L	–	1.5	1.5	1.5	1.5
	I_{CCDR} (mA) @ 2 V	S	–	–	–	–	–
		L	–	0.3	0.3	0.3	0.3

*S = Standard Power (Am99C641)
L = Low Power (Am99CL641)

CONNECTION DIAGRAMS
Top View

DIPs



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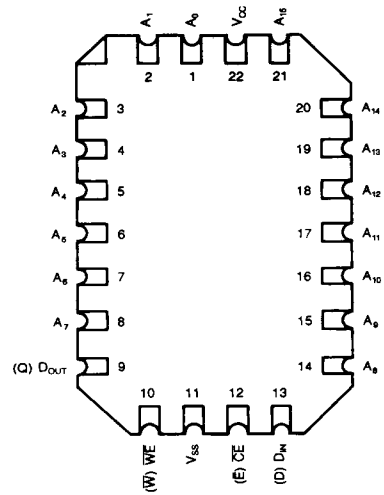
LCC



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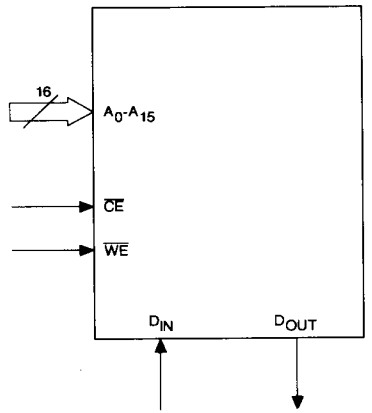
Note: Pin 1 is marked for orientation.
IEEE Nomenclature in Brackets.

LOGIC SYMBOL



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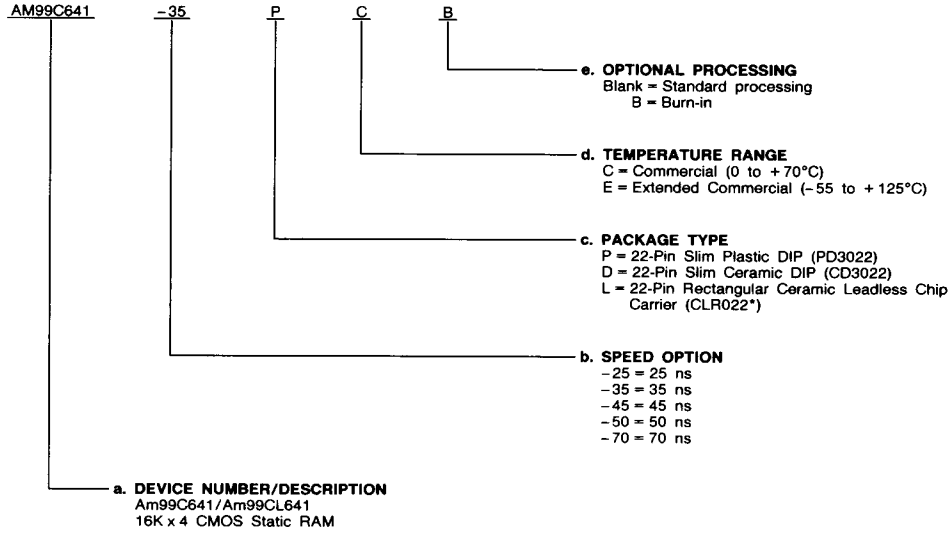
VCC = Power Supply
VSS = Ground

Address Designators	
External	**Internal**
A_0	A_2
A_1	A_3
A_2	A_5
A_3	A_6
A_4	A_7
A_5	A_{12}
A_6	A_{10}
A_7	A_{11}
A_8	A_9
A_9	A_8
A_{10}	A_{14}
A_{11}	A_{13}
A_{12}	A_0
A_{13}	A_1
A_{14}	A_4
A_{15}	A_{15}

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM99C641-25	PC, PCB, DC, DCB, LC, LCB
AM99CL641-25	
AM99C641-35	PC, PCB, DC, DCB, DE, DEB, LC, LCB, LE, LEB
AM99CL641-35	
AM99C641-45	
AM99CL641-45	
AM99C641-55	
AM99CL641-55	
AM99C641-70	
AM99CL641-70	

*Preliminary. Subject to Change.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

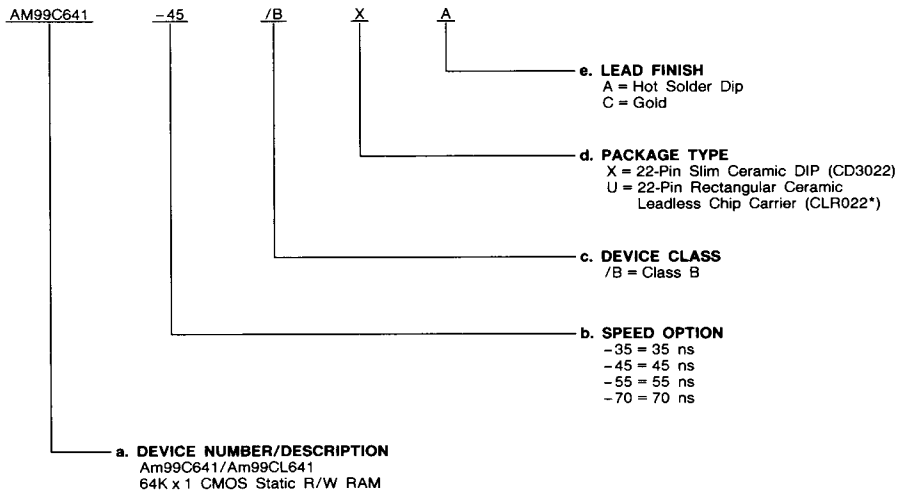
APL and CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) is formed by a combination of:

APL Products:
a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

CPL Products:
a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. CPL Status

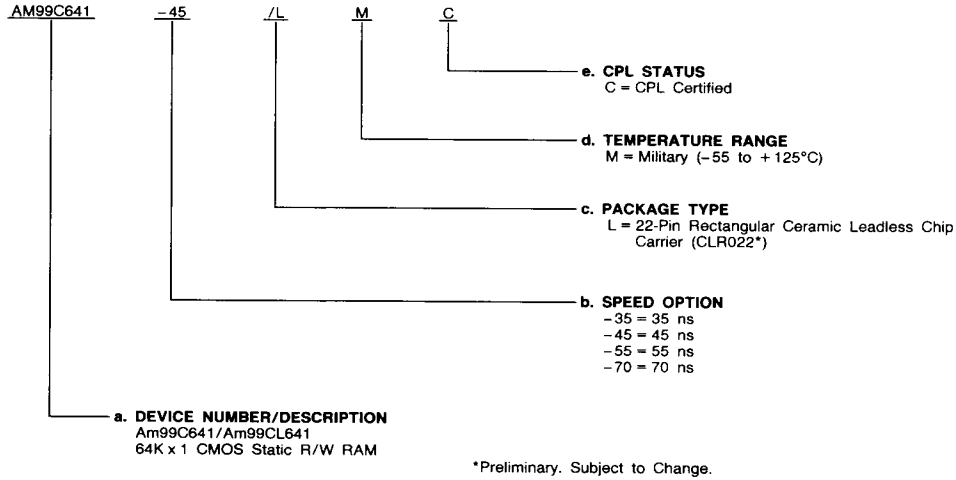
APL Products



*Preliminary. Subject to Change.

ORDERING INFORMATION (Cont'd.)

CPL Products



*Preliminary. Subject to Change.

	Valid Combinations	
APL	AM99C641-35	/BXA, /BXC, /BUA
	AM99CL641-35	
	AM99C641-45	
	AM99CL641-45	
	AM99C641-55	
	AM99CL641-55	
	AM99C641-70	
	AM99CL641-70	
CPL	AM99C641-35	/LMC
	AM99CL641-35	
	AM99C641-45	
	AM99CL641-45	
	AM99C641-55	
	AM99CL641-55	
	AM99C641-70	
	AM99CL641-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A_0-A_{15} Address (Inputs)
The Address input lines select the RAM location to be read or written.

$\overline{CE}$ $\overline{\text{Chip Enable}}$ (Input, Active LOW)
The Chip Enable selects the memory device. $\overline{WE}$ is ignored when $\overline{CE}$ is HIGH.

$\overline{WE}$ $\overline{\text{Write Enable}}$ (Input, Active LOW)
When $\overline{WE}$ is LOW and $\overline{CE}$ is LOW, data will be written into the location specified on the Address pins. When $\overline{WE}$ is HIGH and $\overline{CE}$ is LOW, data will be read out and placed on the D_{OUT} pin.

D_{IN} Data Input
This pin is used for entering data during write operations.

D_{OUT} Data Output (Three-State)
This pin is three-state during write operations. It becomes active when $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH.

V_{CC} Power Supply

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature
- Ceramic Packages ..... −65 to +150°C
- Plastic Packages ..... −55 to +125°C

Ambient Temperature with Power Applied
- Ceramic Packages ..... −55 to +125°C
- Plastic Packages ..... −10 to +85°C

DC Supply Voltage
- to Ground Potential Continuous ..... −0.5 to +7.0 V

All Signal Voltages ..... −0.5 to +7.0 V
DC Output Current ..... 20 mA
Power Dissipation ..... 1.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
- Temperature (T_A) ..... 0 to +70°C
- Supply Voltage (V_{CC}) ..... 4.5 to +5.5 V

Extended Commercial (E) and Military (M) Devices
- Temperature (T_A) ..... −55 to +125°C
- Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 1.0	V
V_{IL}	Input LOW Voltage	(Note 9)	−0.5	0.8	V
$\|I_{IX}\|$	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		2.0	μA
$\|I_{OZ}\|$	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, $\overline{CE}$ ≥ V_{IH}		2.0	μA

DC CHARACTERISTICS over Commercial (0 to +70°C) Operating Range*

Parameter Symbol	Parameter Description	Test Conditions	Power**	Am99C641/Am99CL641 −25	−35	−45	−55	−70	Units
I_{CC}	Dynamic Operating Supply Current	Cycle = Min., Duty = 100%, $\overline{CE}$ ≤ V_{IL}, I/O = 0 mA	S	120	110	100	90	85	mA
			L	100	90	85	80	80	mA
I_{CC1}	Static Operating Supply Current	$\overline{CE}$ ≤ V_{IL}, I/O = 0 mA	S	90	90	80	80	80	mA
			L	60	60	50	50	50	mA
I_{SB1}	Standby Current, Cycling TTL Levels	$\overline{CE}$ ≥ V_{IH}, V_{CC} = Max., Cycle = Min.	S	55	45	40	40	40	mA
			L	40	35	30	25	20	mA
I_{SB2}	Standby Current, Stable TTL Levels	$\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or ≤ V_{IL}	S	20	20	20	20	20	mA
			L	10	10	10	10	10	mA
I_{SB3}	Standby Current, Stable CMOS Input Levels	$\overline{CE}$ ≥ V_{CC} − 0.2 V, V_{IN} ≥ V_{CC} − 0.2 V or ≤ 0.2 V	S	15	15	15	15	15	mA
			L	0.3	0.3	0.3	0.3	0.3	mA

Notes: See notes following Capacitance table on the following page.

*All values are guaranteed maximum limits.
**S = Standard Power (Am99C641)
L = Low Power (Am99CL641)

DC CHARACTERISTICS over Extended Commercial and Military (−55 to +125°C) Operating Ranges*

Parameter Symbol	Parameter Description	Test Conditions	Power**	Am99C641/Am99CL641				Unit
				−35	−45	−55	−70	
I_{CC}	Dynamic Operating Supply Current	Cycle = Min., Duty = 100%, $\overline{CE} \leq V_{IL}$, I/O = 0 mA	S	120	110	100	95	mA
			L	100	95	90	90	mA
I_{CC1}	Static Operating Supply Current	$\overline{CE} \leq V_{IL}$, I/O = 0 mA	S	100	100	100	100	mA
			L	60	50	50	50	mA
I_{SB1}	Standby Current, Cycling TTL Levels	$\overline{CE} \geq V_{IH}$; V_{CC} = Max., Cycle = Min.	S	50	45	45	45	mA
			L	35	30	25	20	mA
I_{SB2}	Standby Current, Stable TTL Levels	$\overline{CE} \geq V_{IH}$; $V_{IN} = V_{IH}$ or $\leq V_{IL}$	S	30	30	30	30	mA
			L	15	15	15	15	mA
I_{SB3}	Standby Current, Stable CMOS Input Levels	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $\leq$ 0.2 V	S	20	20	20	20	mA
			L	1.5	1.5	1.5	1.5	mA

*All values are guaranteed maximum limits.
**S = Standard Power (Am99C641)
L = Low Power (Am99CL641)

CAPACITANCE†

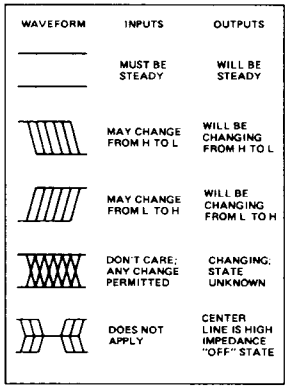
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
C_I††	Input Capacitance	f = 1 MHz, V_{IN} = 0 V		6.0	pF
C_O††	Output Capacitance	V_{OUT} = 0 V		7.0	

† These capacitances are not 100% tested, but are evaluated at initial characterization and at any time the product is modified where capacitance may be affected. Measurement performed at T_A = +25°C.

†† Not included in Group A tests.

Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
3. Parameter not tested—guaranteed by characterization.
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input-pulse levels of 0 to 3.0 V, and output loading of specified I_{OL}/I_{OH} and 30-pF load capacitance. Output timing reference is 1.5 V (see Test Load A in Switching Test Circuits section).
5. The internal write time of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ LOW. Both signals must be active to initiate a write and either signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the transition edge that terminates the write.
6. The minimum limit is not tested and is included for design information only.
7. Parameter not tested, guaranteed by characterization using the load shown in Test Load B—Switching Test Circuits. Transition is measured ±500 mV from steady state voltage.
8. Address input rise and fall times must not exceed 1 μs when $\overline{CE}$ is active. The limit is not tested and is intended for design information only.
9. Undershoot to −3.0 V for a duration of 10 ns between the 50% amplitude point is permissible.

KEY TO SWITCHING WAVEFORMS



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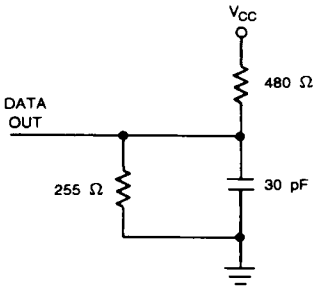
SWITCHING TEST CIRCUITS



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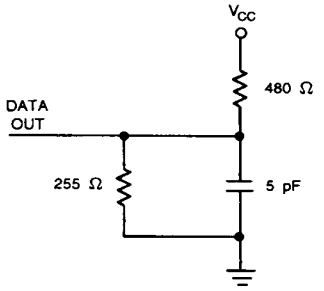
Test Load A



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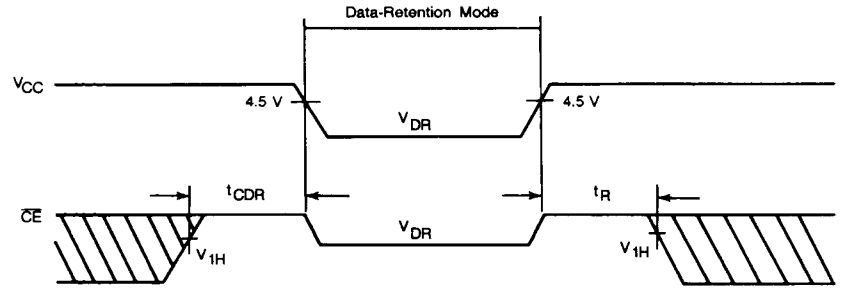
Test Load B

SWITCHING TEST WAVEFORM



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Low V_{CC} Data Retention Characteristics (Low-Power Version Only)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CE} \geq V_{CC} - 0.2$ V		2.0		V
I_{CCDR}	Data Retention Current	V_{CC} = 2 V	COM'L		0.1	mA
			MIL		0.3	
I_{CCDR}	Data Retention Current	V_{CC} = 3 V	COM'L		0.15	mA
			MIL		0.45	
t_{CDR}	Chip Deselect to Data Retention Time (Note 1)	See waveform (Note 2)		0		ns
t_R	Operating Recovery Time (Note 1)			t_{RC}		ns

Notes: 1. Parameter not tested, guaranteed by design.
2. Waveforms shown are not actual and may vary in use.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 7, 8, 9 10, 11 are tested unless otherwise noted) (Note 1)

(Table 1 of 2)

No.	Parameter Symbols		Parameter Description	Am99C641/Am99CL641						Units
				-25		-35		-45		
				Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLES ONE AND TWO (Note 8)										
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		45	ns
4	t_{AXQX}	t_{OH}	Output Hold After Address	3		5		5		ns
5†	t_{ELQX}	t_{LZ}	Chip Enable to Output Active (Note 7)	3		5		5		ns
6†	t_{EHQZ}	t_{HZ}	Chip Disable to Output Disable (Note 7)		15		15		15	ns
7†	t_{ELICCH}	t_{PU}	Chip Enable to Power Up (Note 3)	0		0		0		ns
8†	t_{EHICCL}	t_{PD}	Chip Disable to Power Down (Note 3)	0	25	0	35	0	45	ns
WRITE CYCLES ONE AND TWO (Note 8)										
9	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
10	t_{WLWH}	t_{WP}	Write Pulse Width (Note 5)	20		25		25		ns
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write (Note 5)	25		35		40		ns
12	t_{DVWH}	t_{DW}	Data Setup to End of Write	20		25		25		ns
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
14	t_{AVWH}	t_{AW}	Address Setup to End of Write (Note 5)	20		30		40		ns
15	t_{AVWL}	t_{AS}	Address Setup to Beginning of Write	0		0		0		ns
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
17†	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable (Notes 6 & 7)	0	10	0	15	0	20	ns
18†	t_{WHQX}	t_{OW}	Output Active After End of Write (Notes 6 & 7)	0		0		0		ns

SWITCHING CHARACTERISTICS (Cont'd.)

(Table 2 of 2)

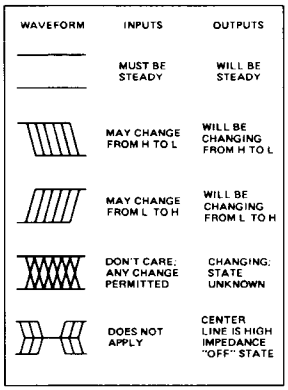
No.	Parameter Symbols		Parameter Description	Am99C641/Am99C641				Units
				-55		-70		
				Min.	Max.	Min.	Max.	
READ CYCLES ONE AND TWO (Note 8)								
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		55		70	ns
2	t_{AVAV}	t_{RC}	Read Cycle Time	55		70		ns
3	t_{AVQV}	t_{AA}	Address Access Time		55		70	ns
4	t_{AXQX}	t_{OH}	Output Hold After Address	5		5		ns
5†	t_{ELQX}	t_{LZ}	Chip Enable to Output Active (Note 7)	5		5		ns
6†	t_{EHQZ}	t_{HZ}	Chip Disable to Output Disable (Note 7)		20		20	ns
7†	t_{ELICCH}	t_{PU}	Chip Enable to Power Up (Note 3)	0		0		ns
8†	t_{EHICCL}	t_{PD}	Chip Disable to Power Down (Note 3)	0	55	0	70	ns
WRITE CYCLES ONE AND TWO (Note 8)								
9	t_{AVAV}	t_{WC}	Write Cycle Time	55		70		ns
10	t_{WLWH}	t_{WP}	Write Pulse Width (Note 5)	30		40		ns
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write (Note 5)	50		55		ns
12	t_{DVWH}	t_{DW}	Data Setup to End of Write	30		30		ns
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		ns
14	t_{AVWH}	t_{AW}	Address Setup to End of Write (Note 5)	50		55		ns
15	t_{AVWL}	t_{AS}	Address Setup to Beginning of Write	0		0		ns
16	t_{WHAX}	t_{WR}	Address Hold After End of Write		0		0	ns
17†	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable (Notes 6 & 7)	0	25	0	30	ns
18†	t_{WHQX}	t_{OW}	Output Active After End of Write (Notes 6 & 7)	0		0		ns

† Not included in Group A tests.

Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
3. Parameter not tested—guaranteed by characterization.
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input-pulse levels of 0 to 3.0 V, and output loading of specified I_{OL}/I_{OH} and 30-pF load capacitance. Output timing reference is 1.5 V (see Test Load A in Switching Test Circuits section).
5. The internal write time of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ LOW. Both signals must be active to initiate a write and either signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the transition edge that terminates the write.
6. The minimum limit is not tested and is included for design information only.
7. Parameter not tested, guaranteed by characterization using the load shown in Test Load B—Switching Test Circuits. Transition is measured ±500 mV from steady state voltage.
8. Address input rise and fall times must not exceed 1 μs when $\overline{CE}$ is active. The limit is not tested and is intended for design information only.
9. Undershoot to −3.0 V for a duration of 10 ns between the 50% amplitude point is permissible.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



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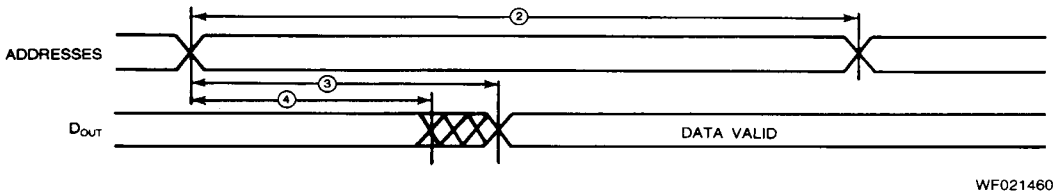

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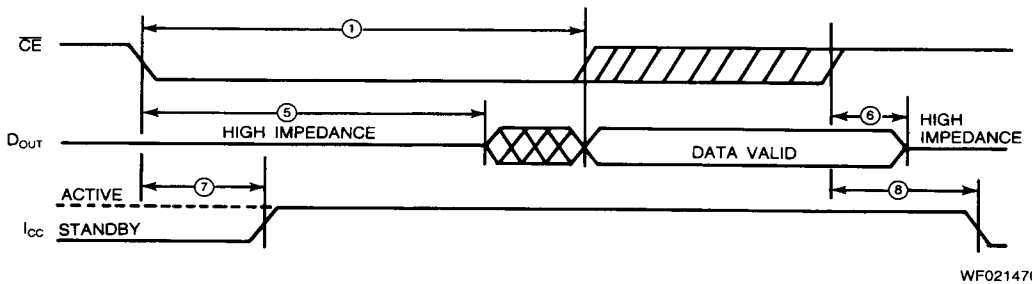
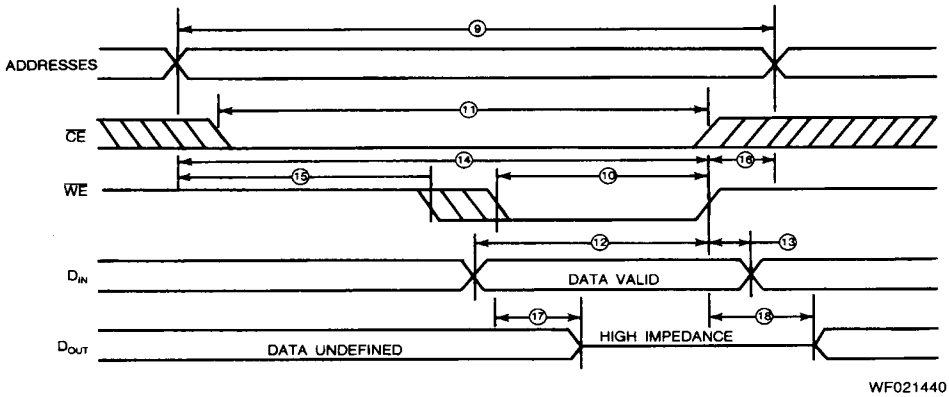
Read Cycle One



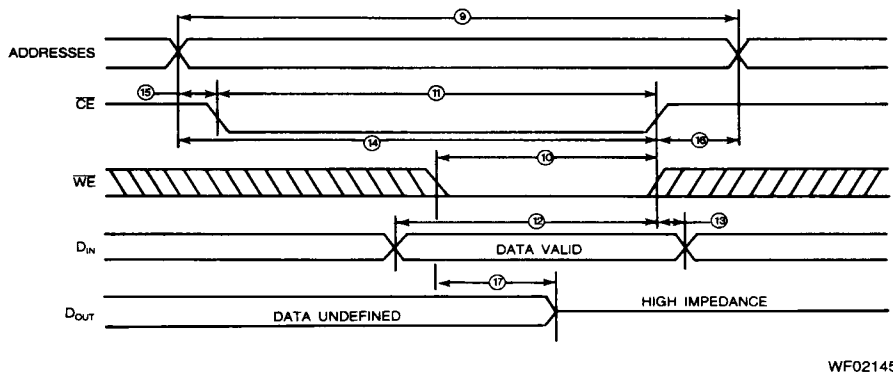
WF021470

Read Cycle Two

SWITCHING WAVEFORMS (Cont'd.)



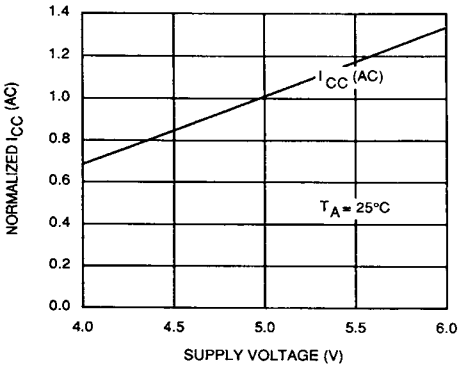
Write Cycle One



Write Cycle Two

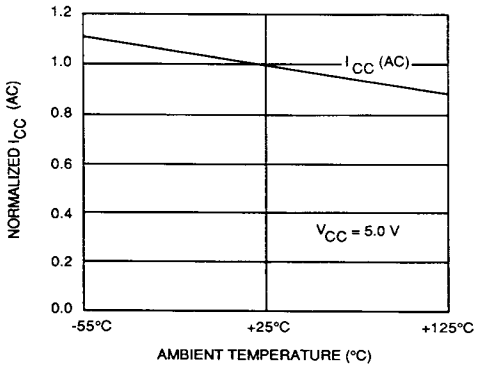
TYPICAL PERFORMANCE CURVES

NORMALIZED SUPPLY CURRENT
vs SUPPLY VOLTAGE



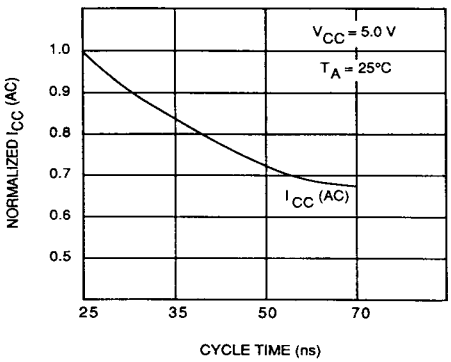
OP002540

NORMALIZED SUPPLY CURRENT
vs AMBIENT TEMPERATURE



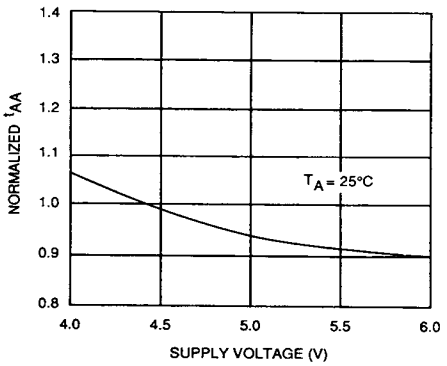
OP002550

NORMALIZED I_{CC} (AC)
vs CYCLE TIME



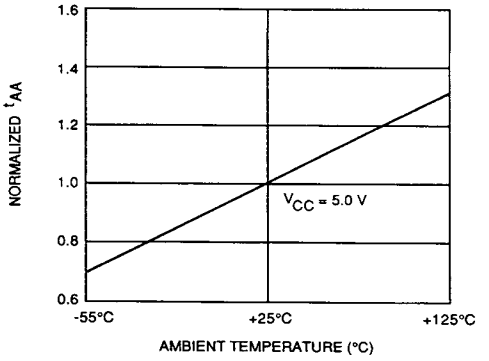
OP002560

NORMALIZED ACCESS TIME
vs SUPPLY VOLTAGE



OP002570

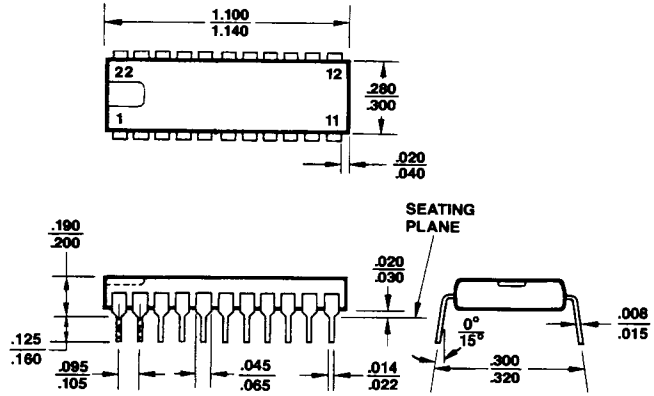
NORMALIZED ACCESS TIME
vs AMBIENT TEMPERATURE



OP002580

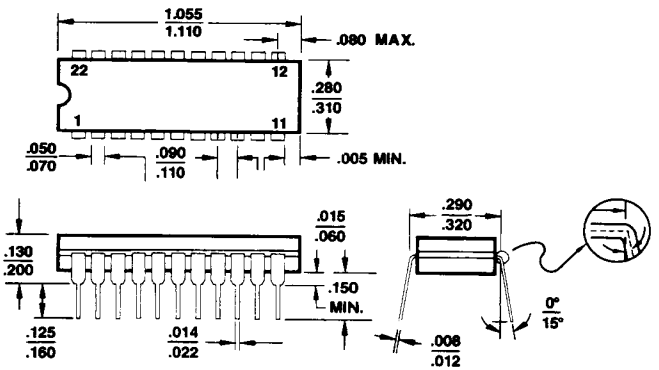
PHYSICAL DIMENSIONS*

PD3022



PID # 07813A

CD3022



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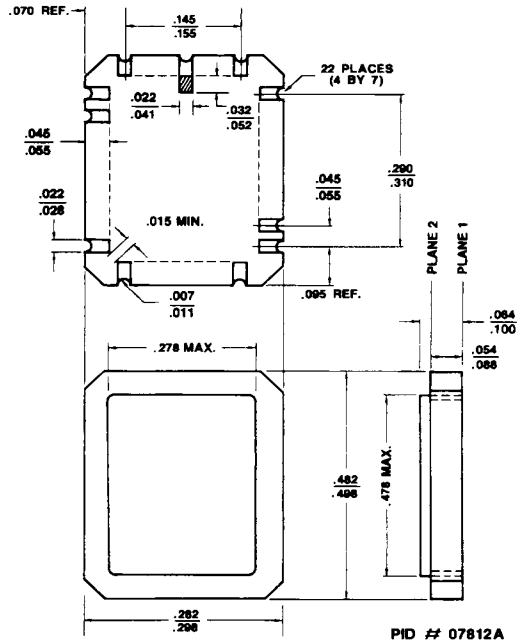
*For reference only.

PHYSICAL DIMENSIONS (Cont'd.)

CLR022*



*Preliminary. Subject to Change.

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