

Timing Generator for Frame Readout CCD Image Sensor

Description

The CXD2470R is a timing generator IC which generates the timing pulses for performing frame readout using the ICX224, ICX284, ICX202 and ICX232 CCD image sensor.

Features

- Base oscillation frequency 24.00 to 36.00MHz (max.)
- High-speed/low-speed shutter function
- Supports quadruple-speed readout drive
- Horizontal driver for CCD image sensor
- Vertical driver for CCD image sensor

Applications

Digital still cameras

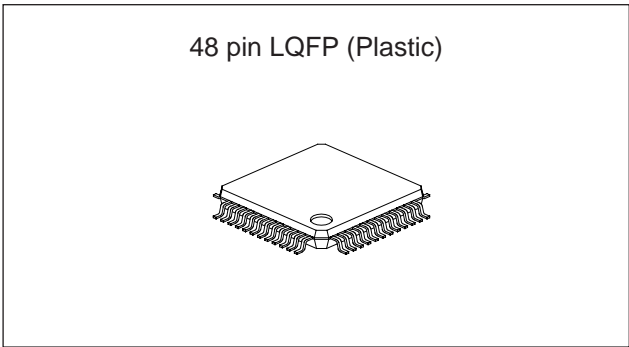
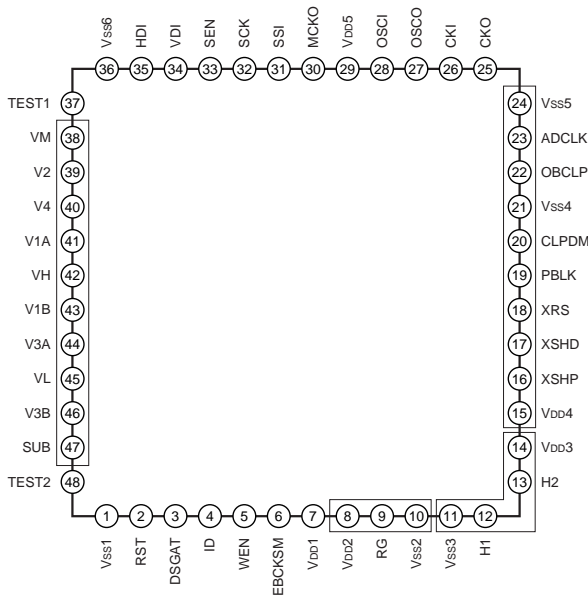
Structure

Silicon gate CMOS IC

Applicable CCD Image Sensors

- ICX224 (Type 1/2, 2020K pixels)
- ICX284 (Type 1/2.7, 2020K pixels)
- ICX202 (Type 1/3, 1250K pixels)
- ICX232 (Type 1/3.6, 1250K pixels)

Pin Configuration



Absolute Maximum Ratings

- Supply voltage

| | | |
|----------|--------------------------|---|
| V_{DD} | $V_{SS} - 0.3$ to $+7.0$ | V |
| V_L | -10.0 to V_{SS} | V |
| V_H | $V_L - 0.3$ to $+26.0$ | V |
- Input voltage

| | | |
|-------|----------------------------------|---|
| V_I | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
|-------|----------------------------------|---|
- Output voltage

| | | |
|----------|----------------------------------|---|
| V_{O1} | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
| V_{O2} | $V_L - 0.3$ to $V_{SS} + 0.3$ | V |
| V_{O3} | $V_L - 0.3$ to $V_H + 0.3$ | V |
- Operating temperature

| | | |
|-----------|----------------|----|
| T_{opr} | -20 to $+75$ | °C |
|-----------|----------------|----|
- Storage temperature

| | | |
|-----------|-----------------|----|
| T_{stg} | -55 to $+150$ | °C |
|-----------|-----------------|----|

Recommended Operating Conditions

- Supply voltage

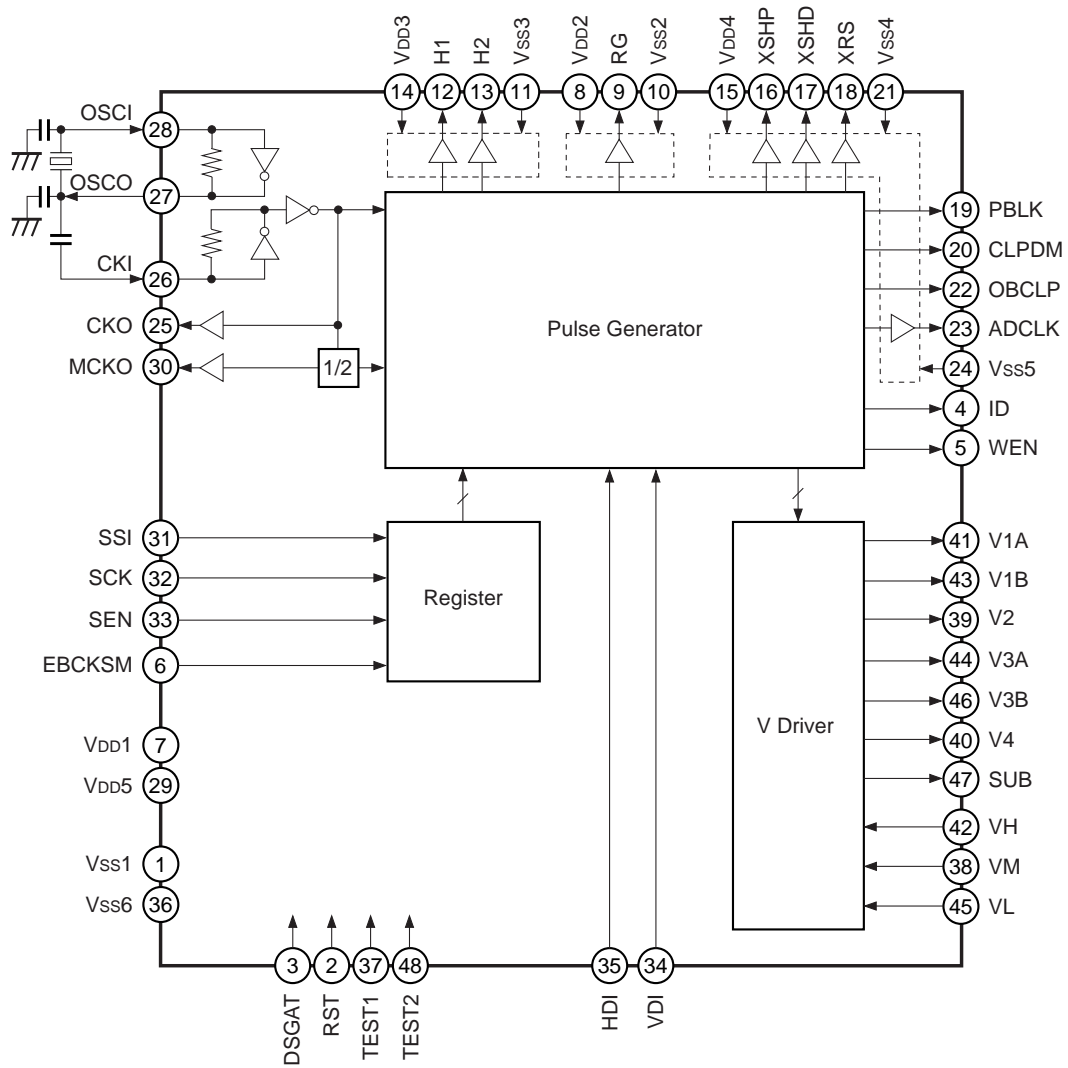
| | | |
|-----------------------------|------------------|---|
| V_{DDb} | 3.0 to 5.5 | V |
| $V_{DDA}, V_{DDC}, V_{DDd}$ | 3.0 to 3.6 | V |
| V_M | 0.0 | V |
| V_H | 14.5 to 15.5 | V |
| V_L | -7.0 to -8.0 | V |
- Operating temperature

| | | |
|-----------|----------------|----|
| T_{opr} | -20 to $+75$ | °C |
|-----------|----------------|----|

* Groups of pins enclosed in the figure indicate sections for which power supply separation is possible.

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Block Diagram



Pin Description

| Pin No. | Symbol | I/O | Description |
|---------|--------|-----|--|
| 1 | Vss1 | — | GND |
| 2 | RST | I | Internal system reset input. High: Normal operation, Low: Reset control Normally apply reset during power-on. Schmitt trigger input/No protective diode on power supply side |
| 3 | DSGAT | I | Control input used to stop pulse generation. High: Normal operation, Low: Stop control Schmitt trigger input/No protective diode on power supply side |
| 4 | ID | O | Vertical direction line identification pulse output. |
| 5 | WEN | O | Memory write timing pulse output. |
| 6 | EBCKSM | I | CHKSUM enable. High: Sum check invalid, Low: Sum check valid With pull-down resistor |
| 7 | VDD1 | — | 3.3V power supply. (Power supply for common logic block) |
| 8 | VDD2 | — | 3.3V power supply. (Power supply for RG) |
| 9 | RG | O | CCD reset gate pulse output. |
| 10 | Vss2 | — | GND |
| 11 | Vss3 | — | GND |
| 12 | H1 | O | CCD horizontal register clock output. |
| 13 | H2 | O | CCD horizontal register clock output. |
| 14 | VDD3 | — | 3.3 to 5.0V power supply. (Power supply for H1/H2) |
| 15 | VDD4 | — | 3.3V power supply. (Power supply for CDS block) |
| 16 | XSHP | O | CCD precharge level sample-and-hold pulse output. |
| 17 | XSHD | O | CCD data level sample-and-hold pulse output. |
| 18 | XRS | O | Sample-and-hold pulse output for analog/digital conversion phase alignment. |
| 19 | PBLK | O | Pulse output for horizontal and vertical blanking period pulse cleaning. |
| 20 | CLPDM | O | CCD dummy signal clamp pulse output. |
| 21 | Vss4 | — | GND |
| 22 | OBCLP | O | CCD optical black signal clamp pulse output. |
| 23 | ADCLK | O | Clock output for analog/digital conversion IC. Logical phase adjustment possible using the serial interface data. |
| 24 | Vss5 | — | GND |
| 25 | CKO | O | Inverter output. |
| 26 | CKI | I | Inverter input. |
| 27 | OSCO | O | Inverter output for oscillation. When not used, leave open or connect a capacitor. |
| 28 | OSCI | I | Inverter input for oscillation. When not used, fix low. |
| 29 | VDD5 | — | 3.3V power supply. (Power supply for common logic block) |
| 30 | MCKO | O | System clock output for signal processing IC. |

| Pin No. | Symbol | I/O | Description |
|---------|--------|-----|---|
| 31 | SSI | I | Serial interface data input for internal mode settings. Schmitt trigger input/No protective diode on power supply side |
| 32 | SCK | I | Serial interface clock input for internal mode settings. Schmitt trigger input/No protective diode on power supply side |
| 33 | SEN | I | Serial interface strobe input for internal mode settings. Schmitt trigger input/No protective diode on power supply side |
| 34 | VDI | I | Vertical sync signal input. Schmitt trigger input |
| 35 | HDI | I | Horizontal sync signal input. Schmitt trigger input |
| 36 | Vss6 | — | GND |
| 37 | TEST1 | I | IC test pin 1; normally fixed to GND. With pull-down resistor |
| 38 | VM | — | GND (GND for vertical driver) |
| 39 | V2 | O | CCD vertical register clock output. |
| 40 | V4 | O | CCD vertical register clock output. |
| 41 | V1A | O | CCD vertical register clock output. |
| 42 | VH | — | 15.0V power supply. (Power supply for vertical driver) |
| 43 | V1B | O | CCD vertical register clock output. |
| 44 | V3A | O | CCD vertical register clock output. |
| 45 | VL | — | -7.5V power supply. (Power supply for vertical driver) |
| 46 | V3B | O | CCD vertical register clock output. |
| 47 | SUB | O | CCD electronic shutter pulse output. |
| 48 | TEST2 | I | IC test pin 2; normally fixed to GND. With pull-down resistor |

Electrical Characteristics

DC Characteristics

(Within the recommended operating conditions)

| Item | Pins | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|-------------------|--|------------------|--|------------------------|------|---------------------|------|
| Supply voltage 1 | V _{DD2} | V _{DDa} | | 3.0 | 3.3 | 3.6 | V |
| Supply voltage 2 | V _{DD3} | V _{DDb} | | 3.0 | 3.3 | 5.5 | V |
| Supply voltage 3 | V _{DD4} | V _{DDc} | | 3.0 | 3.3 | 3.6 | V |
| Supply voltage 4 | V _{DD1} , V _{DD5} | V _{DDd} | | 3.0 | 3.3 | 3.6 | V |
| Input voltage 1*1 | RST, DSGAT, SSI, SCK, SEN, EBCKSM | V _{t+} | | 0.8V _{DDd} | | | V |
| | | V _{t-} | | | | 0.2V _{DDd} | V |
| Input voltage 2*2 | TEST1, TEST2 | V _{IH1} | | 0.7V _{DDd} | | | V |
| | | V _{IL1} | | | | 0.3V _{DDd} | V |
| Input voltage 3 | VDI, HDI | V _{IH2} | | 0.7V _{DDd} | | | V |
| | | V _{IL2} | | | | 0.3V _{DDd} | V |
| Output voltage 1 | H1, H2 | V _{OH1} | Feed current where I _{OH} = -22.0mA | V _{DDb} - 0.8 | | | V |
| | | V _{OL1} | Pull-in current where I _{OL} = 14.4mA | | | 0.4 | V |
| Output voltage 2 | RG | V _{OH2} | Feed current where I _{OH} = -3.3mA | V _{DDb} - 0.8 | | | V |
| | | V _{OL2} | Pull-in current where I _{OL} = 2.4mA | | | 0.4 | V |
| Output voltage 3 | XSHP, XSHD, XRS, PBLK, OBCLP, CLPDM, ADCLK | V _{OH3} | Feed current where I _{OH} = -3.3mA | V _{DDc} - 0.8 | | | V |
| | | V _{OL3} | Pull-in current where I _{OL} = 2.4mA | | | 0.4 | V |
| Output voltage 4 | CKO, MCKO | V _{OH4} | Feed current where I _{OH} = -10.4mA | V _{DDd} - 0.8 | | | V |
| | | V _{OL4} | Pull-in current where I _{OL} = 7.2mA | | | 0.4 | V |
| Output current 1 | V1A, V1B, V3A, V3B, V2, V4 | I _{OL} | V1A/B, V2, V3A/B, V4 = -8.25V | 10.0 | | | mA |
| | | I _{OM1} | V1A/B, V2, V3A/B, V4 = -0.25V | | | -5.0 | mA |
| | | I _{OM2} | V1A/B, V3A/B = 0.25V | 5.0 | | | mA |
| | | I _{OH} | V1A/B, V3A/B = 14.75V | | | -7.2 | mA |
| Output current 2 | SUB | I _{OSL} | SUB = -8.25V | 5.4 | | | mA |
| | | I _{OSH} | SUB = 14.75V | | | -4.0 | mA |

*1 These input pins are Schmitt trigger inputs and do not have protective diodes on the internal power supply side.

*2 These input pins have internal pull-down resistors.

Note) The above table indicates the condition for 3.3V drive.

Inverter I/O Characteristics for Oscillation

(Within the recommended operating conditions)

| Item | Pins | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------|------------|-----------------|---|------------------------|---------------------|---------------------|------|
| Logical Vth | OSCI | LVth | | | V _{DDd} /2 | | V |
| Input voltage | OSCI | V _{IH} | | 0.7V _{DDd} | | | V |
| | | V _{IL} | | | | 0.3V _{DDd} | V |
| Output voltage | OSCO | V _{OH} | Feed current where I _{OH} = -3.6mA | V _{DDd} - 0.8 | | | V |
| | | V _{OL} | Pull-in current where I _{OL} = 2.4mA | | | 0.4 | V |
| Feedback resistor | OSCI, OSCO | RFB | V _{IN} = V _{DDd} or V _{SS} | 500k | 2M | 5M | Ω |
| Oscillation frequency | OSCI, OSCO | f | | 20 | | 50 | MHz |

Inverter Input Characteristics for Base Oscillation Clock Duty Adjustment

(Within the recommended operating conditions)

| Item | Pins | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|-----------------|------|-----------------|----------------------|---------------------|---------------------|---------------------|------|
| Logical Vth | CKI | LVth | | | V _{DDd} /2 | | V |
| Input voltage | | V _{IH} | | 0.7V _{DDd} | | | V |
| | | V _{IL} | | | | 0.3V _{DDd} | V |
| Input amplitude | | V _{IN} | fmax 50MHz sine wave | 0.3 | | | Vp-p |

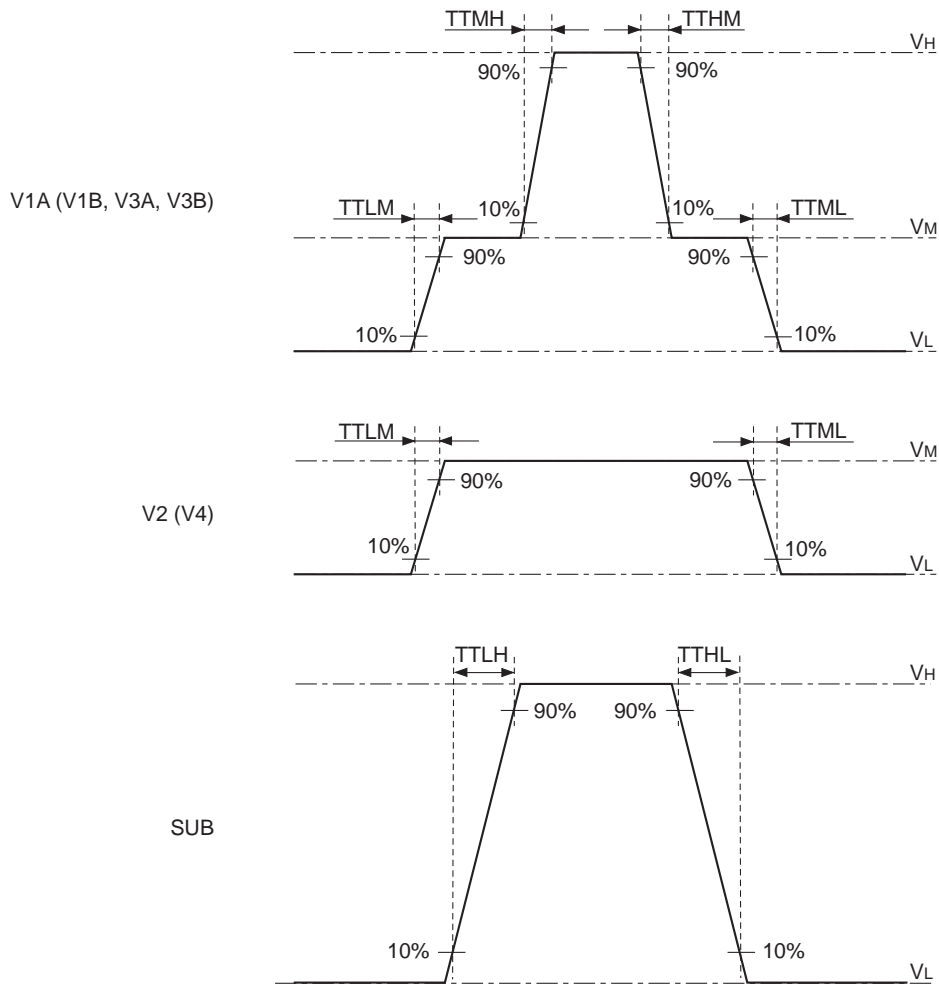
Note) Input voltage is the input voltage characteristics for direct input from an external source. Input amplitude is the input amplitude characteristics in the case of input through a capacitor.

Switching Characteristics(V_H = 15.0V, V_M = GND, V_L = -7.5V)

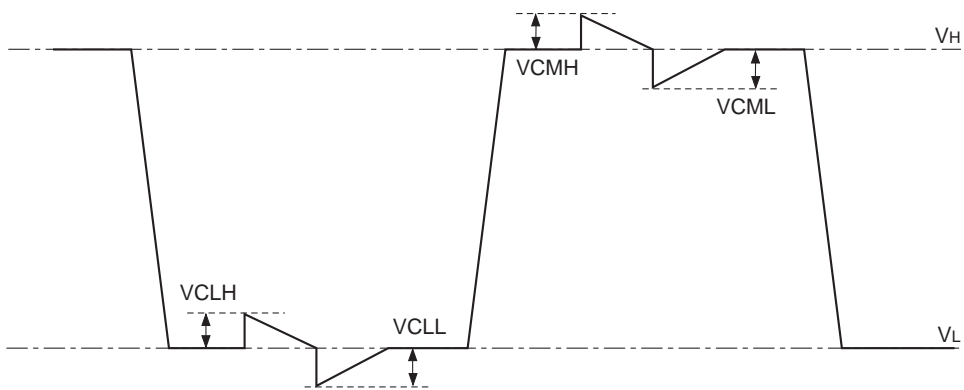
| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|----------------------|--------|----------------------------------|------|------|------|------|
| Rise time | TTLM | V _L to V _M | 200 | 350 | 500 | ns |
| | TTMH | V _M to V _H | 200 | 350 | 500 | ns |
| | TTLH | V _L to V _H | 30 | 60 | 90 | ns |
| Fall time | TTML | V _M to V _L | 200 | 350 | 500 | ns |
| | TTHM | V _H to V _M | 200 | 350 | 500 | ns |
| | TTHL | V _H to V _L | 30 | 60 | 90 | ns |
| Output noise voltage | VCLH | | | | 1.0 | V |
| | VCLL | | | | 1.0 | V |
| | VCMH | | | | 1.0 | V |
| | VCML | | | | 1.0 | V |

- Notes)**
1. The MOS structure of this IC has a low tolerance for static electricity, so full care should be given for measures to prevent electrostatic discharge.
 2. For noise and latch-up countermeasures, be sure to connect a by-pass capacitor (0.1μF or more) between each power supply pin (V_H, V_L) and GND.
 3. To protect the CCD image sensor, clamp the SUB pin output at V_H before input to the CCD image sensor.

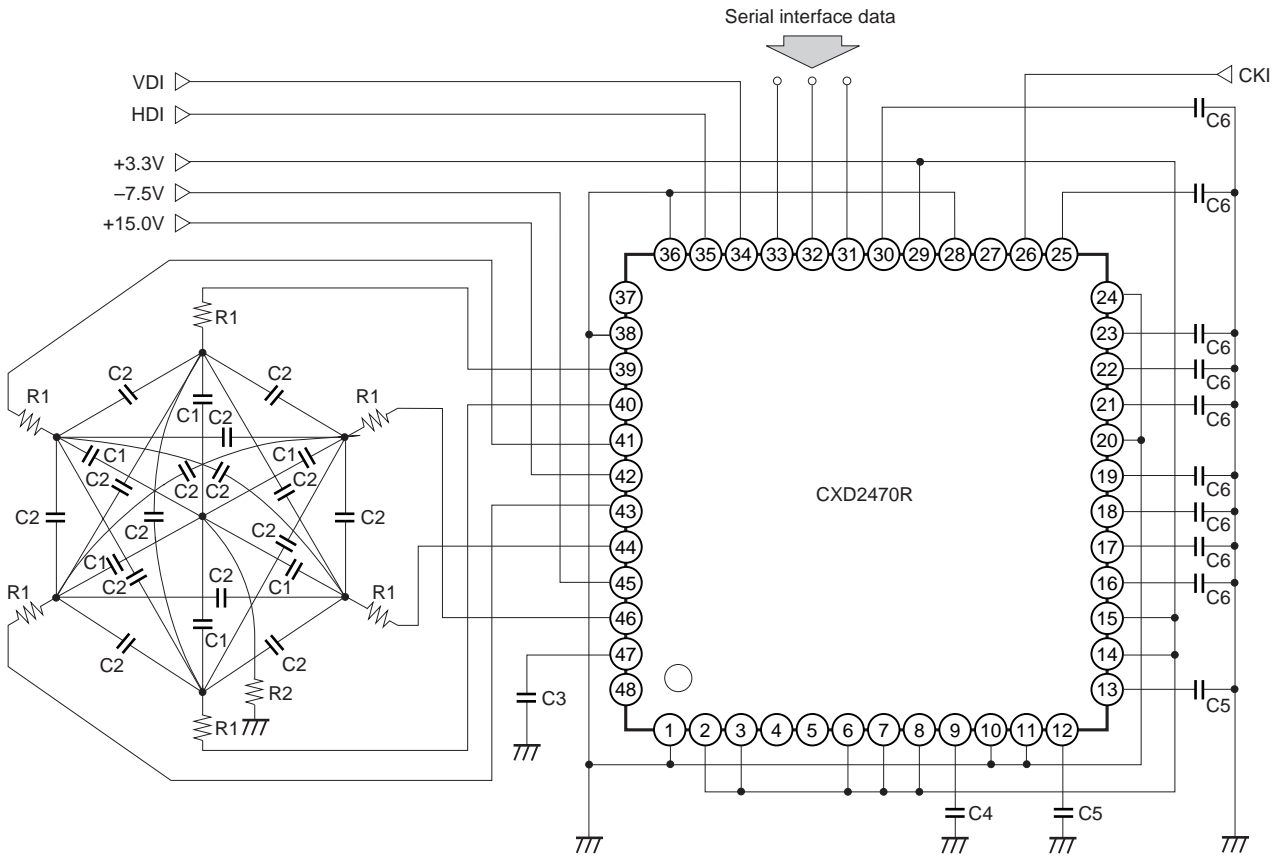
Switching Waveforms



Waveform Noise



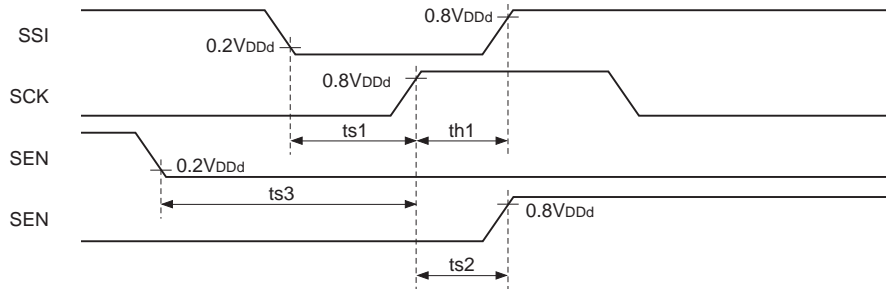
Measurement Circuit



| | | | | | | | | | | | |
|----|--------|----|-------|----|-------|----|------|----|-------|----|------|
| C1 | 3300pF | C2 | 560pF | C3 | 820pF | C4 | 30pF | C5 | 180pF | C6 | 10pF |
| R1 | 30Ω | R2 | 10Ω | | | | | | | | |

AC Characteristics

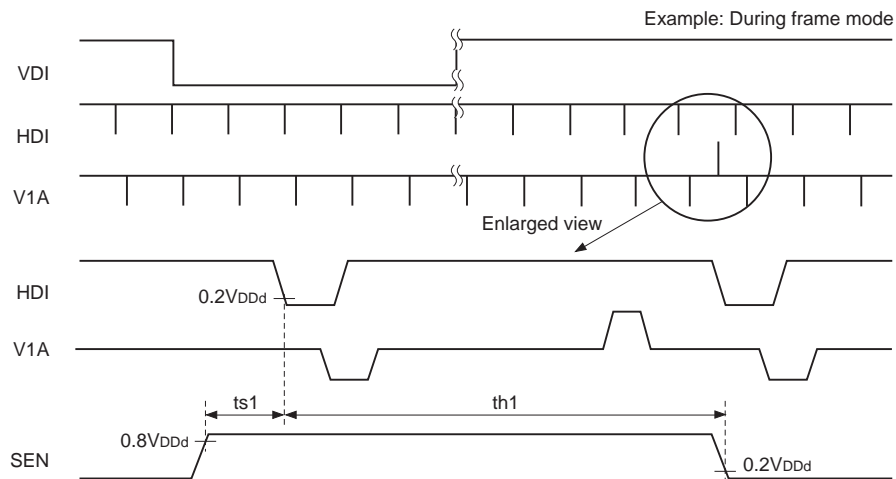
AC characteristics between the serial interface clocks



(Within the recommended operating conditions)

| Symbol | Definition | Min. | Typ. | Max. | Unit |
|--------|---|------|------|------|------|
| ts_1 | SSI setup time, activated by the rising edge of SCK | 20 | | | ns |
| th_1 | SSI hold time, activated by the rising edge of SCK | 20 | | | ns |
| ts_2 | SCK setup time, activated by the rising edge of SEN | 80 | | | ns |
| ts_3 | SEN setup time, activated by the rising edge of SCK | 20 | | | ns |

Serial interface clock internal loading characteristics (1)

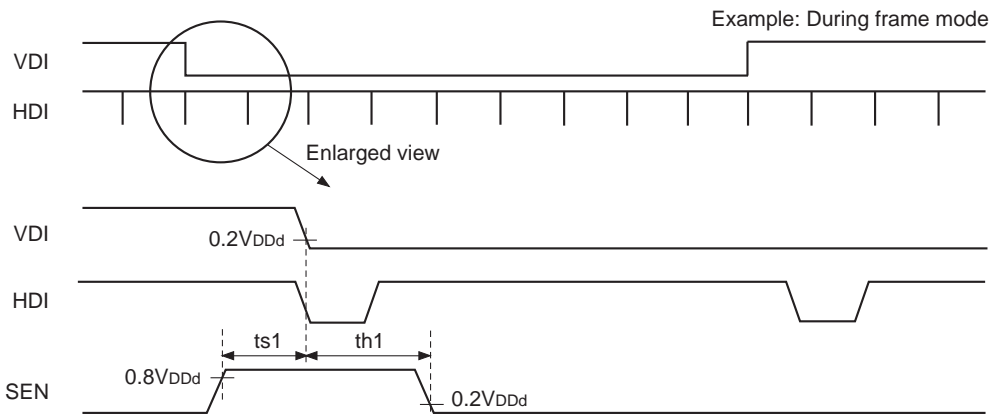


* Be sure to maintain a constantly high SEN logic level near the falling edge of the HDI in the horizontal period during which V1A/B and V3A/B values take the ternary value and during that horizontal period.

(Within the recommended operating conditions)

| Symbol | Definition | Min. | Typ. | Max. | Unit |
|--------|--|------|------|------|---------|
| ts_1 | SEN setup time, activated by the falling edge of HDI | 0 | | | ns |
| th_1 | SEN hold time, activated by the falling edge of HDI | 102 | | | μ s |

Serial interface clock internal loading characteristics (2)



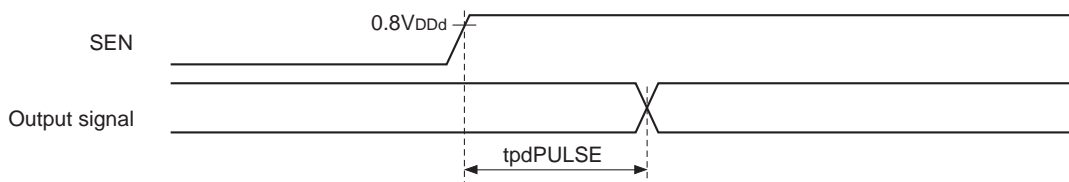
* Be sure to maintain a constantly high SEN logic level near the falling edge of VDI.

(Within the recommended operating conditions)

| Symbol | Definition | Min. | Typ. | Max. | Unit |
|--------|--|------|------|------|------|
| ts1 | SEN setup time, activated by the falling edge of VDI | 0 | | | ns |
| th1 | SEN hold time, activated by the falling edge of VDI | 200 | | | ns |

Serial interface clock output variation characteristics

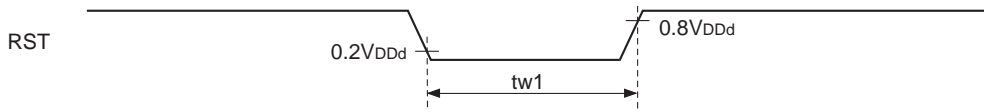
Normally, the serial interface data is loaded to the CXD2470R at the timing shown in "Serial interface clock internal loading characteristics (1)" above. However, one exception to this is when the data such as STB is loaded to the CXD2470R and controlled at the rising edge of SEN. See "Description of Operation".



(Within the recommended operating conditions)

| Symbol | Definition | Min. | Typ. | Max. | Unit |
|----------|--|------|------|------|------|
| tpdPULSE | Output signal delay, activated by the rising edge of SEN | 5 | | 100 | ns |

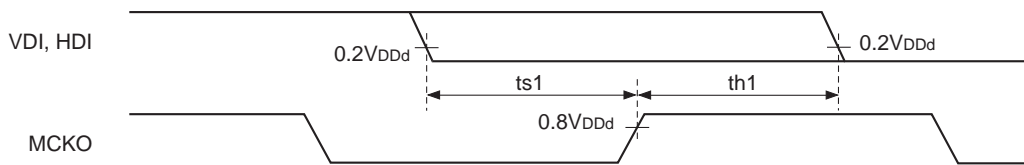
RST loading characteristics



(Within the recommended operating conditions)

| Symbol | Definition | Min. | Typ. | Max. | Unit |
|--------|-----------------|------|------|------|------|
| tw1 | RST pulse width | 35 | | | ns |

VDI and HDI loading characteristics

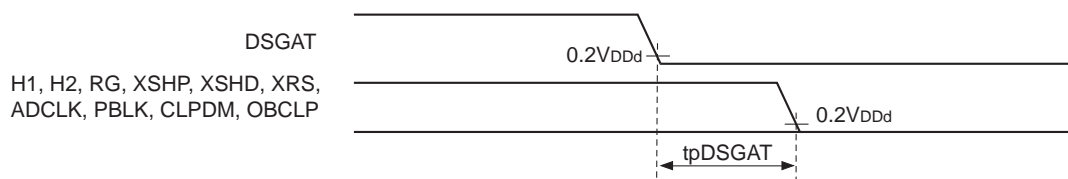


MCKO load capacitance = 10pF*1

(Within the recommended operating conditions)

| Symbol | Definition | Min. | Typ. | Max. | Unit |
|--------|--|------|------|------|------|
| ts1 | VDI and HDI setup time, activated by the rising edge of MCKO | 20 | | | ns |
| th1 | VDI and HDI hold time, activated by the rising edge of MCKO | 5 | | | ns |

Output timing characteristics using DSGAT

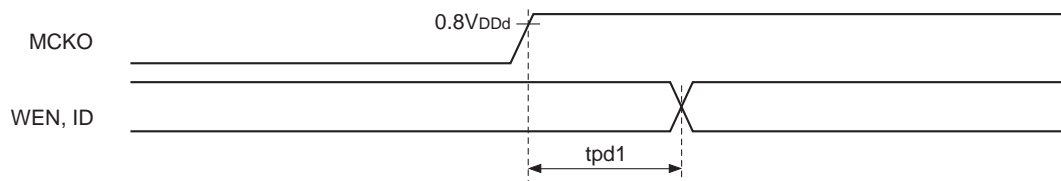


H1 and H2 load capacitance = 180pF, RG load capacitance = 30pF,
 XSHP, XSHD, XRS, PBLK, CLPDM, OBCLP and ADCLK load capacitance = 10pF

(Within the recommended operating conditions)

| Symbol | Definition | Min. | Typ. | Max. | Unit |
|---------|---|------|------|------|------|
| tpDSGAT | Time until the above outputs go low after the fall of DSGAT | | | 100 | ns |

Output variation characteristics



WEN and ID load capacitance = 10pF

(Within the recommended operating conditions)

| Symbol | Definition | Min. | Typ. | Max. | Unit |
|--------|--|------|------|------|------|
| tpd1 | Time until the above outputs change after the rise of MCKO | 20 | | 60 | ns |

Description of Operation

Pulses output from the CXD2470R are controlled mainly by the **RST** and **DSGAT** pins and by the serial interface data. The Pin Status Table is shown below, and the details of serial interface control are described on the following pages.

Pin Status Table

| Pin No. | Symbol | CAM | SLP | STB | DSGAT | RST | Pin No. | Symbol | CAM | SLP | STB | DSGAT | RST | |
|---------|--------|-----|-----|-----|-------|-----|---------|--------|-------|-----|-----|-------|-----|-----|
| 1 | Vss1 | — | | | | | | 25 | CKO | ACT | ACT | L | ACT | ACT |
| 2 | RST | ACT | ACT | ACT | ACT | L | 26 | CKI | ACT | ACT | ACT | ACT | ACT | |
| 3 | DSGAT | ACT | ACT | ACT | L | ACT | 27 | OSCO | ACT | ACT | ACT | ACT | ACT | |
| 4 | ID | ACT | L | L | ACT | L | 28 | OSCI | ACT | ACT | ACT | ACT | ACT | |
| 5 | WEN | ACT | L | L | ACT | L | 29 | VDD5 | — | | | | | |
| 6 | EBCKSM | ACT | ACT | ACT | ACT | ACT | 30 | MCKO | ACT | ACT | L | ACT | ACT | |
| 7 | VDD1 | — | | | | | | 31 | SSI | ACT | ACT | ACT | ACT | DIS |
| 8 | VDD2 | — | | | | | | 32 | SCK | ACT | ACT | ACT | ACT | DIS |
| 9 | RG | ACT | L | L | L | ACT | 33 | SEN | ACT | ACT | ACT | ACT | DIS | |
| 10 | Vss2 | — | | | | | | 34 | VDI | ACT | ACT | ACT | ACT | ACT |
| 11 | Vss3 | — | | | | | | 35 | HDI | ACT | ACT | ACT | ACT | ACT |
| 12 | H1 | ACT | L | L | L | ACT | 36 | Vss6 | — | | | | | |
| 13 | H2 | ACT | L | L | L | ACT | 37 | TEST1 | — | | | | | |
| 14 | VDD3 | — | | | | | | 38 | VM | — | | | | |
| 15 | VDD4 | — | | | | | | 39 | V2 | ACT | VM | VM | VM | VM |
| 16 | XSHP | ACT | L | L | L | ACT | 40 | V4 | ACT | VM | VM | VM | VL | |
| 17 | XSHD | ACT | L | L | L | ACT | 41 | V1A | ACT | VH | VH | VH | VM | |
| 18 | XRS | ACT | L | L | L | ACT | 42 | VH | — | | | | | |
| 19 | PBLK | ACT | L | L | L | H | 43 | V1B | ACT | VH | VH | VH | VM | |
| 20 | CLPDM | ACT | L | L | L | H | 44 | V3A | ACT | VH | VH | VH | VL | |
| 21 | Vss4 | — | | | | | | 45 | VL | — | | | | |
| 22 | OBCLP | ACT | L | L | L | H | 46 | V3B | ACT | VH | VH | VH | VL | |
| 23 | ADCLK | ACT | L | L | L | ACT | 47 | SUB | ACT | VH | VH | VH | VL | |
| 24 | Vss5 | — | | | | | | 48 | TEST2 | — | | | | |

Note) ACT means that the circuit is operating, and DIS means that loading is stopped.

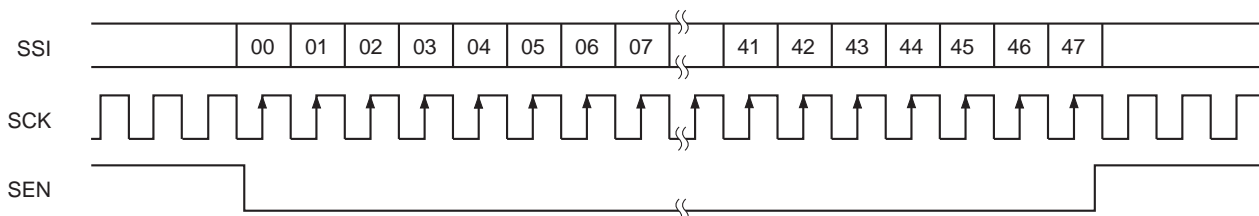
L indicates a low output level, and H a high output level in the controlled status.

Also, VH, VM and VL indicate the voltage levels applied to VH (Pin 42), VM (Pin 38) and VL (Pin 45), respectively, in the controlled status.

Serial Interface Control

The CXD2470R basically loads and reflects the serial interface data sent in the following format in the readout portion at the falling edge of HDI. Here, readout portion specifies the horizontal period during which V1A/B and V3A/B, etc. take the ternary value.

Note that some items reflect the serial interface data at the falling edge of VDI or the rising edge of SEN.



There are two categories of serial interface data: CXD2470R drive control data (hereafter "control data") and electronic shutter data (hereafter "shutter data").

The details of each data are described below.

Control Data

| Data | Symbol | Function | Data = 0 | Data = 1 | RST |
|------------------|--------|-----------------------------------|---|---------------|----------|
| D00 to D07 | CHIP | Chip enable | 10000001 → Enabled Other values → Disabled | | All 0 |
| D08 to D09 | CTG | Category switching | See [D08] to [D09] CTG. | | All 0 |
| D10 to D11 | MODE | Drive mode switching | See [D10] to [D11] MODE. | | All 0 |
| D12 | CCD | CCD switching | ICX224/ICX284 | ICX202/ICX232 | 0 |
| D13 to D14 | SMD | Electronic shutter mode switching | See [D13] to [D14] SMD. | | All 0 |
| D15 to D35 | — | — | — | — | All 0 |
| D36 to D37 | LDAD | ADCLK logic phase switching | See [D36] to [D37] LDAD. | | 1 |
| | | | | | 0 |
| D38 to D39 | STB | Standby control | See [D38] to [D39] STB. | | All 0 |
| D40 to D47 | CKSM | Check sum bit | See [D40] to [D47] CKSM. | | All 0 |

Shutter Data

| Data | Symbol | Function | Data = 0 | Data = 1 | RST |
|------------------|--------|---|--|----------|----------|
| D00 to D07 | CHIP | Chip enable | 10000001 → Enabled Other values → Disabled | | All 0 |
| D08 to D09 | CTG | Category switching | See D08 to D09 CTG. | | All 0 |
| D10 to D17 | SVD | Electronic shutter vertical period specification | See D10 to D17 SVD. | | All 0 |
| D18 to D27 | SHD | Electronic shutter horizontal period specification | See D18 to D27 SHD. | | All 0 |
| D28 to D35 | SPL | High-speed shutter position specification | See D28 to D35 SPL. | | All 0 |
| D36 to D39 | — | — | — | — | All 0 |
| D40 to D47 | CKSM | Check sum bit | See D40 to D47 CKSM. | | All 0 |

Detailed Description of Each Data

Shared data: D08 to D09 CTG [Category]

Of the data provided to the CXD2470R by the serial interface, the CXD2470R loads D10 and subsequent data to each data register as shown in the table below according to the combination of D08 and D09.

| D09 | D08 | Description of operation |
|-----|-----|----------------------------------|
| 0 | 0 | Loading to control data register |
| 0 | 1 | Loading to shutter data register |
| 1 | 0 | Test mode |
| 1 | 1 | |

Note that the CXD2470R can apply these categories consecutively within the same vertical period. However, care should be taken as the data is overwritten if the same category is applied.

Shared data: D40 to D47 CKSM [Check sum]

These are the check sum bits. Apply the data shown below. This function is valid when EBCKSM (Pin 6) is low.

| | | | | | | | | | | | | | | | | | |
|----|-----|-----|-----|-----|-----|-----|-----|-----|------------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | MSB | | | | | | | | LSB | | | | | | | | |
| | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 | | D15 | D14 | D13 | D12 | D11 | D10 | D09 | D08 |
| | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | | D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 |
| | D39 | D38 | D37 | D36 | D35 | D34 | D33 | D32 | | D47 | D46 | D45 | D44 | D43 | D42 | D41 | D40 |
| +) | D47 | D46 | D45 | D44 | D43 | D42 | D41 | D40 | → CKSM | | | | | | | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | → Reflected when the total is "0". | | | | | | | | |

Control data: D10 to D11 MODE [Drive mode]

The CXD2470R drive mode can be switched as follows. However, the drive mode bits are loaded to the CXD2470R and reflected at the falling edge of VDI.

| D11 | D10 | Description of operation |
|-----|-----|--------------------------------|
| 0 | 0 | Quadruple-speed mode (default) |
| 0 | 1 | Frame mode (A field readout) |
| 1 | 0 | Frame mode (B field readout) |
| 1 | 1 | Frame mode |

Control data: D12 CCD [CCD switching]

Specifies CCD image sensor to be used. However, the CCD image sensor switching bit is loaded to the CXD2470R and reflected at the falling edge of VDI. The default is "ICX224/ICX284".

| D12 | CCD |
|-----|---------------|
| 0 | ICX224/ICX284 |
| 1 | ICX202/ICX232 |

Control data: D36 to D37 LDAD [ADCLK logic phase adjustment]

This indicates the ADCLK logic phase adjustment data. The default is 90° relative to MCKO.

| D37 | D36 | Degree of adjustment (°) |
|-----|-----|--------------------------|
| 0 | 0 | 0 |
| 0 | 1 | 90 |
| 1 | 0 | 180 |
| 1 | 1 | 270 |

Control data: D38 to D39 STB [Standby]

The operating mode is switched as follows. However, the standby bits are loaded to the CXD2470R and control is applied immediately at the rising edge of SEN.

| D39 | D38 | Symbol | Operating mode |
|-----|-----|--------|-----------------------|
| X | 0 | CAM | Normal operating mode |
| 0 | 1 | SLP | Sleep mode |
| 1 | 1 | STB | Standby mode |

See the Pin Status Table for the pin status in each mode.

Control data/shutter data: [Electronic shutter]

The CXD2470R realizes various electronic shutter functions by using control data [D13] to [D14] SMD and shutter data [D10] to [D17] SVD, [D18] to [D27] SHD and [D28] to [D35] SPL.

These functions are described in detail below.

First, the various modes are shown below.

These modes are switched using control data [D13] to [D14] SMD.

| D14 | D13 | Description of operation |
|-----|-----|-----------------------------------|
| 0 | 0 | Electronic shutter stopped mode |
| 0 | 1 | High-speed/low-speed shutter mode |
| 1 | 0 | |
| 1 | 1 | HTSG control mode |

The electronic shutter data is expressed as shown in the table below using [D18] to [D27] SHD as an example.

| MSB | | | | | | LSB | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| | ↓ | | | ↓ | | | ↓ | | |
| | 1 | | | C | | | 3 | | |

→ SHD is expressed as [1C3h].

[Electronic shutter stopped mode]

During this mode, all shutter data items are invalid.

SUB is not output in this mode, so the shutter speed is the accumulation time for one field.

[High-speed/low-speed shutter mode]

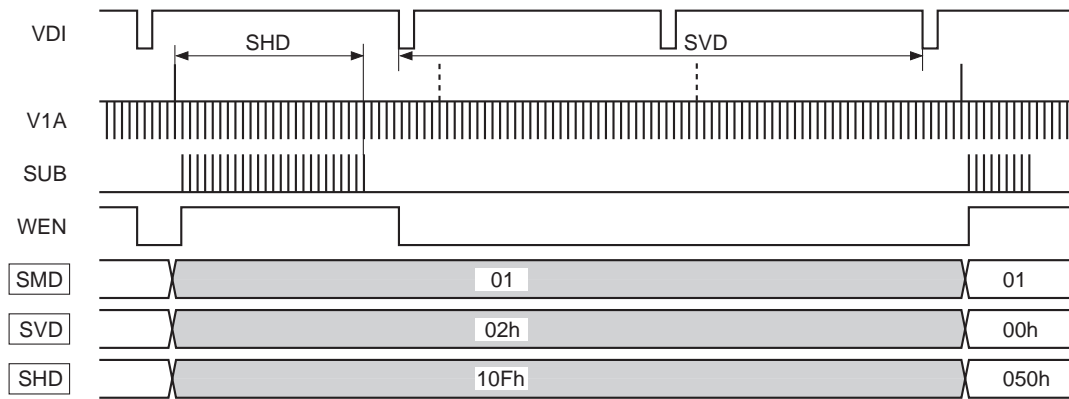
During this mode, the shutter data items have the following meanings.

| Symbol | Data | Description |
|--------|----------------|--|
| SVD | [D10] to [D17] | Number of vertical periods specification (00h ≤ SVD ≤ FFh) |
| SHD | [D18] to [D27] | Number of horizontal periods specification (000h ≤ SHD ≤ 3FFh) |
| SPL | [D28] to [D35] | Vertical period specification for high-speed shutter operation (00h ≤ SPL ≤ FFh) |

The period during which SVD and SHD are specified together is the shutter speed. Concretely, when specifying high-speed shutter, SVD is set to "00h". (See the figure.) During low-speed shutter, or in other words when SVD is set to "01h" or higher, the serial interface data is not loaded until this period is finished.

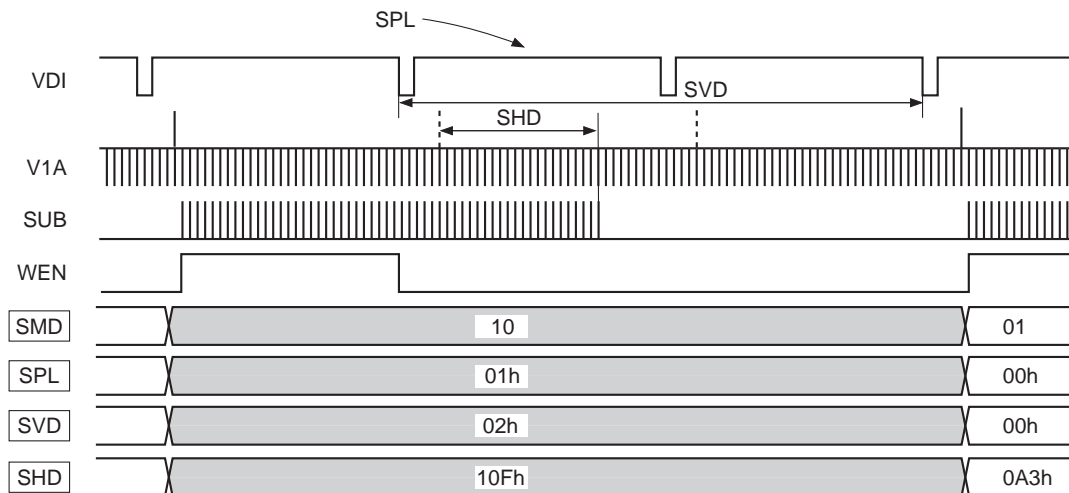
The vertical period indicated here corresponds to one field in each drive mode. In addition, the number of horizontal periods applied to SHD can be considered as (number of SUB pulses – 1).

Note) The bit data definition area is assured in terms of the CXD2470R functions, and does not assure the CCD characteristics.



Further, SPL can be used during this mode to specify the SUB output at the desired vertical period during the low-speed shutter period.

In the case below, SUB is output based on SHD at the SPL vertical period out of (SVD + 1) vertical periods.



Incidentally, SPL is counted as "00h", "01h", "02h" and so on in conformance with SVD.

Using this function it is possible to achieve smooth exposure time transitions when changing from low-speed shutter to high-speed shutter or vice-versa.

[HTSG control mode]

During this mode, all shutter data items are invalid.

The V1A/B and V3A/B ternary level outputs are stopped, so the shutter speed is the value obtained by adding the shutter speed specified in the preceding vertical period to the vertical period during which these readout pulses are stopped as shown in the figure.

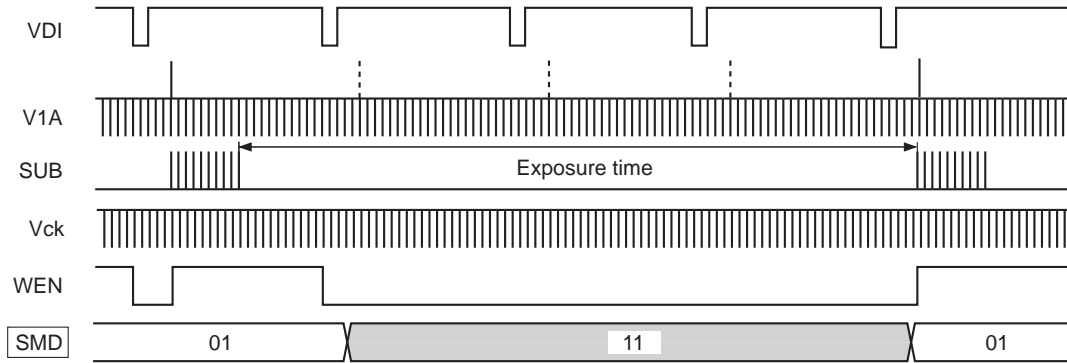
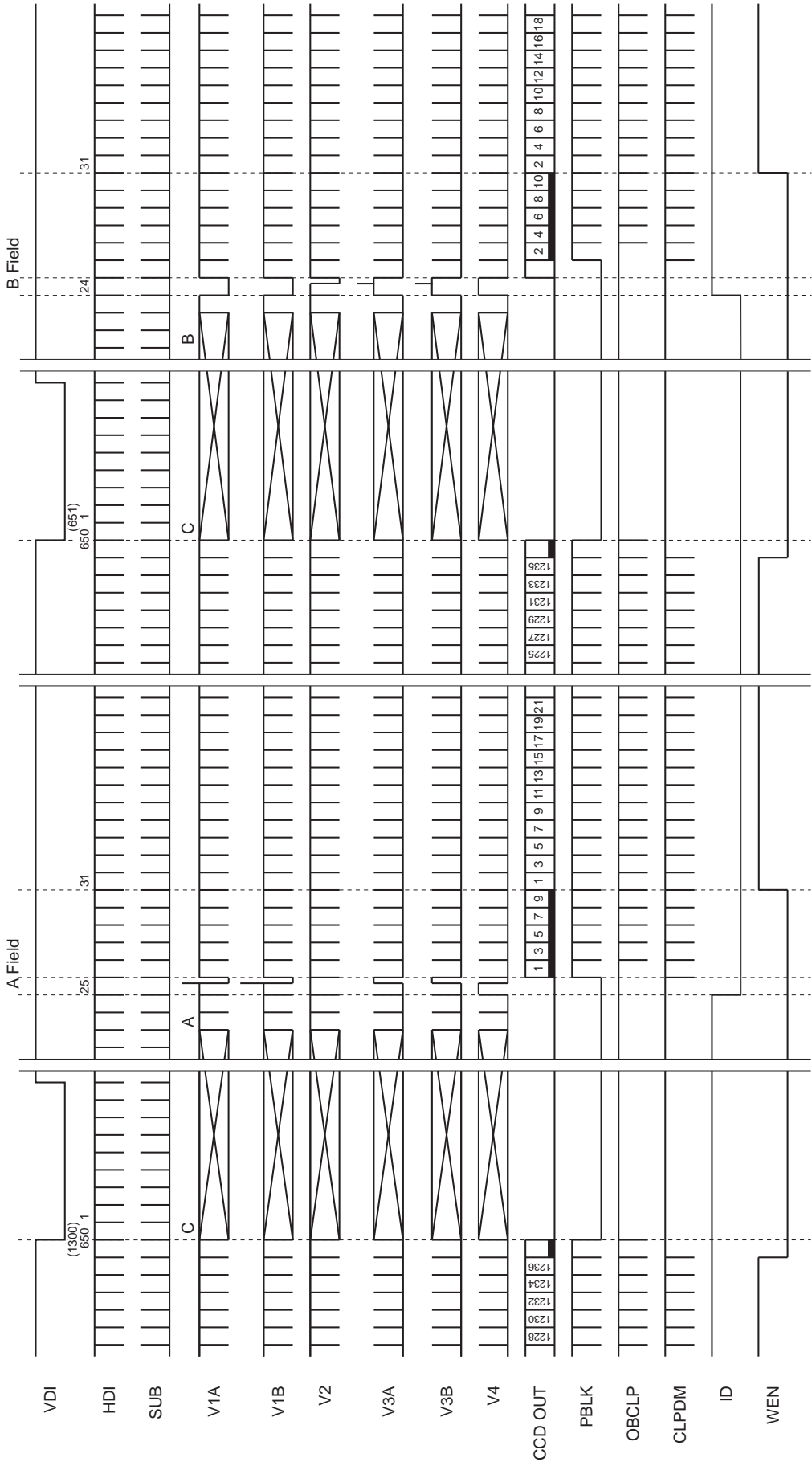


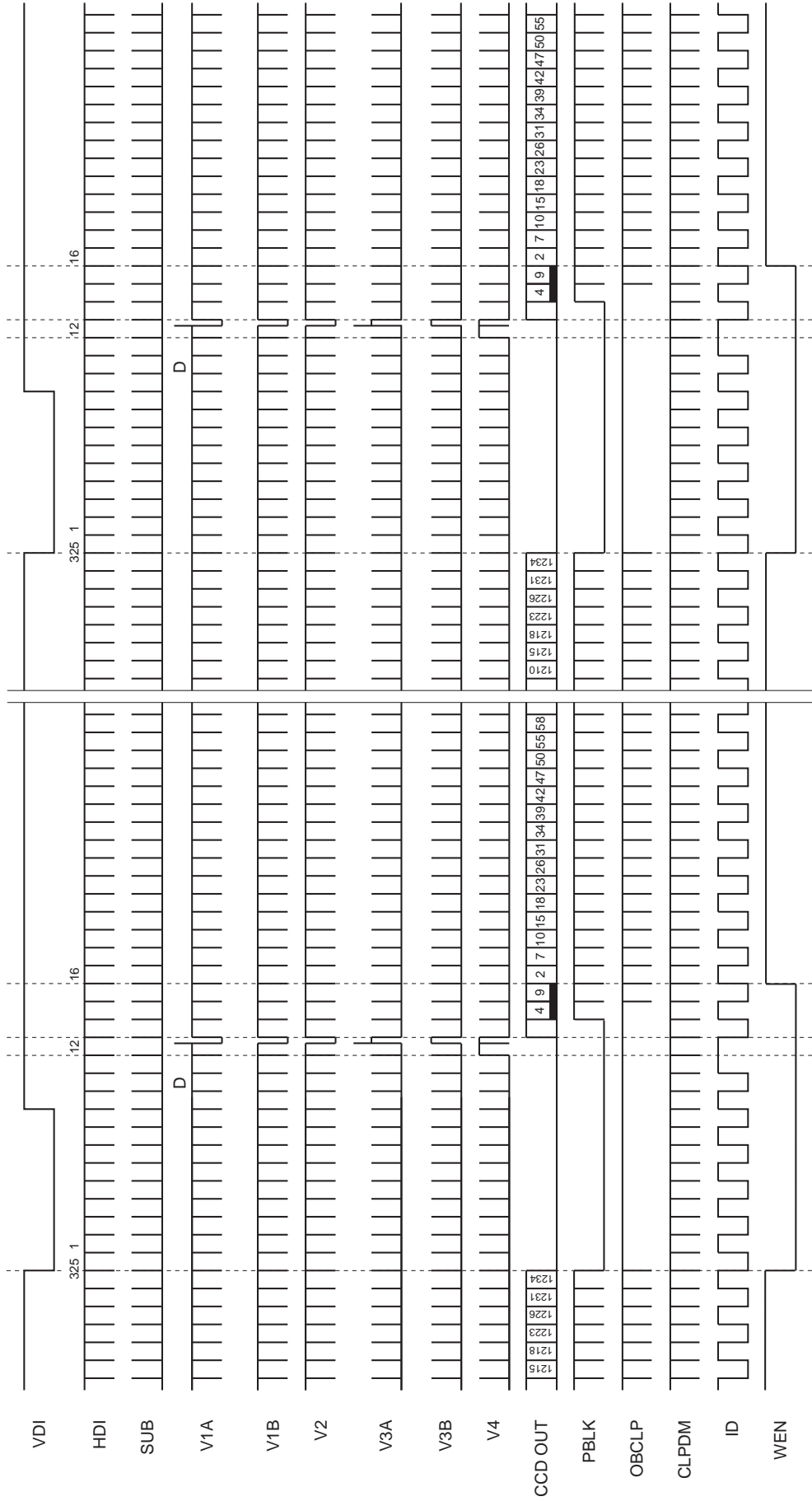
Chart-1 Vertical Direction Timing Chart
MODE
 Frame mode



* The number of SUB pulses is determined by the serial interface. This chart shows the case where SUB pulses are output in each horizontal period.
 * ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

Chart-2 Vertical Direction Timing Chart

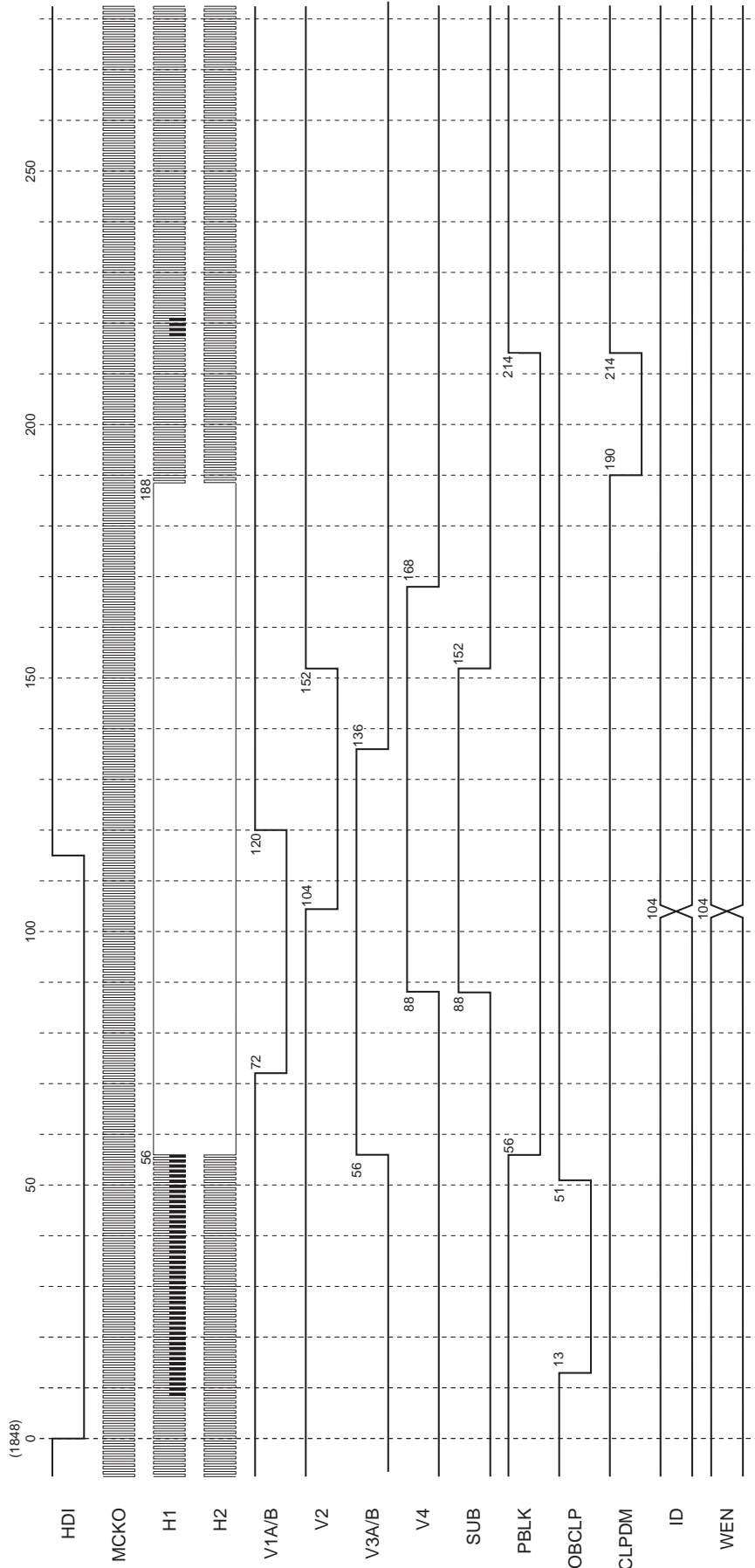
MODE
Quadruple-speed mode



* The number of SUB pulses is determined by the serial interface. This chart shows the case where SUB pulses are output in each horizontal period.
* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

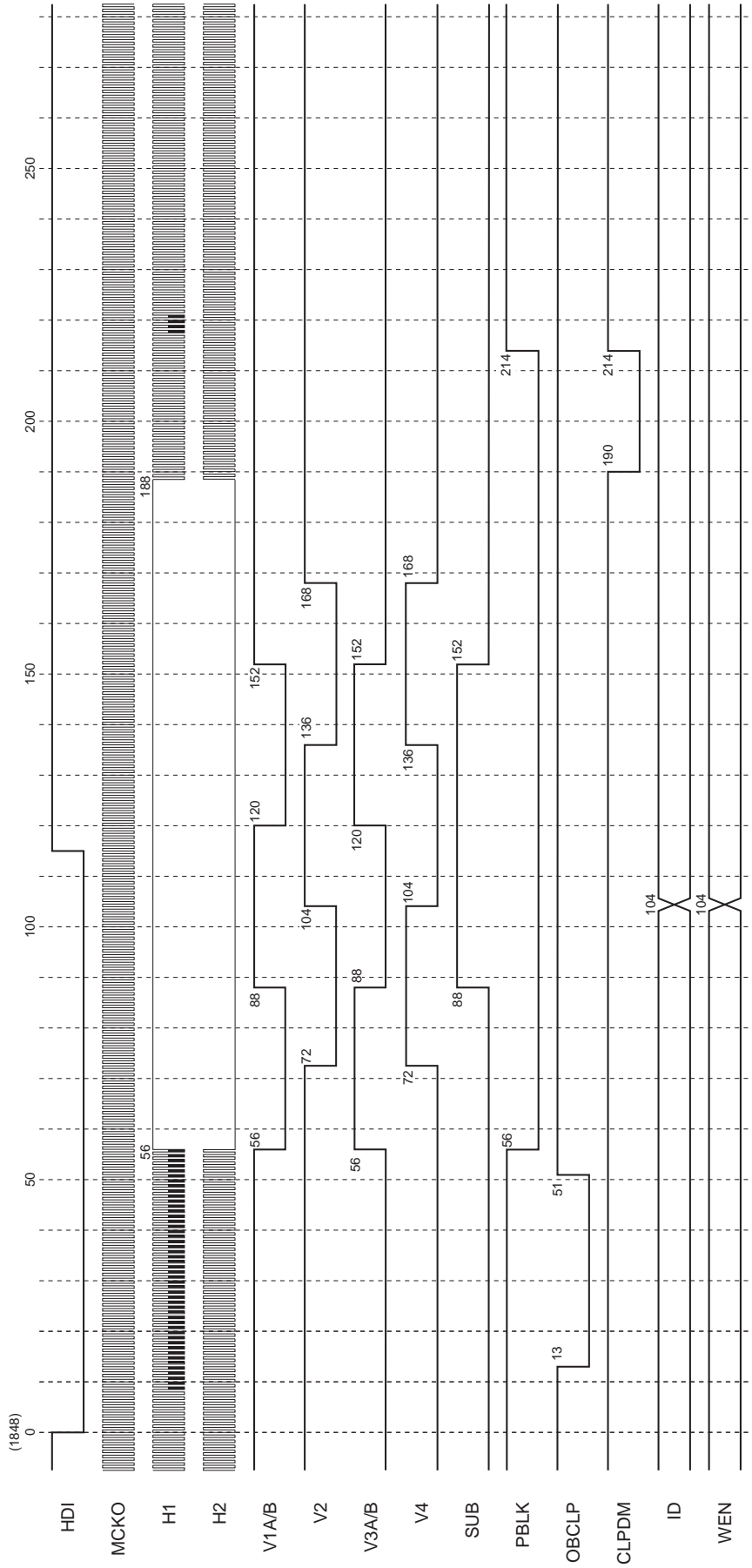
Chart-3 Horizontal Direction Timing Chart
 Applicable CCD image sensor
 • ICX224/ICX284

MODE
 Frame mode



- * The HDI of this chart indicates the actual CXD2470R load timing.
- * The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HDI.
- * The HDI fall period should be between approximately 3.1 to 10.4μs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4μs).
- * SUB is output at the timing shown above when output is controlled by the serial interface data.
- * ID and WEN are output at the timing shown above at the position shown in Chart-1.

Chart-4 Horizontal Direction Timing Chart **MODE** **Quadruple-speed mode** **Applicable CCD image sensor**
 • ICX224/ICX284

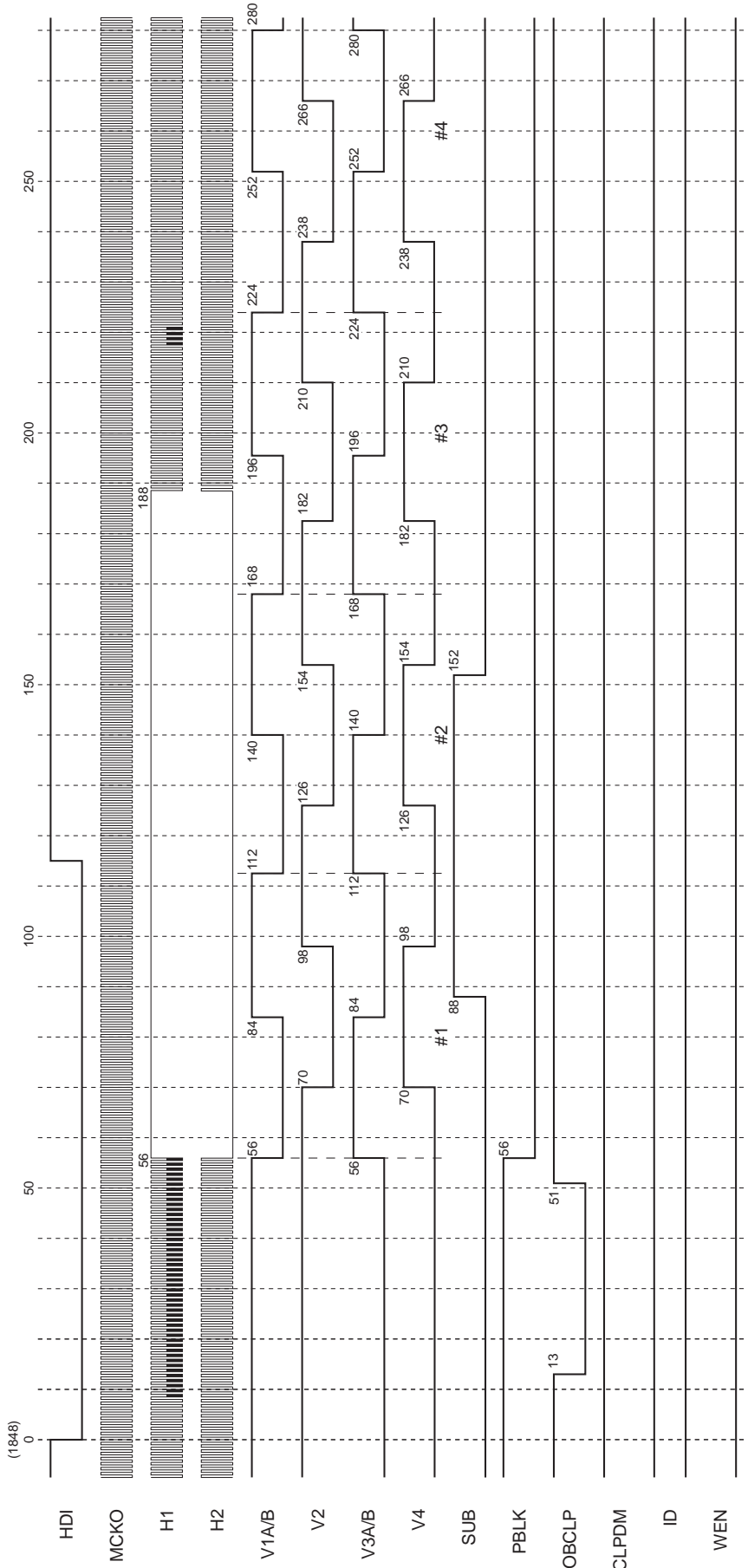


* The HDI of this chart indicates the actual CXD2470R load timing.
 * The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HDI.
 * The HDI fall period should be between approximately 3.1 to 10.4μs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4μs).
 * SUB is output at the timing shown above when output is controlled by the serial interface data.
 * ID and WEN are output at the timing shown above at the position shown in Chart-2.

Chart-5 Horizontal Direction Timing Chart
(High-speed sweep: C)

MODE
Frame mode

Applicable CCD image sensor
• ICX224/ICX284



- * The HDI of this chart indicates the actual CXD2470R load timing.
- * The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HDI.
- * The HDI fall period should be between approximately 3.1 to 10.4µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs).
- * SUB is output at the timing shown above when output is controlled by the serial interface data.
- * High-speed sweep of V1A/B, V2, V3A/B and V4 is performed up to 22H of 1848ck (#758).

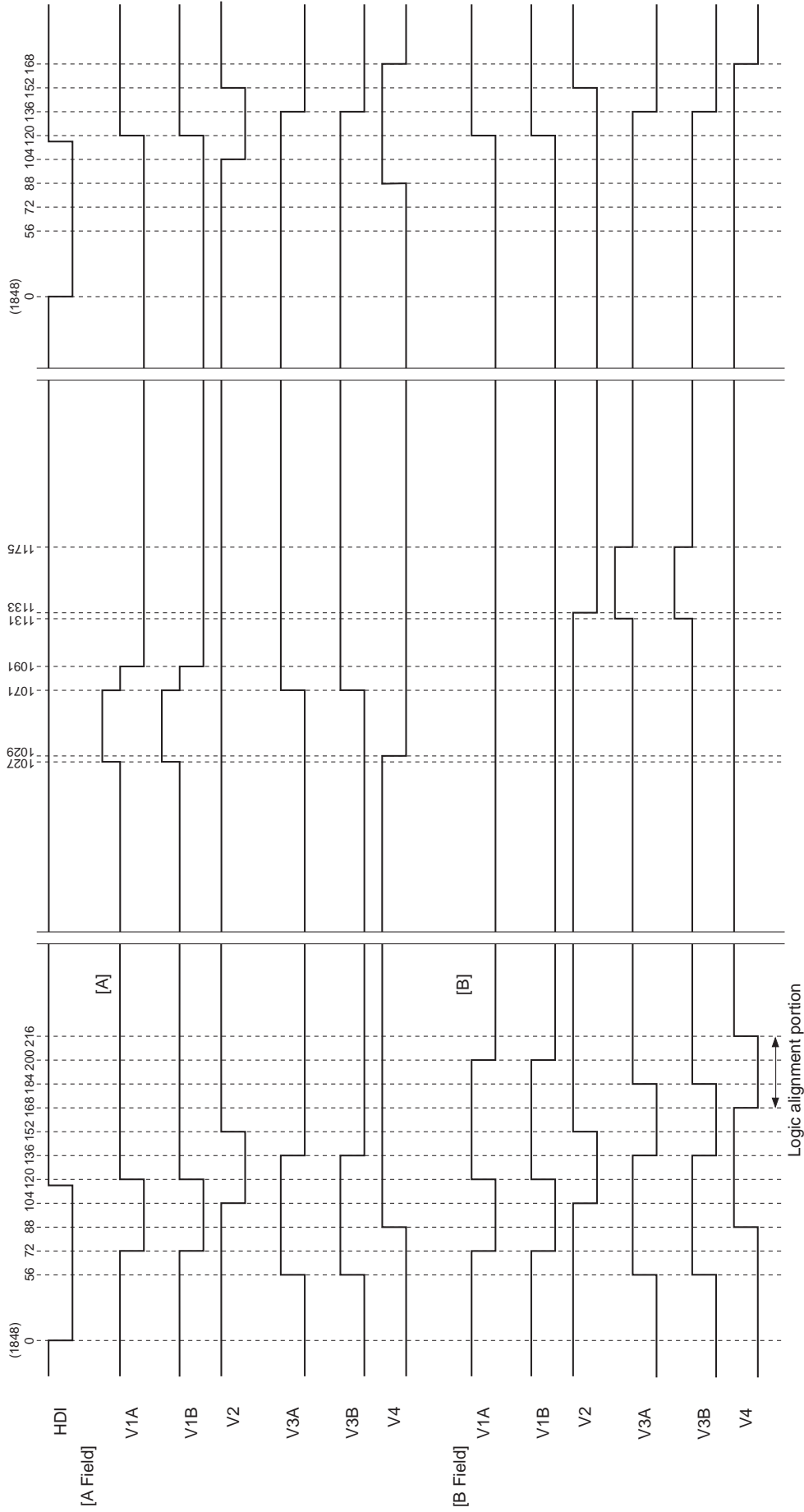
Chart-6 Horizontal Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

- ICX224/ICX284



* The HDI of this chart indicates the actual CXD2470R load timing.

* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HDI.

* The HDI fall period should be between approximately 3.0 to 13.4μs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4μs).

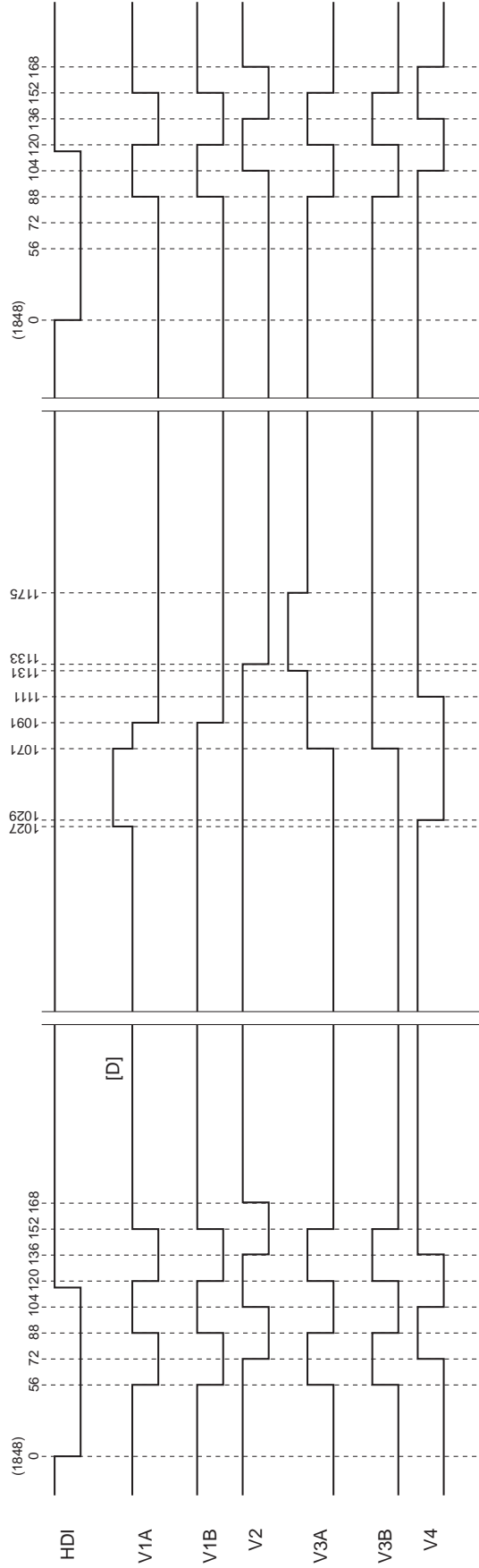
Chart-7 Horizontal Direction Timing Chart

MODE

Quadruple-speed mode

Applicable CCD image sensor

- ICX224/ICX284

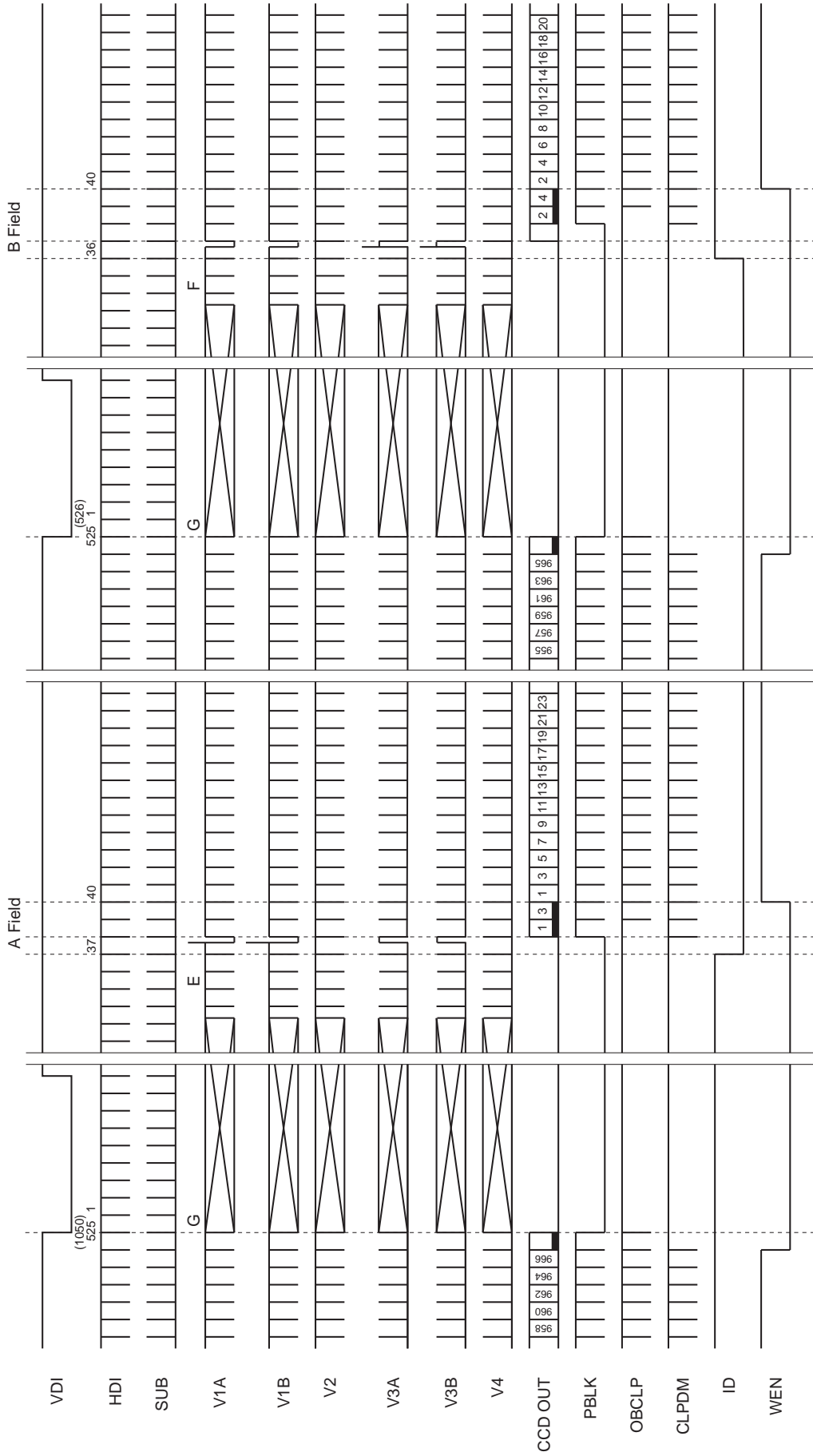


* The HDI of this chart indicates the actual CXD2470R load timing.
 * The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HDI.
 * The HDI fall period should be between approximately 3.1 to 10.4μs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4μs).

Applicable CCD image sensor
• ICX202/ICX232

MODE
Frame mode

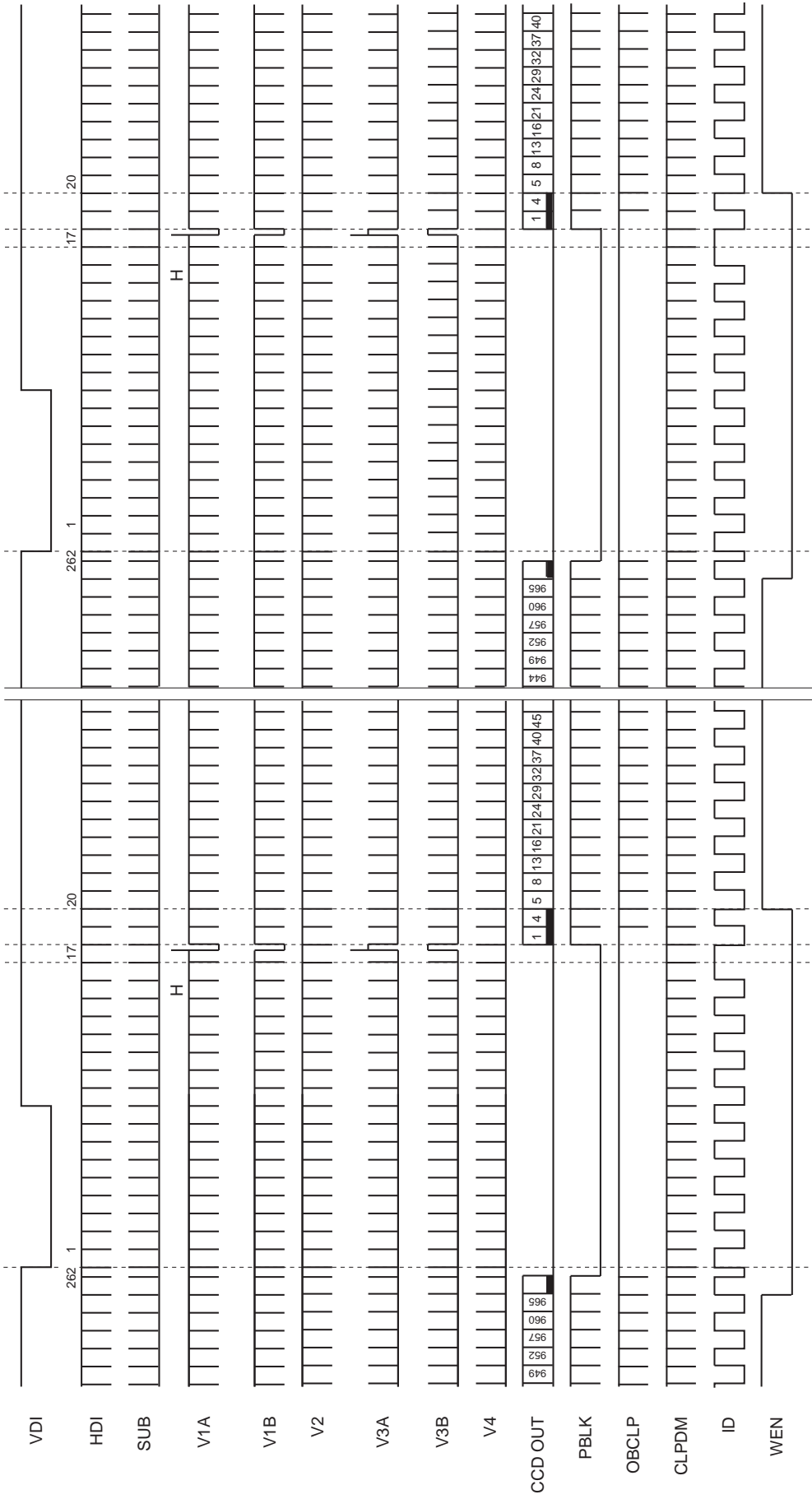
Chart-8 Vertical Direction Timing Chart



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

Chart-9 Vertical Direction Timing Chart

MODE
Quadruple-speed mode

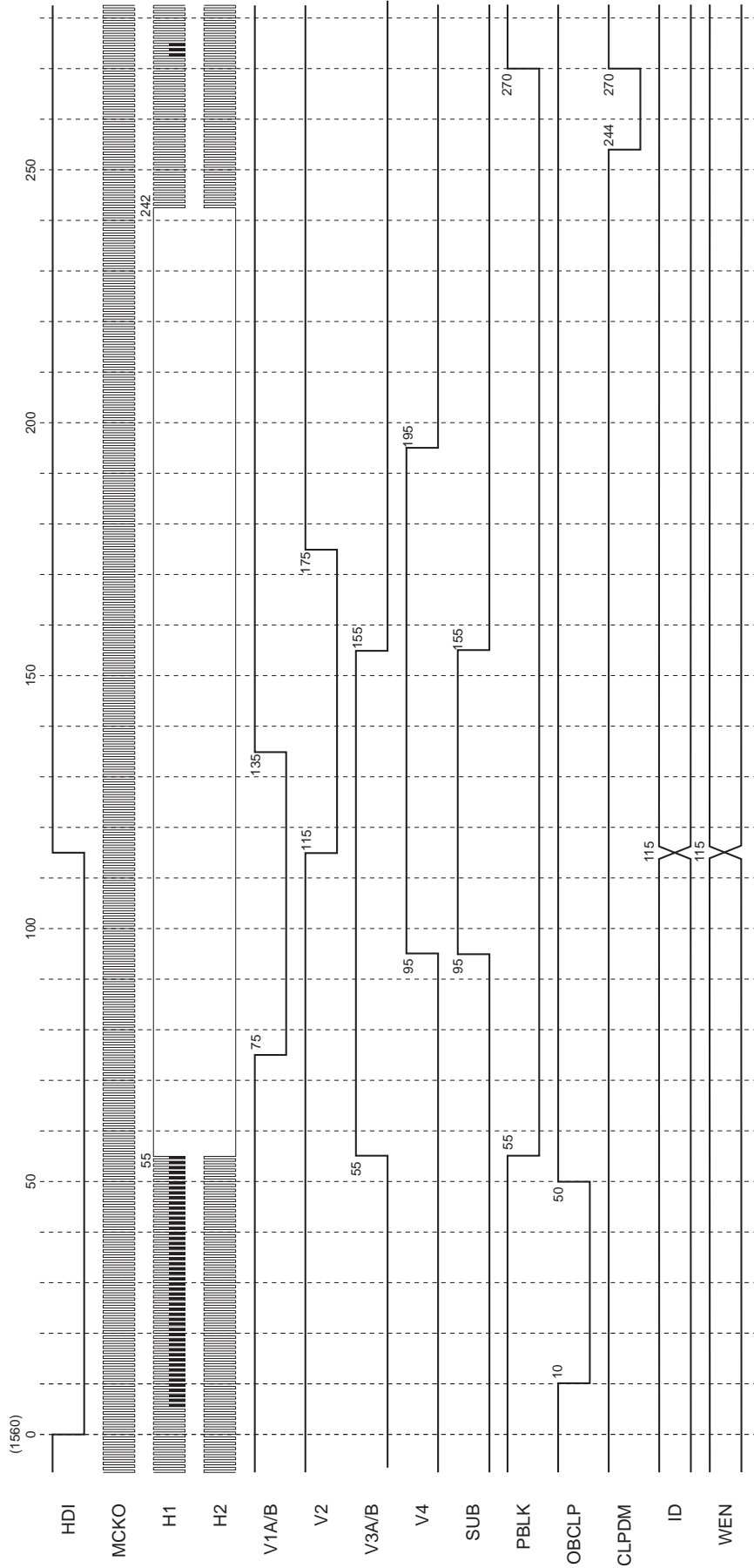


* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
 * ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component.

Applicable CCD image sensor
 • ICX202/ICX232

MODE
 Frame mode

Chart-10 Horizontal Direction Timing Chart



- * The HDI of this chart indicates the actual CXD2470R load timing.
- * The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HDI.
- * The HDI fall period should be between approximately 3.0 to 13.4μs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4μs).
- * SUB is output at the timing shown above when output is controlled by the serial interface data.
- * ID and WEN are output at the timing shown above at the position shown in Chart-8.

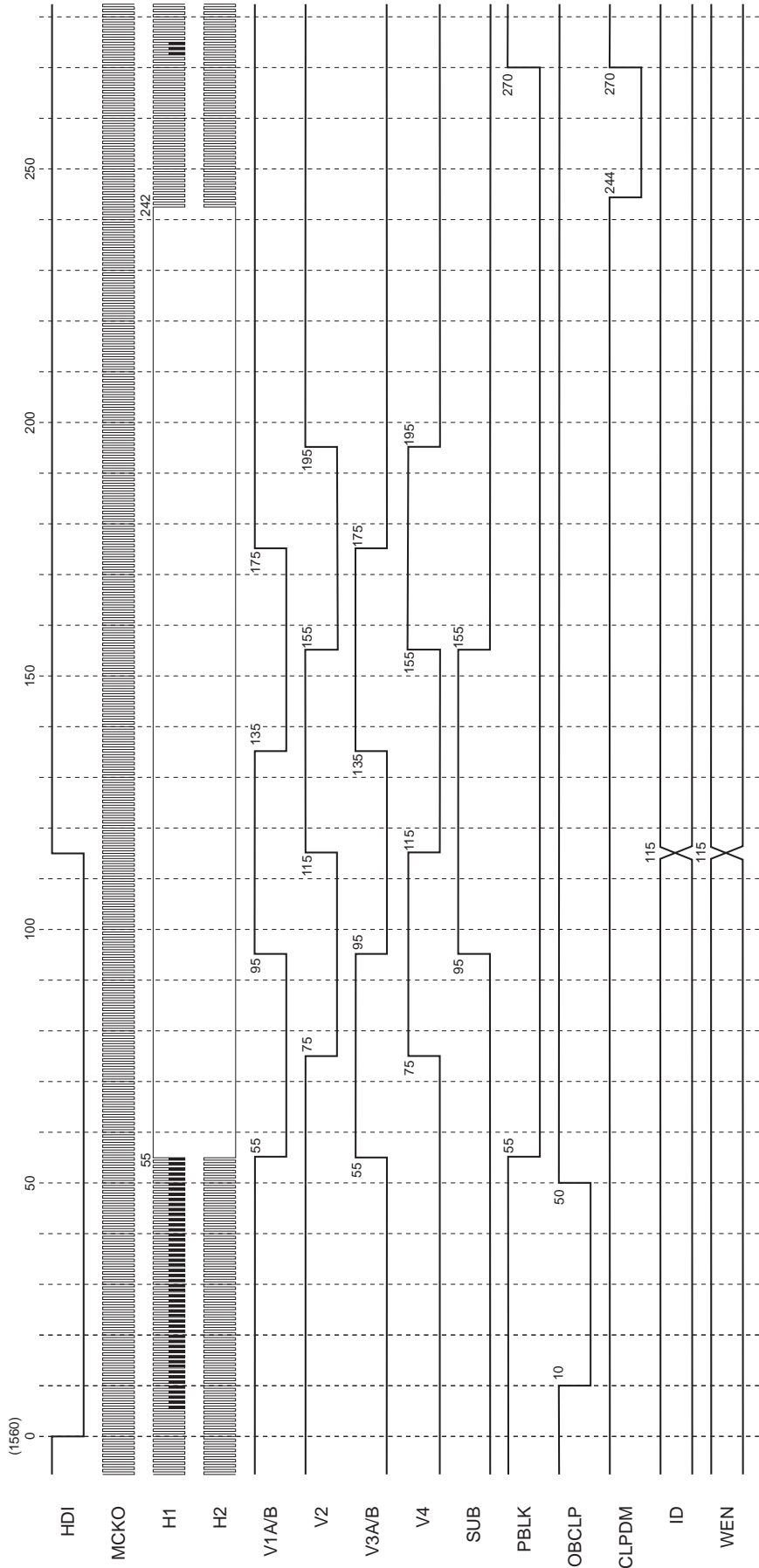
Applicable CCD image sensor

- ICX202/ICX232

MODE

Quadruple-speed mode

Chart-11 Horizontal Direction Timing Chart

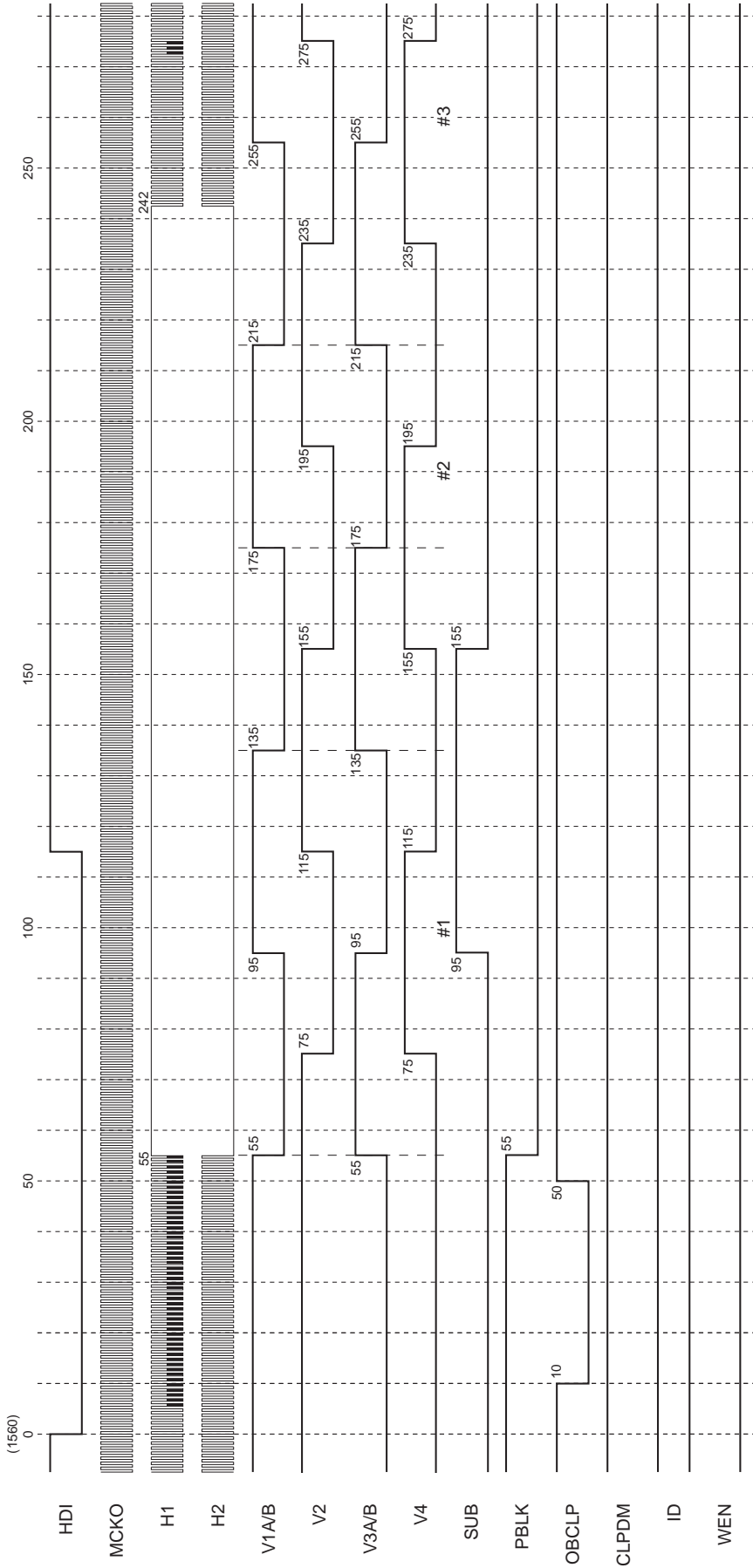


- * The HDI of this chart indicates the actual CXD2470R load timing.
- * The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HDI.
- * The HDI fall period should be between approximately 3.0 to 13.4μs (when the drive frequency is 18MHz). This chart shows a period of 115clk (6.4μs).
- * SUB is output at the timing shown above when output is controlled by the serial interface data.
- * ID and WEN are output at the timing shown above at the position shown in Chart-9.

Applicable CCD image sensor
 • ICX202/ICX232

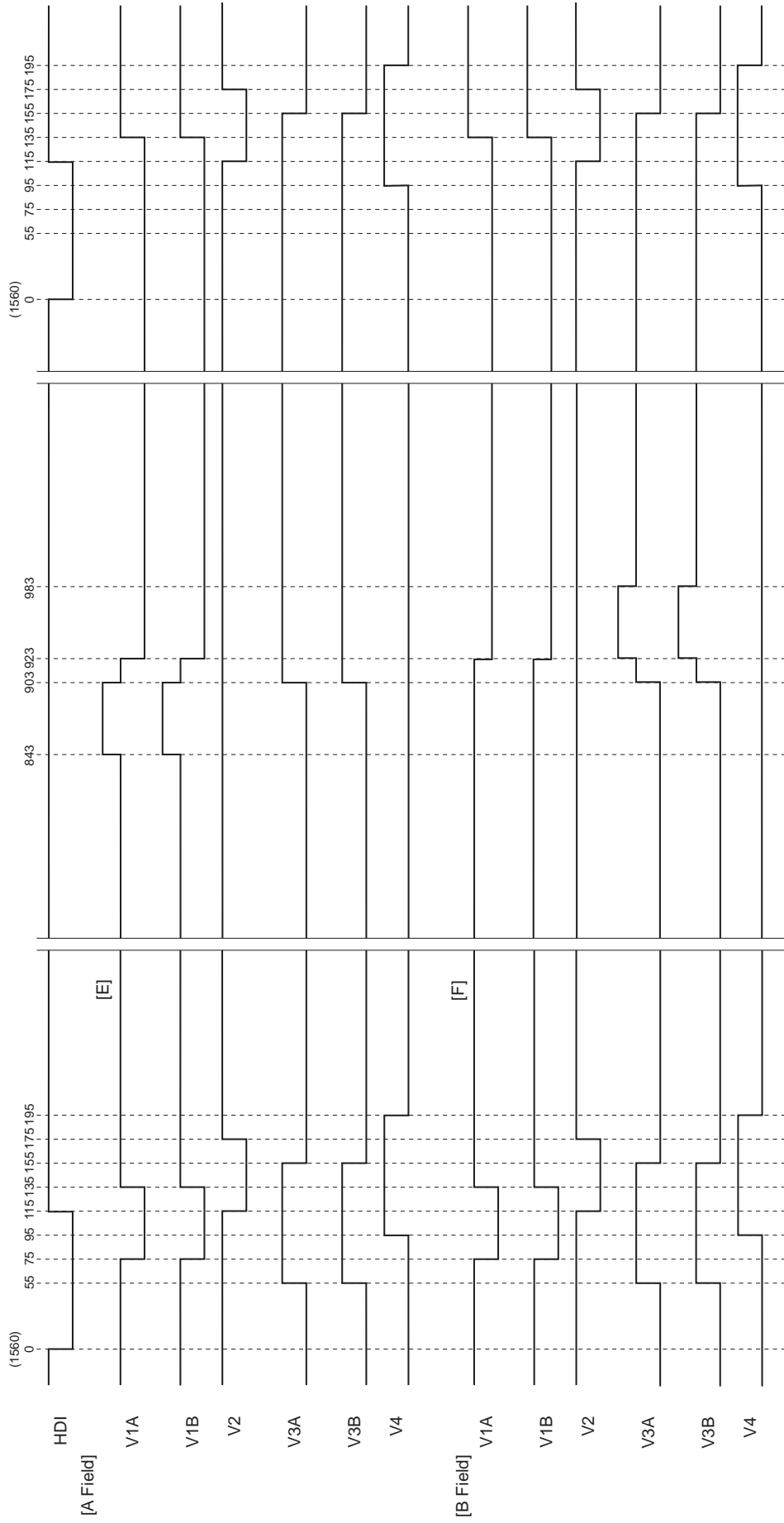
MODE
 Frame mode

Chart-12 Horizontal Direction Timing Chart
 (High-speed sweep: G)



* The HDI of this chart indicates the actual CXD2470R load timing.
 * The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HDI.
 * The HDI fall period should be between approximately 3.0 to 13.4μs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4μs).
 * SUB is output at the timing shown above when output is controlled by the serial interface data.
 * High-speed sweep of V1A/B, V2, V3A/B and V4 is performed up to 33H of 1295ck (#659).

Chart-13 Horizontal Direction Timing Chart **MODE** Frame mode **Applicable CCD image sensor**
 • ICX202/ICX232

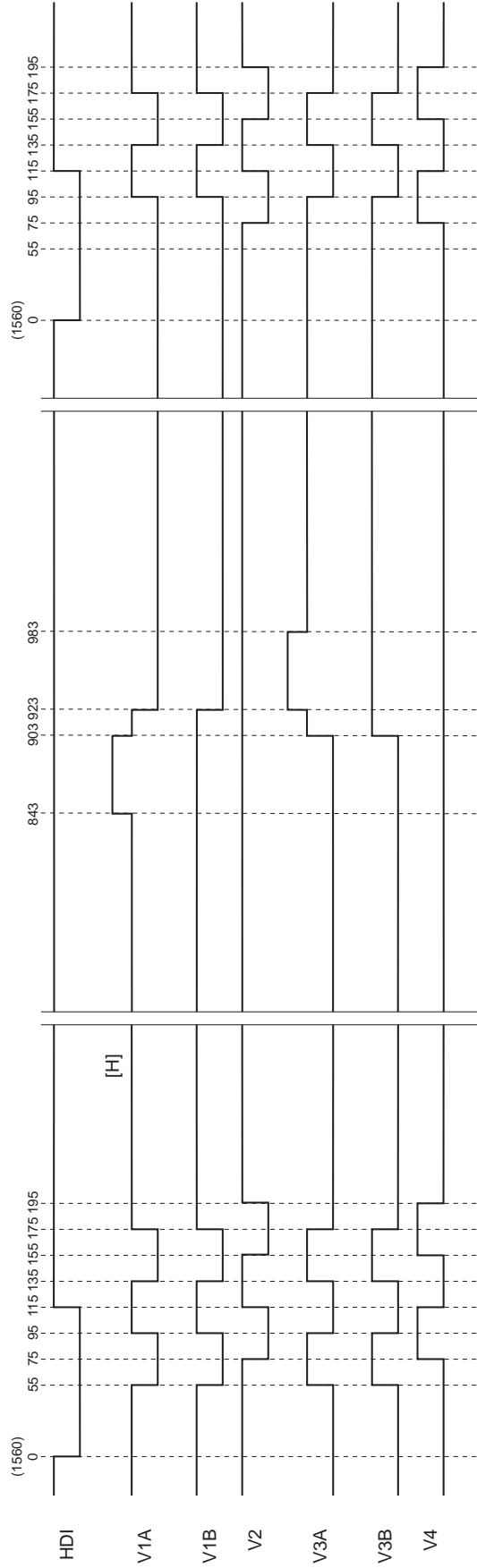


* The HDI of this chart indicates the actual CXD2470R load timing.
 * The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HDI.
 * The HDI fall period should be between approximately 3.0 to 13.4µs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4µs).

Applicable CCD image sensor
 • ICX202/ICX232

MODE
 Quadruple-speed mode

Chart-14 Horizontal Direction Timing Chart

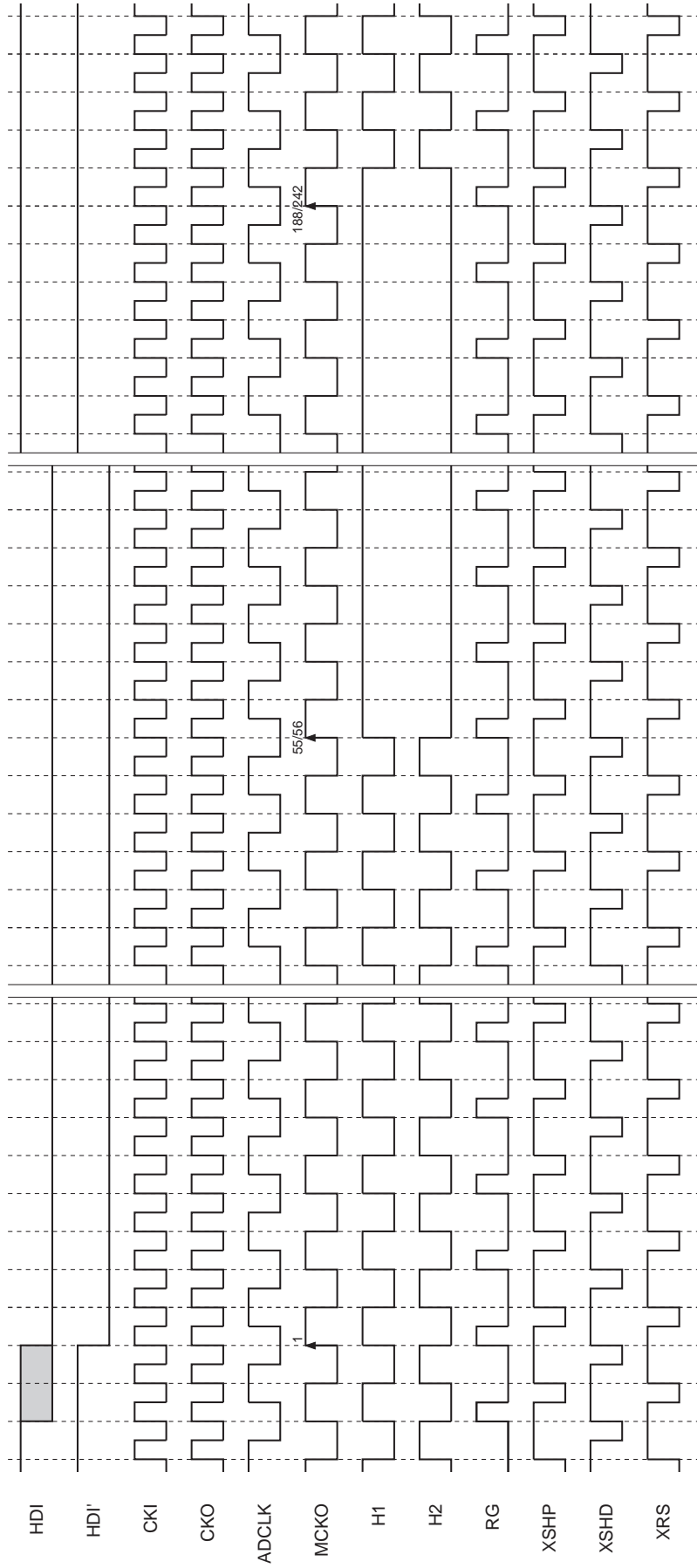


* The HDI of this chart indicates the actual CXD2470R load timing.
 * The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HDI.
 * The HDI fall period should be between approximately 3.0 to 13.4μs (when the drive frequency is 18MHz). This chart shows a period of 115ck (6.4μs).

Chart-15 High-Speed Phase Timing Chart

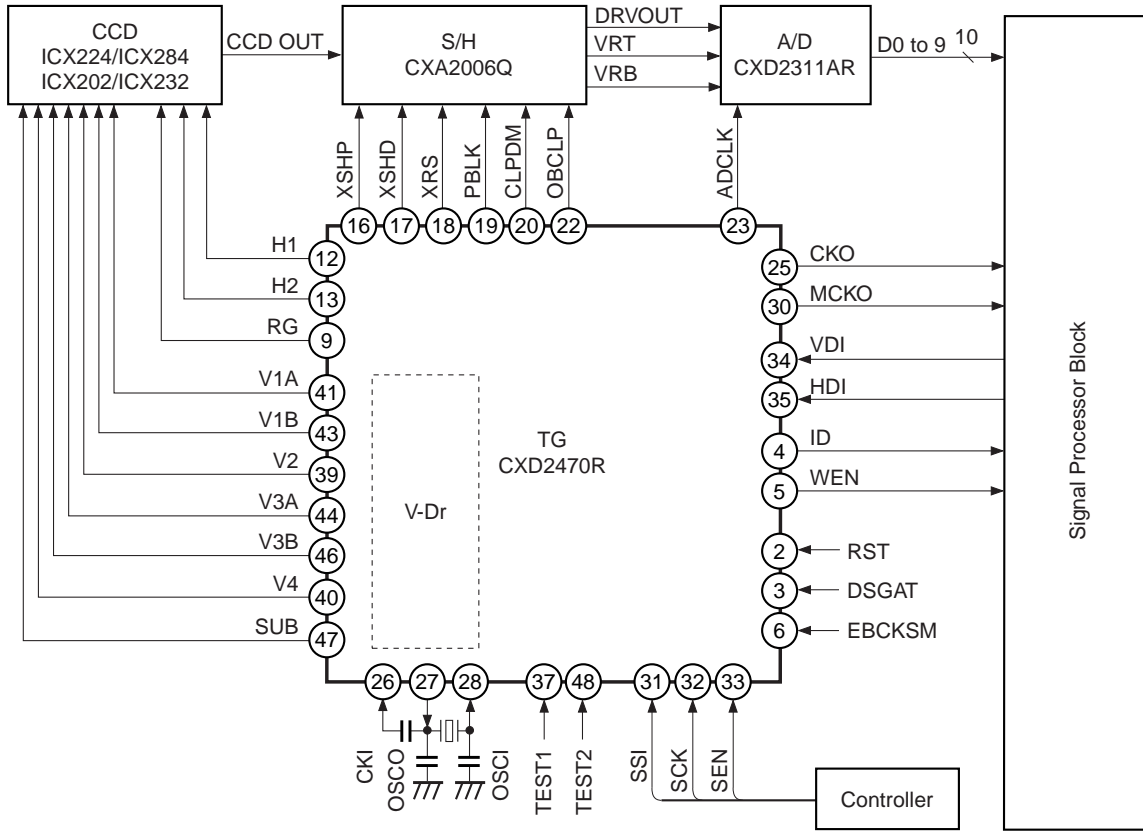
MODE

Applicable CCD image sensor
 • ICX224/ICX284/ICX202/ICX232



* HDI' indicates the HDI which is the actual CXD2470R load timing.
 * The phase relationship of each pulse shows the logical position relationship. For the actual output waveform, a delay is added to each pulse.
 * The logical phase of ADCLK can be specified by the serial interface.

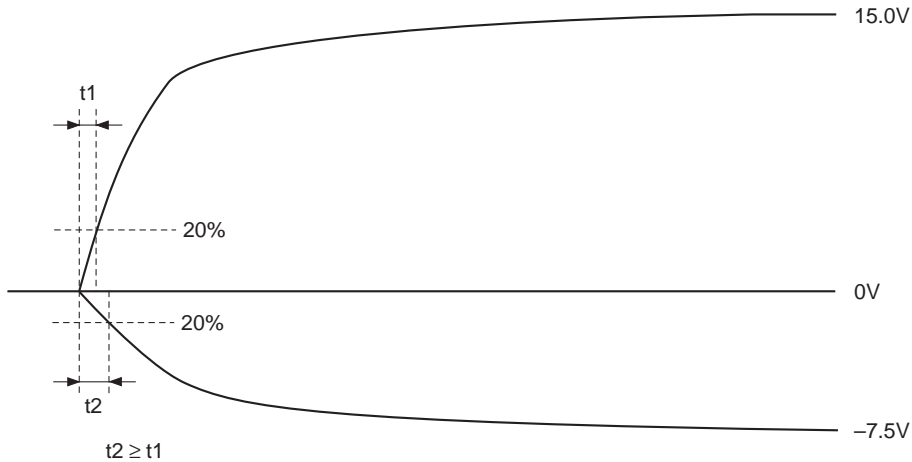
Application Circuit Block Diagram



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes for Power-on

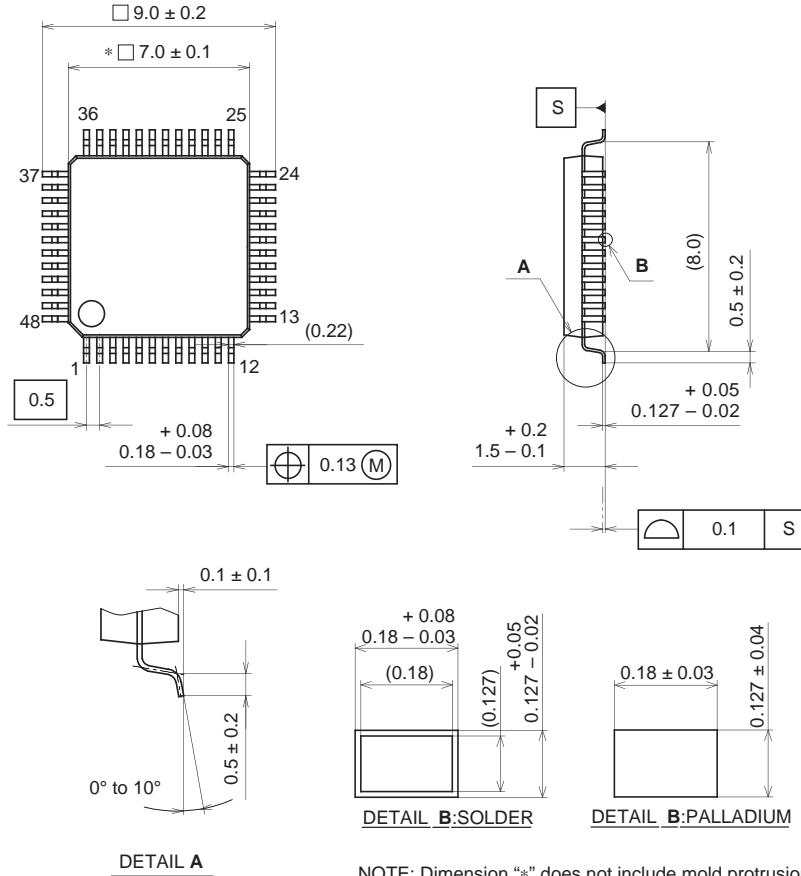
Of the three -7.5V, +15.0V and +3.3V power supplies, be sure to start up the -7.5V and +15.0V power supplies in the following order to prevent the SUB pin of the CCD image sensor from going to negative potential.



Package Outline

Unit: mm

48PIN LQFP (PLASTIC)



| | |
|------------|----------------|
| SONY CODE | LQFP-48P-L01 |
| EIAJ CODE | LQFP048-P-0707 |
| JEDEC CODE | _____ |

PACKAGE STRUCTURE

| | |
|------------------|--------------------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER/PALLADIUM PLATING |
| LEAD MATERIAL | 42/COPPER ALLOY |
| PACKAGE MASS | 0.2g |