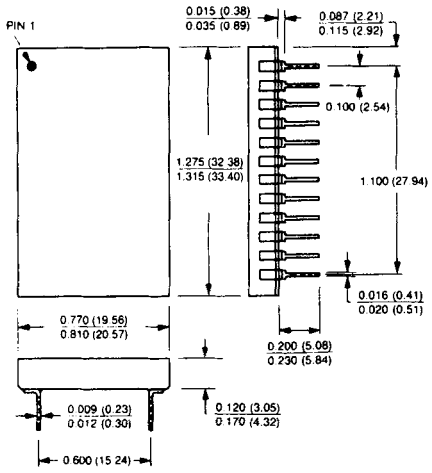
Low-Power CMOS, 12-bit A/D Converters

FEATURES

- Low Power 125mW Maximum
- Small 24-Pin DIP
- Linearity and No Missing Codes Guaranteed Over Temperature
- ±0.1% FSR Absolute Accuracy
- Totally Adjustment Free No Full-Scale or Zero Adjustments Necessary
- Full Mil Operation −55°C to +125°C
- MIL-PRF-38534 Screening Optional

24 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN5250 Series devices are extremely low-power, 12-bit, successive approximation A/D converters in industry-standard, 24-pin, ceramic, dual-in-line packages. Power consumption is 125mW maximum.

Combining the advantages of highly stable thin-film resistors, functional laser trimming and hermetic packaging, the MN5250 Series offers designers the ultimate in convenience for high-resolution, low-power analog-to-digital conversion. All devices are supplied complete with internal reference, and no external trimming components or adjustments are necessary to meet published specifications.

Four input voltage rages are offered, and all units are fully specified and 100% tested for linearity and accuracy at their operating temperature extremes as well as at room temperature. All models of the MN5250 Series may be procured for operation over the full −55°C to +125°C military temperature range (“H” models) or the 0°C to +70°C commercial temperature range. For military/aerospace or harsh-environment commercial/industrial applications, “H/B CH” models are fully screened to MIL-PRF-38534, class H requirements.

The MN5250 Series is the ideal choice for designs requiring high resolution and low power consumption. Their small size, low power consumption and adjustment-free operation make them excellent selections for compact, highly reliable systems. Typical applications include remote-site seismological monitoring, precision portable instruments and high-accuracy industrial instrumentation.

MN5250 SERIES LOW-POWER CMOS 12-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C
	−55°C to +125°C ("H" Models)
Storage Temperature	−65°C to +150°C
+12V Supply (Pin 15)	+18 Volts
−12V Supply (Pin 13)	−18 Volts
Logic Supply (+Vdd, Pin 2)	−0.5 to+16 Volts
Analog Input (Pin 14)	±25 Volts
Digital Inputs (Pins 1, 24)	−0.5 to +Vdd

ORDERING INFORMATION

PART NUMBER — MN525X H /B CH

Select MN5250, MN5251, MN5252, or MN5253.
Standard Part is specified for 0°C to +70°C operation.
Add "H" suffix for specified −55°C to +125°C operation.
Add "/B" to "H" devices for Environmental Stress Screening.
Add "CH" to "H/B" devices for 100% screening according to MIL-PRF-38534.

SPECIFICATIONS (T_A = +25° C, Supply Voltages ±12V and +5V, unless otherwise specified).

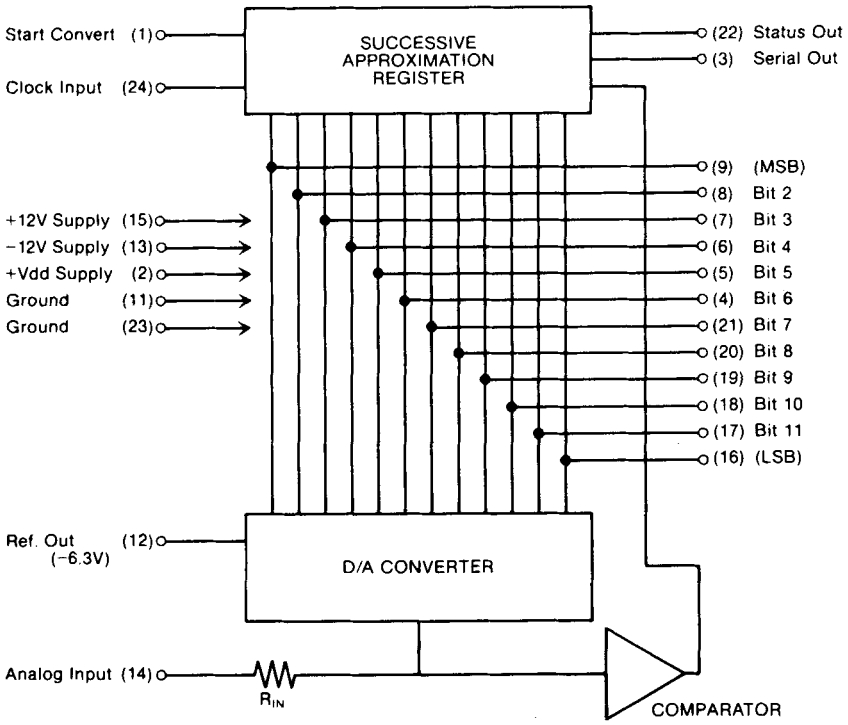
ANALOG INPUTS	+Vdd	MIN.	TYP.	MAX.	UNITS
Input Voltage Range (Input Impedance): MN5250 (50KΩ)			0 to −10		Volts
MN5251 (50KΩ)			− 5 to + 5		Volts
MN5252 (100KΩ)			−10 to +10		Volts
MN5253 (50KΩ)			0 to +10		Volts
DIGITAL INPUTS					
Logic Levels (Note 1): Logic "1"	+ 5V	3.5			Volts
	+12V	8.4			Volts
Logic "0"	+ 5V			1.5	Volts
	+12V			3.5	Volts
Loading: Input Current			10		pA
Input Capacitance (V_{in}=0V)			5		pF
Start Convert Input: Pulse Width	+ 5V	750			nSec
	+12V	250			nSec
Setup Time Start High to Clock	+ 5V	300			nSec
	+12V	150			nSec
Clock Input: Frequency (Note 2)				71	kHz
Positive Pulse Width (Note 3)	+ 5V	600			nSec
	+12V	300			nSec
Rise and Fall Times (Note 3)	+ 5V			15	µSec
	+12V			4	µSec
TRANSFER CHARACTERISTICS					
Linearity Error (Note 4): +25°C			±¼	±½	LSB
0°C to +70°C			±¼	±½	LSB
−55°C to +125°C ("H" Models)			±½	±1	LSB
Differential Linearity Error			±½		LSB
No Missing Codes (0°C to +70°C)			Guaranteed		
Full Scale Absolute Accuracy Error (Notes 5, 6):					
+25°C			± 0.05	± 0.1	%FSR
0°C to +70°C			± 0.2	± 0.5	%FSR
−55°C to +125°C ("H" Models)			± 0.3	± 0.6	%FSR
Zero Error (Notes 5, 6): +25°C			± 0.01		%FSR
0°C to +70°C			± 0.04	± 0.1	%FSR
−55°C to +125°C ("H" Models)			± 0.05	± 0.1	%FSR
Gain Error (Note 5)			± 0.05		%
Gain Drift			±20		ppm/°C
DYNAMIC CHARACTERISTICS					
Conversion Time (Note 2)				175	µSec
Analog Input Settling Time (Note 8)			2		µSec
DIGITAL OUTPUTS					
Logic Coding (Note 9): Unipolar Ranges			Complementary Straight Binary		
Bipolar Ranges			Complementary Offset Binary		
Logic Levels (Note 1): Logic "1"	+ 5V	4.95			Volts
	+12V	11.95			Volts
Logic "0"	+ 5V			0.01	Volts
	+12V			0.05	Volts
Output Drive Current, All Outputs:					
Logic "1" (V_{OH}=2.5V)	+ 5V	0.2	1.7		mA
(V_{OH}=11V)	+12V	0.3	1.0		mA
Logic "0" (V_{OL}=0.4V)	+ 5V	0.1	0.6		mA
(V_{OL}=1.5V)	+12V	1.0	4.0		mA

REFERENCE OUTPUT	+Vdd	MIN.	TYP.	MAX.	UNITS
Internal Reference: Voltage			− 6.3		Volts
Accuracy			± 5.		%
Tempco of Drift			±15.		ppm/°C
Ext. Current Without Buffering				10	μA
POWER SUPPLY REQUIREMENTS					
Power Supply Range (Note 10): +12V Supply		+11.64	+12.00	+12.36	Volts
−12V Supply		−11.64	−12.00	−12.36	Volts
+ 5V Supply		+ 4.75	+ 5.00	+12.36	Volts
Power Supply Rejection: +12V Supply			± 0.003		%FSR/%Vs
−12V Supply			± 0.03		%FSR/%Vs
+ 5V Supply			± 0.0003		%FSR/%Vs
Current Drain: +12V Supply			2.4	3.5	mA
−12V Supply			− 2.0	4	mA
+ 5V Supply			0.5	6.5	mA
Power Consumption			56	125	mW

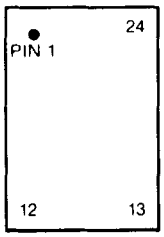
SPECIFICATION NOTES:

1. The +Vdd Logic Suppy (Pin 2) can be at any voltage between +5V (low power TTL compatibility) and +12V (CMOS compatibility).
2. Conversion Time is defined as the width of the converter's STATUS (E.O.C.) pulse. See Timing Diagram. For MN5250 Series A/D's, a 175 μSec conversion time corresponds to an external clock frequency of 71 KHz. Micro Networks guarantees linearity and absolute accuracy at and below this clock frequency.
3. The clock may be asymmetrical, and it may ramp up and down as long as it meets minimum pulse width and maximum rise and fall time requirements.
4. Micro Networks tests and guarantees maximum linearity error at room temperature and at the high and low extremes of the specified operating temperature range.
5. See the tutorial section of the Micro Networks' Product Guide and Applications Manual for an explanation of how Micro Networks defines Full Scale Absolute Accuracy, Zero, and Gain Errors. For MN5250 Series A/D's we 100% test Full Scale Absolute Accuracy Error and Zero Error at room temperature and at the high and low extremes of the specified operating temperature range.
6. 1 LSB for a 12 bit converter corresponds to 0.024%FSR. See Note 7.
7. FSR stands for Full Scale Range and is equal to the peak to peak input voltage of the selected converter. For the MN5250, MN5251, and MN5253, FSR = 10V, and 1 LSB = 2.44mV. For the MN5252, FSR = 20V, and 1LSB = 4.88mV.
8. Analog Input Settling Time is the time required for the input circuitry to settle to within ±½ LSB for a 10V step in input signal.
9. Serial and parallel output data have the same coding. Serial data is in Non-Return to Zero (NRZ) format. See Output Coding and Timing Diagram.
10. The recommended range for the ±12V supplies is ±3%. Units will operate over a range of ±10V to ±14V with reduced accuracy.

BLOCK DIAGRAM



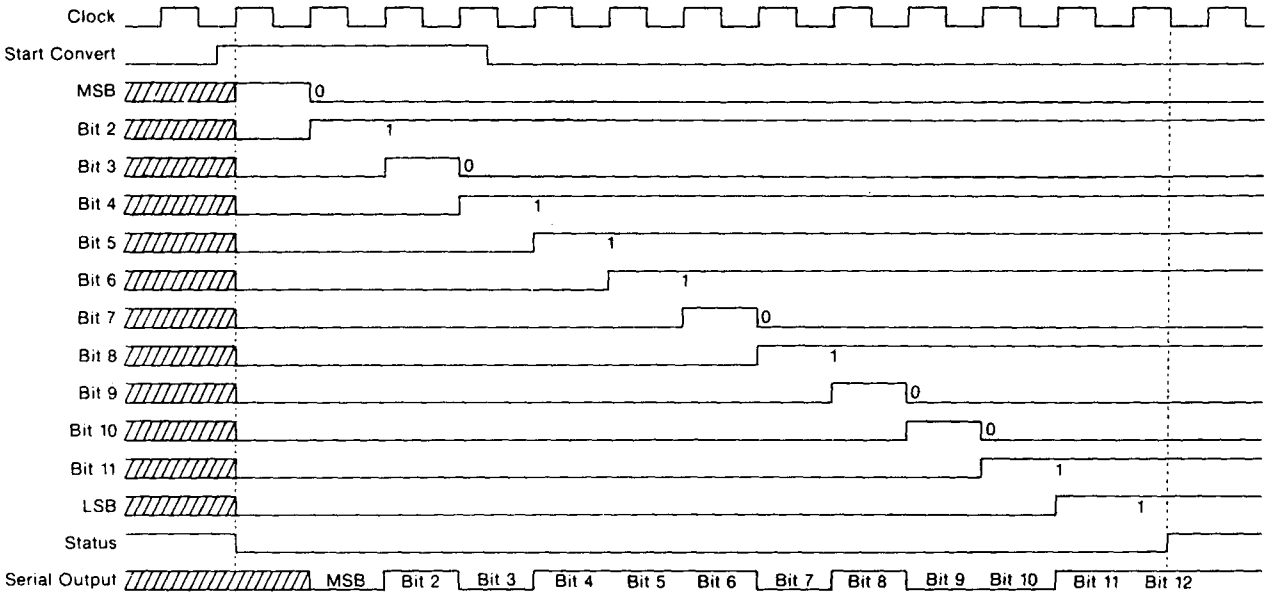
PIN DESIGNATIONS



Pin 1. Start Convert
Pin 2. Logic Supply (+Vdd)
Pin 3. Serial Output
Pin 4. Bit 6
Pin 5. Bit 5
Pin 6. Bit 4
Pin 7. Bit 3
Pin 8. Bit 2
Pin 9. Bit 1 (MSB)
Pin 10. N/C
Pin 11. Ground
Pin 12. Ref. Out (−6.3V)

Pin 13. −12V Supply
Pin 14. Analog Input
Pin 15. +12V Supply
Pin 16. Bit 12 (LSB)
Pin 17. Bit 11
Pin 18. Bit 10
Pin 19. Bit 9
Pin 20. Bit 8
Pin 21. Bit 7
Pin 22. Status (E.O.C.)
Pin 23. Ground
Pin 24. Clock Input

TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. Operation shown is for the digital word 0101 1101 0011 which corresponds to 6.357V on the 0 to +10V (MN5253) input range. See Output Coding.
2. Conversion Time is defined as the width of the Status (E.O.C.) pulse.
3. The converter is reset (MSB = "1", all other bits = "0", Status = "0") by holding the Start Convert high during a low to high clock transition; the Start Convert must be high for a minimum of 300nsec prior to the clock transition. Output bits, starting with the MSB, will be set to their final values on succeeding clock edges. The Start Convert must return low prior to the falling edge of the fourth clock cycle after conversion commences.
4. The Start Convert may be brought high at any time during a conversion to reset and begin converting again.
5. The delay between the resetting clock edge and the Status actually dropping to a "0" is 750nsec maximum.
6. The Status (E.O.C.) output will rise to a "1" 750nsec (maximum) after the first falling clock edge after the determination of LSB. Status will remain high until the converter is reset. Parallel output data is valid as long as Status is a "1".
7. Both serial and parallel data bits become valid on the same rising clock edges. Serial data is valid on subsequent falling clock edges, and these edges can be used to clock serial data into receiving registers.
8. For continuous conversion, connect the Status output pin (pin 22) to the Start Convert input (Pin 1).
9. When the converter is initially "powered up", it may come on at any point in the conversion cycle.

DIGITAL OUTPUT CODING

ANALOG INPUT				DIGITAL OUTPUT	
MN5250	MN5251	MN5252	MN5253	MSB	LSB
0.0000V − 0.0024V	+ 5.0000V + 4.9976V	+10.0000V + 9.9951V	+10.0000V + 9.9976V	0000 0000 0000 0000 0000 0000*
− 4.9976V − 5.0000V − 5.0024V	+ 0.0024V 0.0000V − 0.0024V	+ 0.0049V 0.0000V − 0.0049V	+ 5.0024V + 5.0000V + 4.9976V	0111 1111 1110* 1000 0000 0000* 1000 0000 0000*
− 9.9976V −10.0000V	− 4.9976V − 5.0000V	− 9.9951V −10.0000V	+ 0.0024V 0.0000V	1111 1111 1110* 1111 1111 1111

* Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as 0 will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN5252 (±10V analog input range) the transition from digital output 1111 1111 1111 to 1111 1111 1110 (or vice versa) will ideally occur at an input voltage of −9.9951 volts. Subsequently, any input voltage more negative than −9.9951 volts will give a digital output of all "1's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 (or vice versa) will ideally occur at an input of zero volts, and the 0000 0000 0000 to 0000 0000 0001 (or vice versa) transition should occur at +9.9951 volts. An input greater than +9.9951 volts will give all "0's".

APPLICATIONS INFORMATION

The digital circuitry used in the MN5250 Series A/D's is CMOS. The standard precautionary measures for handling CMOS should be followed.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5250 Series converters. The units' two GROUND pins (Pins 11 and 23) are not connected internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01 μF bypass capacitor should be connected between Pins 11 and 23 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the converters. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagram below.