National Semiconductor

# NM93C06/C46/C56/C66
# 256-/1024-/2048-/4096-Bit Serial EEPROM (MICROWIRE™ Bus Interface)

## General Description

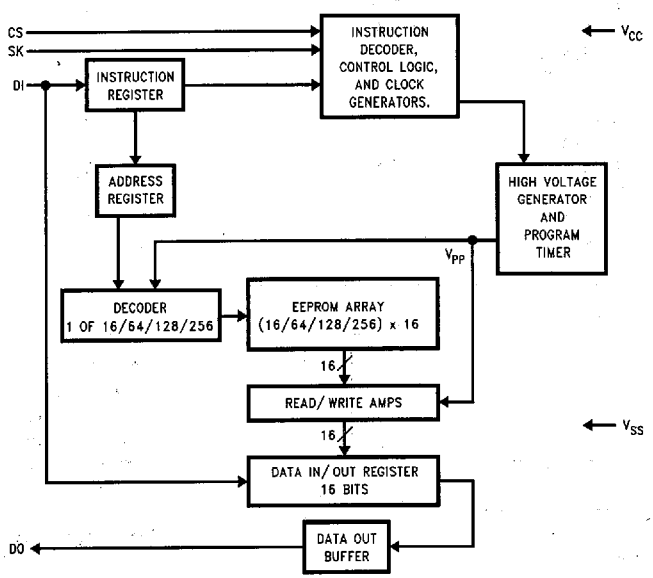
The NM93C06/C46/C56/C66 devices are 256/1024/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. These memory devices are available in both SO and TSSOP packages for small space considerations.

The EEPROM Interfacing is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin during programming.

## Features

- Device status during programming mode
- Typical active current of 200 μA; Typical standby current of 10 μA
- No erase required before write
- Reliable CMOS floating gate technology
- 4.5V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: $10^6$ data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

## Block Diagram

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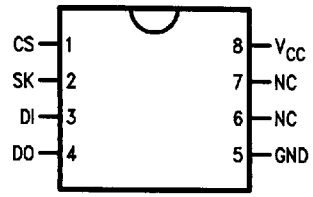
## Connection Diagrams

**Dual-In-Line Package (N)**
**8-Pin SO (M8) and 8-Pin TSSOP (MT8)**

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**Top View**

**See NS Package Number**
**N08E, M08A and MTC08**

**Pin Names**

| | |
|---|---|
| CS | Chip Select |
| SK | Serial Data Clock |
| DI | Serial Data Input |
| DO | Serial Data Output |
| GND | Ground |
| $V_{CC}$ | Power Supply |

## Ordering Information

**Commercial Temp. Range (0°C to +70°C)**

| Order Number |
|---|
| NM93C06N/NM93C46N |
| NM93C56N/NM93C66N |
| NM93C06M8/NM93C46M8 |
| NM93C56M8/NM93C66M8 |
| NM93C06MT8/NM93C46MT8 |
| NM93C56MT8/NM93C66MT8 |

**Extended Temp. Range (−40°C to +85°C)**

| Order Number |
|---|
| NM93C06EN/NM93C46EN |
| NM93C56EN/NM93C66EN |
| NM93C06EM8/NM93C46EM8 |
| NM93C56EM8/NM93C66EM8 |
| NM93C06EMT8/NM93C46EMT8 |
| NM93C56EMT8/NM93C66EMT8 |

**Automotive Temp. Range (−40°C to +125°C)**

| Order Number |
|---|
| NM93C06VN/NM93C46VN |
| NM93C56VN/NM93C66VN |
| NM93C06VM8/NM93C46VM8 |
| NM93C56VM8/NM93C66VM8 |
| NM93C06VMT8/NM93C46VMT8 |
| NM93C56VMT8/NM93C66VMT8 |

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Ambient Storage Temperature | −65°C to +150°C |
| All Input or Output Voltages with Respect to Ground | +6.5V to −0.3V |
| Lead Temp. (Soldering, 10 sec.) | +300°C |
| ESD Rating | 2000V |

## Operating Conditions

| | |
|---|---|
| Ambient Operating Temperature | |
| NM93C06–NM93C66 | 0°C to +70°C |
| NM93C06E–NM93C66E | −40°C to +85°C |
| NM93C06V–NM93C66V | −40°C to +125°C |
| Power Supply ($V_{CC}$) | 4.5V to 5.5V |

## DC and AC Electrical Characteristics $V_{CC}$ = 5.0V ±10% unless otherwise specified

**Note:** Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

| Symbol | Parameter | Part Number | Conditions | Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CCA}$ | Operating Current | NM93C06-NM93C66<br>NM93C06E/V-NM93C66E/V | CS = $V_{IH}$, SK = 1 MHz<br>SK = 1 MHz | | 1<br>1 | mA |
| $I_{CCS}$ | Standby Current | NM93C06-NM93C66<br>NM93C06E/V-NM93C66E/V | CS = $V_{IL}$ | | 50<br>50 | μA<br>μA |
| $I_{IL}$<br>$I_{OL}$ | Input Leakage<br>Output Leakage | | $V_{IN}$ = 0V to $V_{CC}$<br>(Note 3) | | ±1 | μA |
| $V_{IL}$<br>$V_{IH}$ | Input Low Voltage<br>Input High Voltage | | | −0.1<br>2 | 0.8<br>$V_{CC}$ + 1 | V |
| $V_{OL1}$<br>$V_{OH1}$ | Output Low Voltage<br>Output High Voltage | | $I_{OL}$ = 2.1 mA<br>$I_{OH}$ = −400 μA | <br>2.4 | 0.4 | V<br>V |
| $V_{OL2}$<br>$V_{OH2}$ | Output Low Voltage<br>Output High Voltage | | $I_{OL}$ = 10 μA<br>$I_{OH}$ = −10 μA | <br>$V_{CC}$ − 0.2 | 0.2 | V |
| $f_{SK}$ | SK Clock Frequency | NM93C06-NM93C66<br>NM93C06E/V-NM93C66E/V | (Note 4) | 0<br>0 | 1<br>1 | MHz |
| $t_{SKH}$ | SK High Time | NM93C06-NM93C66<br>NM93C06E/V-NM93C66E/V | | 250<br>300 | | ns |
| $t_{SKL}$ | SK Low Time | | | 250 | | ns |
| $t_{SKS}$ | SK Setup Time | | SK must be at $V_{IL}$ for $t_{SKS}$ before CS goes high | 50 | | ns |
| $t_{CS}$ | Minimum CS Low Time | NM93C06-NM93C66<br>NM93C06E/V-NM93C66E/V | (Note 2) | 250<br>250 | | ns |

## DC and AC Electrical Characteristics $V_{CC}$ = 5.0V ±10% (unless otherwise specified) (Continued)

| Symbol | Parameter | Part Number | Conditions | Min | Max | Units |
|---|---|---|---|---|---|---|
| $t_{CSS}$ | CS Setup Time | NM93C06-NM93C66<br>NM93C06E/V-NM93C66E/V | | 50<br>50 | | ns |
| $t_{DH}$ | DO Hold Time | | | 70 | | ns |
| $t_{DIS}$ | DI Setup Time | NM93C06-NM93C66<br>NM93C06E/V-NM93C66E/V | | 100<br>200 | | ns |
| $t_{CSH}$ | CS Hold Time | | | 0 | | ns |
| $t_{DIH}$ | DI Hold Time | | | 20 | | ns |
| $t_{PD1}$ | Output Delay to "1" | NM93C06-NM93C66<br>NM93C06E/V-NM93C66E/V | | | 500<br>500 | ns |
| $t_{PD0}$ | Output Delay to "0" | NM93C06-NM93C66<br>NM93C06E/V-NM93C66E/V | | | 500<br>500 | ns |
| $t_{SV}$ | CS to Status Valid | NM93C06-NM93C66<br>NM93C06E/V-NM93C66E/V | | | 500<br>500 | ns |
| $t_{DF}$ | CS to DO in TRI-STATE® | NM93C06-NM93C66<br>NM93C06E/V-NM93C66E/V | CS = $V_{IL}$ | | 100<br>100 | ns |
| $t_{WP}$ | Write Cycle Time | | | | 10 | ms |

## Capacitance

$T_A$ = 25°C f = 1 MHz

| Symbol | Test | Typ | Max | Units |
|---|---|---|---|---|
| $C_{OUT}$ | Output Capacitance | | 5 | pF |
| $C_{IN}$ | Input Capacitance | | 5 | pF |

**Note 1:** Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** CS (Chip Select) must be brought low (to $V_{IL}$) for an interval of $t_{CS}$ in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (This is shown in the opcode diagrams in the following pages).

**Note 3:** Typical leakage values are in the 20 nA range.

**Note 4:** The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the $f_{SK}$ parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both $t_{SKH}$ and $t_{SKL}$ limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

## AC Test Conditions

| $V_{CC}$ Range | $V_{IL}/V_{IH}$ Input Levels | $V_{IL}/V_{IH}$ Timing Level | $V_{OL}/V_{OH}$ Timing Level | $I_{OL}/I_{OH}$ |
|---|---|---|---|---|
| 4.5V ≤ $V_{CC}$ ≤ 5.5V (TTL Levels) | 0.4V/2.4V | 1.0V/2.0V | 0.4V/2.4V | −2.1 mA/0.4 mA |
| Output Load: 1 TTL Gate ($C_L$ = 100 pF) | | | | |

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## Functional Description

The NM93C06/C46/C56/C66 devices have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the C06 and C46 the next 8 bits carry the op code and the 6-bit address for register selection. For the C56 and C66 the next 10-bits carry the op code and the 8-bit address for register selection.

All Data in signals are clocked into the device on the low-to-high SK transition.

**Read (READ):**

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

**Erase/Write Enable (WEN):**

When $V_{CC}$ is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable WEN instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (WDS) instruction is executed or $V_{CC}$ is completely removed from the part.

**Erase (ERASE):**

The ERASE instruction will program all bits in the selected register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the $t_{CS}$ interval. DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

**Write (WRITE):**

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the $t_{CS}$ interval. DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

**Erase All (ERAL):**

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the $t_{CS}$ interval.

**Write All (WRALL):**

The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the $t_{CS}$ interval.

**Write Disable (WDS):**

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

**NOTE:** The NSC CMOS EEPROMs do not require an 'ERASE' or 'ERASE ALL' operation prior to the 'WRITE' and 'WRITE ALL' instructions. The 'ERASE' and 'ERASE ALL' instructions are included to maintain compatibility with earlier technology EEPROMs.

## Instruction Set for the NM93C06 and NM93C46

| Instruction | SB | Op Code | Address | Data | Comments |
|---|---|---|---|---|---|
| READ | 1 | 10 | A5–A0 | | Reads data stored in memory, at specified address. |
| WEN | 1 | 00 | 11XXXX | | Enable all programming modes. |
| ERASE | 1 | 11 | A5–A0 | | Erase selected register. |
| WRITE | 1 | 01 | A5–A0 | D15–D0 | Writes selected register. |
| ERAL | 1 | 00 | 10XXXX | | Erases all registers. |
| WRALL | 1 | 00 | 01XXXX | D15–D0 | Writes all registers. |
| WDS | 1 | 00 | 00XXXX | | Disables all programming modes. |

**Note:** Address bits A5 and A4 become "Don't Care" for the NM93C06.

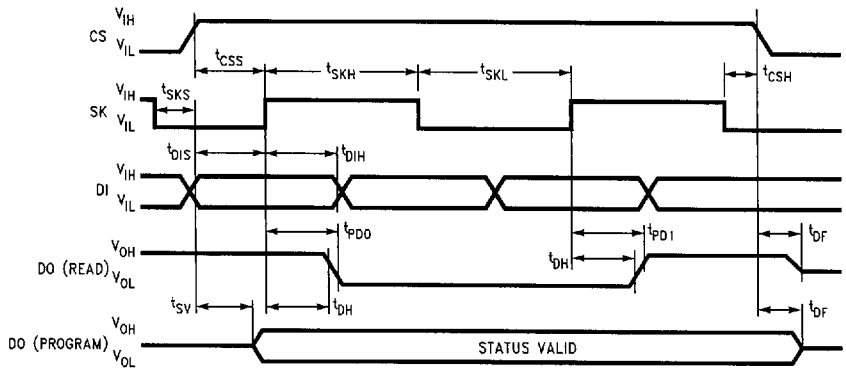
## Instruction Set for the NM93C56 and NM93C66

| Instruction | SB | Op Code | Address | Data | Comments |
|---|---|---|---|---|---|
| READ | 1 | 10 | A7–A0 | | Reads data stored in memory, at specified address. |
| WEN | 1 | 00 | 11XXXXXX | | Enable all programming modes. |
| ERASE | 1 | 11 | A7–A0 | | Erase selected register. |
| ERAL | 1 | 00 | 10XXXXXX | | Erases all registers. |
| WRITE | 1 | 01 | A7–A0 | D15–D0 | Writes selected register. |
| WRALL | 1 | 00 | 01XXXXXX | D15–D0 | Writes all registers. |
| WDS | 1 | 00 | 00XXXXXX | | Disables all programming modes. |

**Note:** Address bit A7 becomes "Don't Care" for the NM93C56.

## Timing Diagrams

### Synchronous Data Timing

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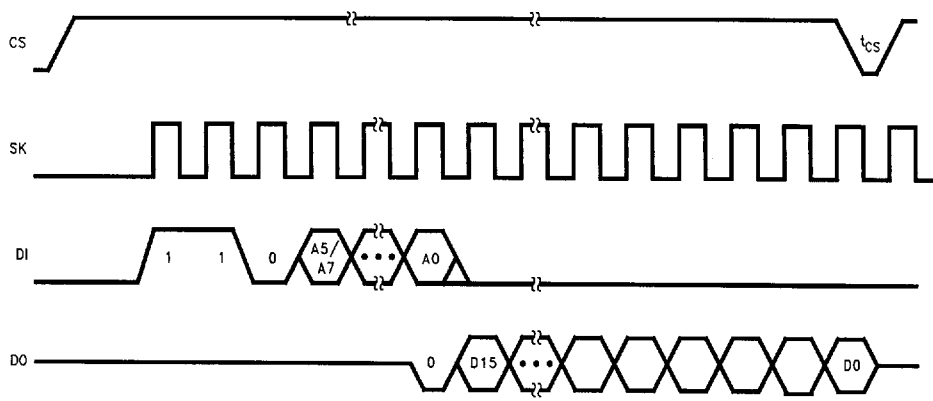
### READ

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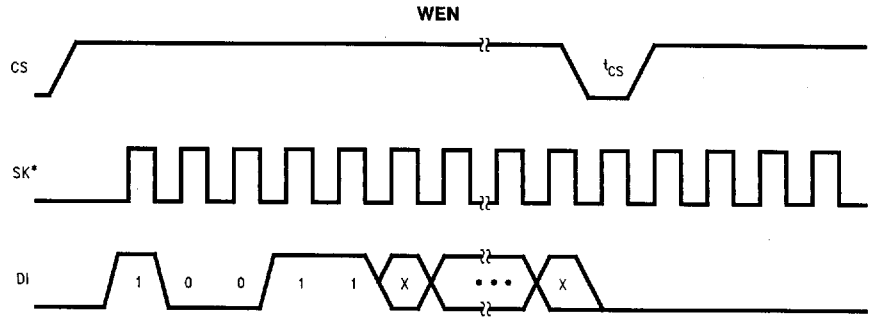
### WEN

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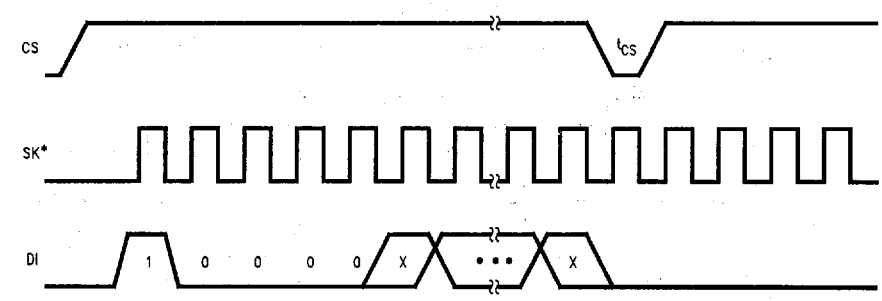
## Timing Diagrams (Continued)

**WDS:**

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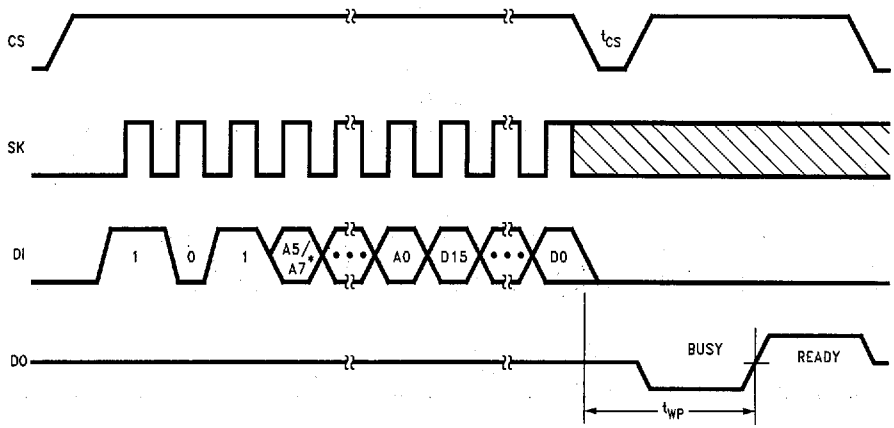
**WRITE:**

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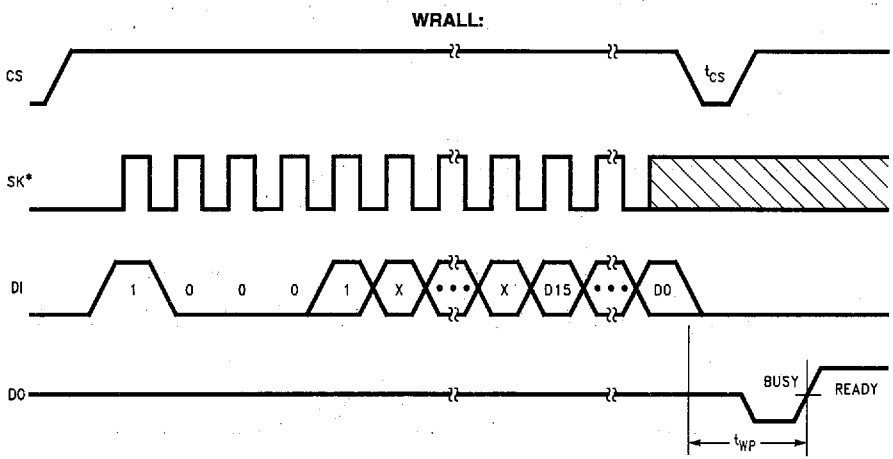
**WRALL:**

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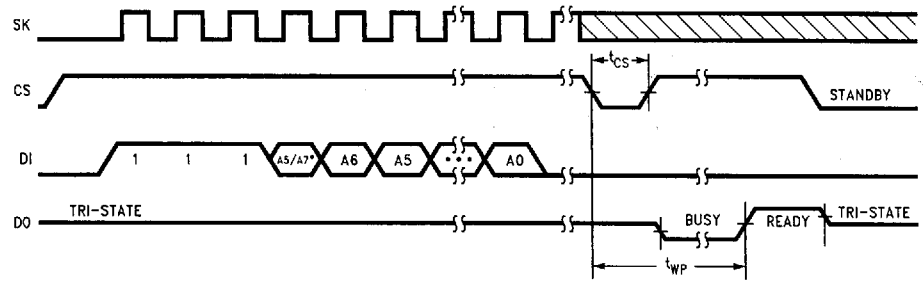
## Timing Diagrams (Continued)

**ERASE:**

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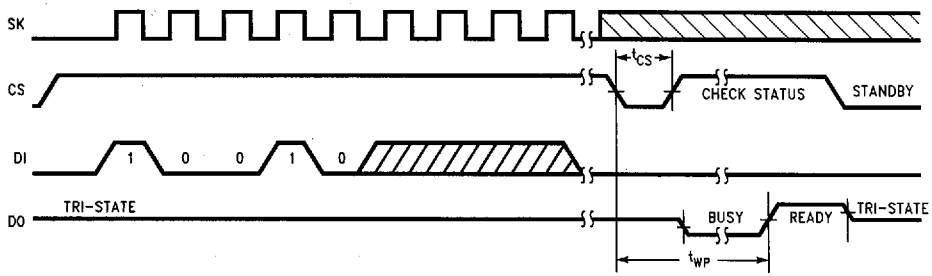
**ERAL:**

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## Functional Description (Continued)

**Mode 2: Master Reset**

**Sequence of Operation**

1. Input and Output Ready, HF and FULL can be in any state before the reset sequence with Master Reset ($\overline{MR}$) HIGH.
2. Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width $t_{MRW}$ before rising again.
3. Master Reset rises.
4. IR rises (if not HIGH already) to indicate ready to write state recovery time $t_{MRIRH}$ after the falling edge of $\overline{MR}$. Both HF and FULL will go LOW indicating an empty FIFO, occurring recovery times $t_{MRE}$ and $t_{MRO}$ respectively after the falling edge of $\overline{MR}$. OR falls recovery time $t_{MRORL}$ after $\overline{MR}$ falls. Data at outputs goes LOW recovery time $t_{MRONL}$ after $\overline{MR}$ goes LOW.
5. Shift-In can be taken HIGH after a minimum recovery time $t_{MRSIH}$ after $\overline{MR}$ goes HIGH.

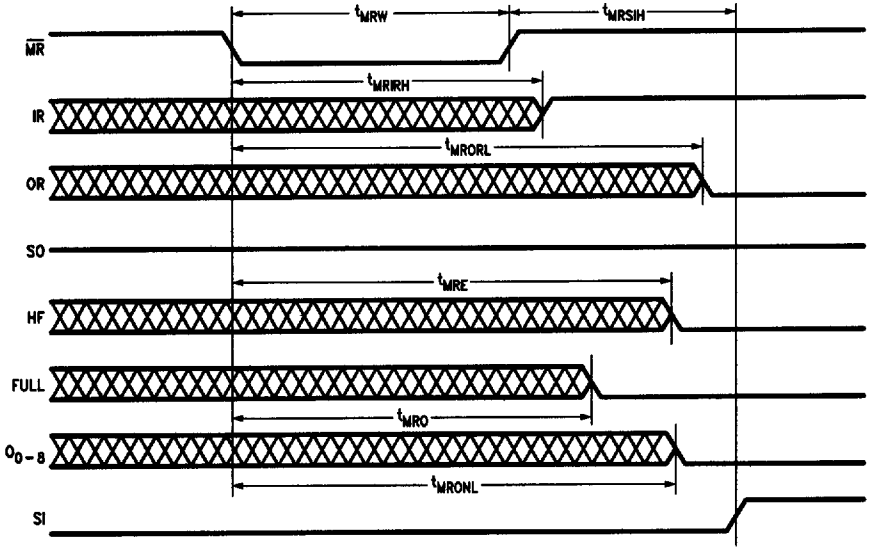


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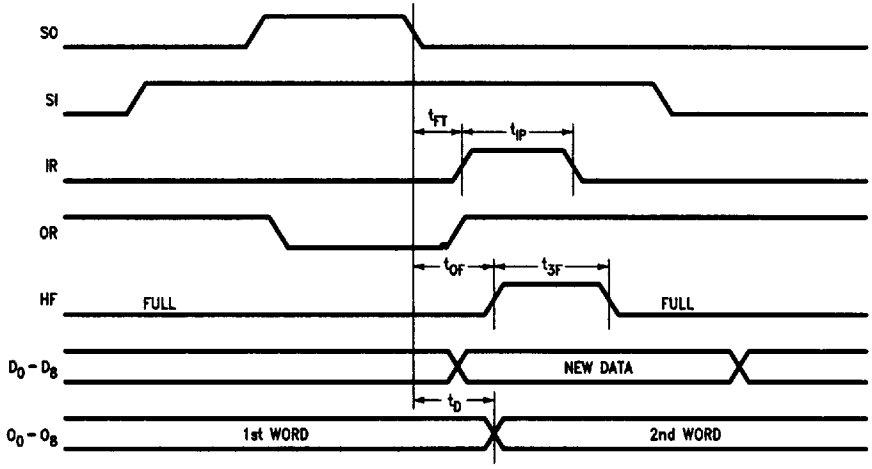
**FIGURE 2. Mode of Operation Mode 2**

## Functional Description (Continued)

**Mode 3: With FIFO Full, Shift-In is Held HIGH In Anticipation of an Empty Location**

**Sequence of Operation**

1. The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. Shift-Out is LOW. IR is LOW.
2. Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after propagation delay $t_D$. New data is written into the FIFO after SO goes LOW.
3. Input Ready goes HIGH one fall-through time, $t_{FT}$, after the falling edge of SO. Also, HF goes HIGH one $t_{OF}$ after SO falls, indicating that the FIFO is no longer full.
4. IR returns LOW pulse width $t_{IP}$ after rising and shifting new data in. Also, HF returns LOW pulse width $t_{3F}$ after rising, indicating the FIFO is once more full.
5. Shift-In is brought LOW to complete the shift-in process and maintain normal operation

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**Note:** $\overline{MR}$ and FULL are HIGH; $\overline{OE}$ is LOW.

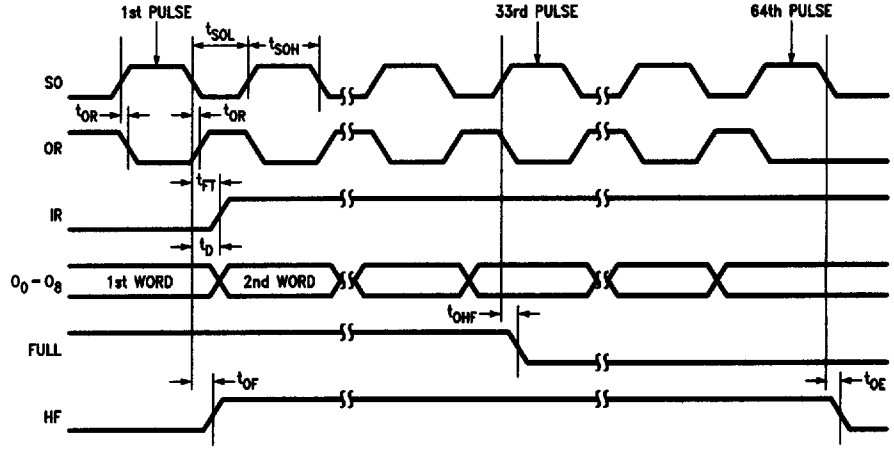
**FIGURE 3. Modes of Operation Mode 3**

## Functional Description (Continued)

**Mode 4: Shift-Out Sequence, FIFO Full to Empty**

**Sequence of Operation**

1. FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.
2. SO goes HIGH, resulting in OR going LOW one propagation delay, $t_{OR}$, after SO rises. OR LOW indicates output stage is busy.
3. SO goes LOW, new data reaches output one propagation delay, $t_D$, after SO falls; OR goes HIGH one propagation delay, $t_{OR}$, after SO falls and HF rises one propagation delay, $t_{OF}$, after SO falls. IR rises one fall-through time, $t_{FT}$, after SO falls.
4. Repeat process through the 64th SO pulse. FULL flag goes LOW one propagation delay, $t_{OHF}$, after the rising edge of 33rd SO, indicating that the FIFO is less than half full. On the falling edge of the 64th SO, HF goes LOW one propagation delay, $t_{OE}$, after SO, indicating the FIFO is empty. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.

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**Note:** SI and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH; $D_0$–$D_8$ are immaterial.

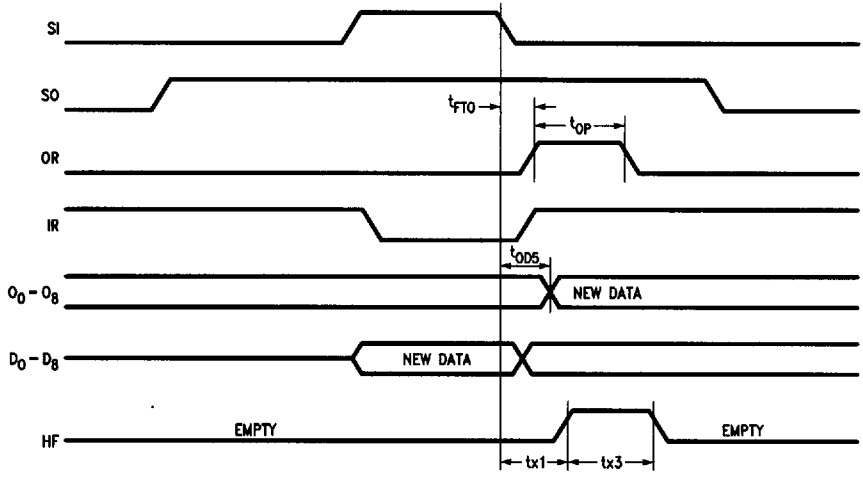
**FIGURE 4. Modes of Operation Mode 4**

## Functional Description (Continued)

**Mode 5: With FIFO Empty, Shift-Out is Held HIGH in Anticipation of Data**

**Sequence of Operation**

1. FIFO is initially empty; Shift-Out goes HIGH.
2. Shift-In pulse loads data into the FIFO and IR falls. HF rises propagation delay $t_{X1}$ after the falling edge of SI.
3. OR rises a fall-through time of $t_{FTO}$ after the falling edge of Shift-In, indicating that new data is ready to be output.
4. Data arrives at output one propagation delay, $t_{OD5}$, after the falling edge of Shift-In.
5. OR goes LOW pulse width $t_{OP}$ after rising and HF goes LOW pulse width $t_{X3}$ after rising, indicating that the FIFO is empty once more.
6. Shift-Out goes LOW, necessary to complete the Shift-Out process.

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**Note:** FULL is LOW; $\overline{MR}$ is HIGH; $\overline{OE}$ is LOW; $t_{DOF} = t_{FTO} - t_{OD5}$. Data output transition—valid data arrives at output stage $t_{DOF}$ after OR is HIGH.

**FIGURE 5. Modes of Operation Mode 5**