Table A–1. Maximum Ratings

Num	Rating	Symbol	Value	Unit
1	Supply Voltage[1,2]	V_{DD}	–0.3 to + 6.5	V
2	Input Voltage[1,2,3,4]	V_{in}	–0.3 to +6.5	V
3	Instantaneous Maximum Current Single pin limit (applies to all pins)[1,4,5,6]	I_D	25	mA
4	Operating Maximum Current Digital input disruptive current [4,5,6] $V_{SS} - 0.3 \le V_{IN} \le V_{DD} + 0.3$	I_{iD}	– 500 to +500	µA
5	Flash EEPROM Program/Erase Supply Voltage[7,8]	V_{FPE}	(V_{DD} – 0.35) to +12.6	V
6	Operating Temperature Range MC68F333 "C" Suffix	T_A	T_L to T_H –40 to +85	℃
7	Storage Temperature Range	T_{stg}	–55 to +150	℃

NOTES:

1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.
3. All functional non-supply pins are internally clamped to V_{SS}. All functional pins except EXTAL and XFC are internally clamped to V_{DD}.
4. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current condition.
5. This parameter is periodically sampled rather than 100% tested.
6. Total input current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.
7. V_{FPE} must not be raised to programming level while V_{DD} is below specified minimum value. V_{FPE} must not be reduced below minimum specified value while V_{DD} is applied.
8. Flash EEPROM modules can be damaged by power-on and power-off V_{FPE} transients. Maximum power-on overshoot tolerance is 13.5 V for periods of less than 30 ns.

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Table A–2. Typical Ratings

Num	Rating	Symbol	Value	Unit
1	Supply Voltage	V_{DD}	5.0	V
2	Operating Temperature	T_A	25	°C
3	V_{DD} Supply Current RUN LPSTOP, VCO Off LPSTOP, External clock, max f_{sys}	I_{DD}	 90 125 3	 mA µA µA
4	Clock Synthesizer Operating Voltage	V_{DDSYN}	5.0	V
5	V_{DDSYN} Supply Current VCO on, maximum f_{sys} External Clock, maximum f_{sys} LPSTOP, VCO off V_{DD} powered down	I_{DDSYN}	 1.0 4.0 250 50	 mA mA µA µA
6	RAM Standby Voltage	V_{SB}	3.0	V
7	RAM Standby Current Normal RAM operation Standby operation	I_{SB}	 7.0 40	 µA µA
8	Power Dissipation	P_D	455	mW

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Table A–3. Thermal Characteristics

Num	Characteristic	Symbol	Value	Unit
1	Thermal Resistance Plastic 160-Pin Surface Mount	Θ_{JA}	37	°C/W

The average chip-junction temperature (T_J) in C can be obtained from:

$$T_J = T_A + (P_D \Theta_{JA}) \quad (1)$$

where

T_A = Ambient Temperature, °C

Θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{DD} \times V_{DD}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D + (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

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Table A–4. Clock Control Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, 4.194-MHz reference)

Num	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range	f_{ref}	25	50	kHz
2	System Frequency[1]		dc	16.78	
	On-Chip PLL Frequency	f_{sys}	0.131	16.78	MHz
	External Clock Operation		dc	16.78	
3	PLL Startup Time[2,3,4,5]	t_{spll}	—	50	ms
4	PLL Lock Time[2,4,5,6]	t_{lpll}	—	20	ms
5	Limp Mode Clock Frequency[7]	f_{limp}			MHz
	SYNCR X Bit = 0		—	f_{sys} max /2	
	SYNCR X Bit = 1		—	f_{sys} max	
6	CLKOUT Stability[2,4,5,8]				
	Short term (5 µs interval)	C_{stab}	–0.5	0.5	%
	Long term (500 µs interval)		–0.05	0.05	

NOTES:

1. All internal registers retain data at 0 Hz.
2. This parameter is periodically sampled rather than 100% tested.
3. Parameter measured from the time V_{DD} and V_{DDSYN} are valid to $\overline{\text{RESET}}$ release.
4. Assumes that an external filter capacitor with a value of 0.1 µF and an insulation resistance greater than 30,000 MΩ is attached to the XFC pin. Total external resistance from the XFC pin due to external leakage sources must be greater than 10 MΩ to guarantee this specification.
5. Proper layout procedures must be followed to achieve specifications.
6. Assumes that stable V_{DDSYN} is applied, and that the crystal oscillator is stable. Lock time is measured from the time V_{DD} and V_{DDSYN} are valid to $\overline{\text{RESET}}$ release. This specification also applies to the period required for PLL lock after changing the W and Y frequency control bits in the synthesizer control register (SYNCR) while the PLL is running, and to the period required for the clock to lock after LPSTOP.
7. Determined by the initial control voltage applied to the on-chip VCO. The X bit in SYNCR controls a divide by two scaler on the system clock output.
8. Stability is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SS} and variation in crystal oscillator frequency increase the C_{stab} percentage for a given interval.

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Table A–5. DC Characteristics

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
1	Input High Voltage	V_{IH}	0.7 (V_{DD})	V_{DD} + 0.3	V
2	Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.2 (V_{DD})	V
3	Input Hysteresis[1,9]	V_{HYS}	0.5	—	V
4	Input Leakage Current[2] V_{in} = V_{DD} or V_{SS} All input-only pins except ADC pins	I_{in}	–2.5	2.5	µA
5	High Impedance (Off-State) Leakage Current[2] V_{in} = V_{DD} or V_{SS} All input/output and output pins	I_{OZ}	–2.5	2.5	µA
6	CMOS Output High Voltage[2,3] I_{OH} = –10.0 µA Group 1,2,4 input/output and all output pins	V_{OH}	V_{DD} – 0.2	—	V
7	CMOS Output Low Voltage[2] I_{OL} = 10.0 µA Group 1,2,4 input/output and all output pins	V_{OL}	—	0.2	V
8	Output High Voltage [2,3] I_{OH} = –0.8 mA Group 1,2,4 input/output and all output pins	V_{OH}	V_{DD} – 0.8	—	V
9	Output Low Voltage[2] I_{OL} = 1.6 mA Group 1 I/O Pins, CLKOUT, FREEZE/QUOT, IPIPE I_{OL} = 5.3 mA Group 2 and Group 4 I/O Pins, CSBOOT, BG/CS I_{OL} = 12 mA Group 3	V_{OL}	— — —	0.4 0.4 0.4	V
10	Data Bus Mode Select Pull-up Current[5] V_{in} = V_{IL} DATA[15:0] V_{in} = V_{IH} DATA[15:0]	I_{MSP}	— –15	–120 —	µA
11	V_{DD} Supply Current[6] RUN[4] RUN, TPU emulation mode RUN, Single-Chip Mode LPSTOP, 32.768-kHz crystal, VCO Off (STSCIM = 0) LPSTOP (External clock input frequency = maximum f_{sys})	I_{DD}	— — — — —	160 170 150 350 5	mA mA mA µA mA
12	Clock Synthesizer Operating Voltage	V_{DDSYN}	4.5	5.5	V
13	V_{DDSYN} Supply Current[6] 32.768-kHz crystal, VCO on, maximum f_{sys} External Clock, maximum f_{sys} LPSTOP, 32.768-kHz crystal, VCO off (STSCIM = 0) 32.768-kHz crystal, V_{DD} powered down	I_{DDSYN}	— — — —	1 5 150 100	mA mA µA µA
14	RAM Standby Voltage[7] Specified V_{DD} applied V_{DD} = V_{SS}	V_{SB}	0.0 3.0	5.5 5.5	V
15	RAM Standby Current[6] Normal RAM operation[10] $V_{DD} > V_{SB} – 0.5$ V Transient condition $V_{SB} – 0.5$ V ≥ V_{DD} ≥ V_{SS} + 0.5 V Standby operation[7] $V_{DD} < V_{SS}$ + 0.5 V	I_{SB}	— — —	TBD 5 100	µA mA µA
16	Power Dissipation[8]	P_D	—	880	mW
17	Input Capacitance[2,9] All input-only pins except ADC pins All input/output pins	C_{in}	— —	10 20	pF
18	Load Capacitance[2] Group 1 I/O Pins and CLKOUT, FREEZE/QUOT, IPIPE Group 2 I/O Pins and CSBOOT, BG/CS Group 3 I/O pins Group 4 I/O pins	C_L	— — — —	90 100 130 200	pF

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Table A–5. DC Characteristics (Continued)

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

NOTES:

1. Parameter applies to the following pins:
   Port ADA: PADA[7:0]/AN[7:0]
   Port A: PA[7:0]/ADDR[18:11]
   Port B: PB[7:0]/ADDR[10:3]
   Port E: PE[7:6]/SIZ[1:0], PE5/$\overline{AS}$, PE4/$\overline{DS}$, PE3
   Port F: PF[7:1]/IRQ[7:1], PF0/MODCLK
   Port G: PG[7:0]/DATA[15:8]
   Port H: PH[7:0]/DATA[7:0]
   Port QS: PQS7/TXD, PQS[6:4]/PCS[3:1], PQS3/PCS0/$\overline{SS}$, PQS2/SCK, PQS1/MOSI, PQS0/MISO
   Other: $\overline{BKPT}$/DSCLK, PAI, PCLK, $\overline{RESET}$, T2CLK, TPUCH[15:0], TSC
2. Input-Only Pins: $\overline{BKPT}$/DSCLK, EXTAL, PAI, PCLK, TSC
   Output-Only Pins: ADDR[2:0], $\overline{CSBOOT}$, $\overline{BG}$/$\overline{CS1}$, CLKOUT, FREEZE/QUOT, DSO/$\overline{IPIPE}$, PWMA, PWMB
   Input/Output Pins:
   Group 1: Port G: PG[7:0]/DATA[15:8]
   Port H: PH[7:0]/DATA[7:0]
   Other: DSI/$\overline{IFETCH}$, TPUCH[15:0]
   Group 2: Port A: PA[7:0]/ADDR[18:11]
   Port B: PB[7:0]/ADDR[10:3]
   Port C: PC[6:3]/ADDR[22:19]/$\overline{CS}$[9:6], PC2/FC2/$\overline{CS5}$,PC1/FC1, PC0/FC0/$\overline{CS3}$
   Port E: PE[7:6]/SIZ[1:0], PE5/$\overline{AS}$, PE4/$\overline{DS}$, PE3
   Port F: PF[7:1]/IRQ[7:1], PF0/MODCLK
   Port QS: PQS7/TXD, PQS[6:4]/PCS[3:1], PQS3/PCS0/$\overline{SS}$
   Other: ADDR23/$\overline{CS10}$/ECLK, R/$\overline{W}$, $\overline{BERR}$, $\overline{BR}$/$\overline{CS0}$, $\overline{BGACK}$/$\overline{CS2}$
   Group 3: $\overline{HALT}$, $\overline{RESET}$
   Group 4: Port QS: PQS2/SCK, PQS1/MOSI, PQS0/MISO
3. Does not apply to $\overline{HALT}$, $\overline{RESET}$ (open-drain pins), and port QS in wired-OR mode.
4. Current measured with system clock frequency of 16.78 MHz, all modules active.
5. Use of an active pulldown device is recommended.
6. Total operating current is the sum of the appropriate I_{DD}, I_{DDSYN}, and I_{SB} values, plus I_{DDA}. I_{DD} values include supply currents for device modules powered by V_{DDE} and V_{DDI} pins.
7. RAM modules cannot switch into standby mode as long as V_{SB} does not exceed V_{DD} by more than 0.5 Volt. RAM arrays cannot be accessed while the module is in standby mode.
8. Power dissipation measured with system clock frequency of 16.78 MHz, all modules active. Specification does not apply to TPU emulation mode. Power dissipation can be calculated using the expression:

$$P_D = \text{Maximum } V_{DD}\,(I_{DD} + I_{DDSYN} + I_{SB}) + \text{Maximum } V_{DDA}\,(I_{DDA})$$

   I_{DD} includes supply currents for all device modules powered by V_{DDE} and V_{DDI} pins.
9. This parameter is periodically sampled rather than 100% tested.
10. When V_{SB} is more than 0.3 V greater than V_{DD}, current flows between the V_{STBY} and V_{DD} pins, which causes standby current to increase toward the maximum transient condition specification. System noise on the V_{DD} and V_{STBY} pin can contribute to this condition.

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Table A–6. AC Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
F1	Frequency of Operation (32.768 kHz crystal)[2]	f	0.13	16.78	MHz
1	Clock Period	t_{cyc}	59.6	—	ns
1A	ECLK Period	t_{Ecyc}	476	—	ns
1B	External Clock Input Period[3]	t_{Xcyc}	59.6	—	ns
2, 3	Clock Pulse Width	t_{CW}	24	—	ns
2A, 3A	ECLK Pulse Width	t_{ECW}	236	—	ns
2B, 3B	External Clock Input High/Low Time[3]	t_{XCHL}	29.8	—	ns
4, 5	Clock Rise and Fall Time	t_{Crf}	—	5	ns
4A, 5A	Rise and Fall Time — All Outputs except CLKOUT	t_{rf}	—	8	ns
4B, 5B	External Clock Rise and Fall Time[4]	t_{XCrf}	—	5	ns
6	Clock High to ADDR, FC, SIZE, $\overline{RMC}$ Valid	t_{CHAV}	0	29	ns
7	Clock High to ADDR, DATA, FC, SIZE, $\overline{RMC}$ High Impedance	t_{CHAZx}	0	59	ns
8	Clock High to ADDR, FC, SIZE, $\overline{RMC}$ Invalid	t_{CHAZn}	0	—	ns
9	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Asserted	t_{CLSA}	2	25	ns
9A	$\overline{AS}$ to $\overline{DS}$ or $\overline{CS}$ Asserted (Read)[5]	t_{STSA}	–15	15	ns
9C	Clock Low to $\overline{IFETCH}$, $\overline{IPIPE}$ Asserted	t_{CLIA}	2	22	ns
11	ADDR, FC, SIZE, $\overline{RMC}$ Valid to $\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Asserted	t_{AVSA}	15	—	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated	t_{CLSN}	2	29	ns
12A	Clock Low to $\overline{IFETCH}$, $\overline{IPIPE}$ Negated	t_{CLIN}	2	22	ns
13	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated to ADDR, FC, SIZE Invalid (Address Hold)	t_{SNAI}	15	—	ns
14	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Width Asserted	t_{SWA}	100	—	ns
14A	$\overline{DS}$, $\overline{CS}$ Width Asserted (Write)	t_{SWAW}	45	—	ns
14B	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Width Asserted (Fast Write Cycle)	t_{SWDW}	40	—	ns
15	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Width Negated[6]	t_{SN}	40	—	ns
16	Clock High to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ High Impedance	t_{CHSZ}	—	59	ns
17	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Negated to R/$\overline{W}$ High	t_{SNRN}	15	—	ns
18	Clock High to R/$\overline{W}$ High	t_{CHRH}	0	29	ns
20	Clock High to R/$\overline{W}$ Low	t_{CHRL}	0	29	ns
21	R/$\overline{W}$ High to $\overline{AS}$, $\overline{CS}$ Asserted	t_{RAAA}	15	—	ns
22	R/$\overline{W}$ Low to $\overline{DS}$, $\overline{CS}$ Asserted (Write)	t_{RASA}	70	—	ns
23	Clock High to Data Out Valid	t_{CHDO}	—	29	ns
24	Data Out Valid to Negating Edge of $\overline{AS}$, $\overline{CS}$ (Fast Write Cycle)	t_{DVASN}	15	—	ns

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Table A–6. AC Timing (Continued)

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
25	$\overline{DS}$, $\overline{CS}$ Negated to Data Out Invalid (Data Out Hold)	t_{SNDOI}	15	—	ns
26	Data Out Valid to $\overline{DS}$, $\overline{CS}$ Asserted (Write)	t_{DVSA}	15	—	ns
27	Data In Valid to Clock Low (Data Setup)	t_{DICL}	5	—	ns
27A	Late $\overline{BERR}$, $\overline{HALT}$ Asserted to Clock Low (Setup Time)	t_{BELCL}	20	—	ns
28	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DSACK[1:0]}$, $\overline{BERR}$, $\overline{HALT}$, $\overline{AVEC}$ Negated	t_{SNDN}	0	80	ns
29	$\overline{DS}$, $\overline{CS}$ Negated to Data In Invalid (Data In Hold)[7]	t_{SNDI}	0	—	ns
29A	$\overline{DS}$, $\overline{CS}$ Negated to Data In High Impedance[7,8]	t_{SHDI}	—	55	ns
30	CLKOUT Low to Data In Invalid (Fast Cycle Hold)[7]	t_{CLDI}	15	—	ns
30A	CLKOUT Low to Data In High Impedance[7]	t_{CLDH}	—	90	ns
31	$\overline{DSACK[1:0]}$ Asserted to Data In Valid[9]	t_{DADI}	—	50	ns
33	Clock Low to $\overline{BG}$ Asserted/Negated	t_{CLBAN}	—	29	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted ($\overline{RMC}$ Not Asserted)[10]	t_{BRAGA}	1	—	t_{cyc}
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GAGN}	1	2	t_{cyc}
39	$\overline{BG}$ Width Negated	t_{GH}	2	—	t_{cyc}
39A	$\overline{BG}$ Width Asserted	t_{GA}	1	—	t_{cyc}
46	R/$\overline{W}$ Width Asserted (Write or Read)	t_{RWA}	150	—	ns
46A	R/$\overline{W}$ Width Asserted (Fast Write or Read Cycle)	t_{RWAS}	90	—	ns
47A	Asynchronous Input Setup Time $\overline{BR}$, $\overline{BGACK}$, $\overline{DSACK[1:0]}$, $\overline{BERR}$, $\overline{AVEC}$, $\overline{HALT}$	t_{AIST}	5	—	ns
47B	Asynchronous Input Hold Time	t_{AIHT}	15	—	ns
48	$\overline{DSACK[1:0]}$ Asserted to $\overline{BERR}$, $\overline{HALT}$ Asserted[11]	t_{DABA}	—	30	ns
53	Data Out Hold from Clock High	t_{DOCH}	0	—	ns
54	Clock High to Data Out High Impedance	t_{CHDH}	—	28	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RADC}	40	—	ns
56	$\overline{RESET}$ Pulse Width (Reset Instruction)	t_{HRPW}	512	—	t_{cyc}
57	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	t_{BNHN}	0	—	ns
70	Clock Low to Data Bus Driven (Show)	t_{SCLDD}	0	29	ns
71	Data Setup Time to Clock Low (Show)	t_{SCLDS}	15	—	ns
72	Data Hold from Clock Low (Show)	t_{SCLDH}	10	—	ns
73	$\overline{BKPT}$ Input Setup Time	t_{BKST}	15	—	ns
74	$\overline{BKPT}$ Input Hold Time	t_{BKHT}	10	—	ns
75	Mode Select Setup Time	t_{MSS}	20	—	t_{cyc}
76	Mode Select Hold Time	t_{MSH}	0	—	ns
77	$\overline{RESET}$ Assertion Time[12]	t_{RSTA}	4	—	t_{cyc}
78	$\overline{RESET}$ Rise Time[12,13]	t_{RSTR}	—	10	t_{cyc}

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Table A–6. AC Timing (Continued)

(V_{DD} and V_{DDSYN} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. Minimum system clock frequency is four times the crystal frequency, subject to specified limits.
3. When an external clock is used, minimum high and low times are based on a 50% duty cycle. The minimum allowable t_{Xcyc} period is reduced when the duty cycle of the external clock signal varies. The relationship between external clock input duty cycle and minimum t_{Xcyc} is expressed:

   Minimum t_{Xcyc} period = minimum t_{XCHL} / (50% – external clock input duty cycle tolerance).
4. Parameters for an external clock signal applied while the internal PLL is disabled (MODCLK pin held low during reset). Does not pertain to an external VCO reference applied while the PLL is enabled (MODCLK pin held high during reset). When the PLL is enabled, the clock synthesizer detects successive transitions of the reference signal — if transitions occur within the correct clock period, rise/fall times and duty cycle are not critical.
5. Specification 9A is the worst-case skew between $\overline{AS}$ and $\overline{DS}$ or $\overline{CS}$. The amount of skew depends on the relative loading of these signals. When loads are kept within specified limits, skew will not cause $\overline{AS}$ and $\overline{DS}$ to fall outside the limits shown in specification 9.
6. If multiple chip selects are used, $\overline{CS}$ width negated (specification 15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select. The $\overline{CS}$ width negated specification between multiple chip selects does not apply to chip selects being used for synchronous ECLK cycles.
7. Hold times are specified with respect to $\overline{DS}$ or $\overline{CS}$ on asynchronous reads and with respect to CLKOUT on fast cycle reads. The user is free to use either hold time.
8. Maximum value is equal to (t_{cyc} / 2) + 25 ns.
9. If the asynchronous setup time (specification 47A) requirements are satisfied, the $\overline{DSACK[1:0]}$ low to data setup time (specification 31) and $\overline{DSACK[1:0]}$ low to $\overline{BERR}$ low setup time (specification 48) can be ignored. The data must only satisfy the data-in to clock low setup time (specification 27) for the following clock cycle. $\overline{BERR}$ must satisfy only the late $\overline{BERR}$ low to clock low setup time (specification 27A) for the following clock cycle.
10. To ensure coherency during every operand transfer, $\overline{BG}$ is not asserted in response to $\overline{BR}$ until after all cycles of the current operand transfer are complete and $\overline{RMC}$ is asserted.
11. In the absence of $\overline{DSACK[1:0]}$, $\overline{BERR}$ is an asynchronous input using the asynchronous setup time (specification 47A).
12. After external $\overline{RESET}$ negation is detected, a short transition period (approximately 2 t_{cyc}) elapses, then the SCIM drives $\overline{RESET}$ low for 512 t_{cyc}.
13. External logic must pull $\overline{RESET}$ high during this period in order for normal MCU operation to begin.
14. Address access time = (2.5 + WS) $t_{cyc} - t_{CHAV} - t_{DICL}$
    Chip select access time = (2 + WS) $t_{cyc} - t_{CLSA} - t_{DICL}$
    Where: WS = number of wait states. When fast termination is used (2 clock bus) WS = –1.

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Table A–7. Background Debugging Mode Timing

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
B0	DSI Input Setup Time	t_{DSISU}	15	—	ns
B1	DSI Input Hold Time	t_{DSIH}	10	—	ns
B2	DSCLK Setup Time	t_{DSCSU}	15	—	ns
B3	DSCLK Hold Time	t_{DSCH}	10	—	ns
B4	DSO Delay Time	t_{DSOD}	—	25	ns
B5	DSCLK Cycle Time	t_{DSCCYC}	2	—	t_{cyc}
B6	CLKOUT High to FREEZE Asserted/Negated	t_{FRZAN}	—	50	ns
B7	CLKOUT High to $\overline{\text{IFETCH}}$ High Impedance	t_{IFZ}	—	50	ns
B8	CLKOUT High to $\overline{\text{IFETCH}}$ Valid	t_{IF}	—	50	ns
B9	DSCLK Low Time	t_{DSCLO}	1	—	t_{cyc}

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.

Table A–8. ECLK Bus Timing

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
E1	ECLK Low to Address Valid[2]	t_{EAD}	—	60	ns
E2	ECLK Low to Address Hold	t_{EAH}	10	—	ns
E3	ECLK Low to $\overline{\text{CS}}$ Valid ($\overline{\text{CS}}$ Delay)	t_{ECSD}	—	150	ns
E4	ECLK Low to $\overline{\text{CS}}$ Hold	t_{ECSH}	15	—	ns
E5	$\overline{\text{CS}}$ Negated Width	t_{ECSN}	30	—	ns
E6	Read Data Setup Time	t_{EDSR}	30	—	ns
E7	Read Data Hold Time	t_{EDHR}	15	—	ns
E8	ECLK Low to Data High Impedance	t_{EDHZ}	—	60	ns
E9	$\overline{\text{CS}}$ Negated to Data Hold (Read)	t_{ECDH}	0	—	ns
E10	$\overline{\text{CS}}$ Negated to Data High Impedance	t_{ECDZ}	—	1	t_{cyc}
E11	ECLK Low to Data Valid (Write)	t_{EDDW}	—	2	t_{cyc}
E12	ECLK Low to Data Hold (Write)	t_{EDHW}	5	—	ns
E13	$\overline{\text{CS}}$ Negated to Data Hold (Write)	t_{ECHW}	0	—	ns
E14	Address Access Time (Read)[3]	t_{EACC}	386	—	ns
E15	Chip Select Access Time (Read)[4]	t_{EACS}	296	—	ns
E16	Address Setup Time	t_{EAS}	—	1/2	t_{cyc}

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. When previous bus cycle is not an ECLK cycle, the address may be valid before ECLK goes low.
3. Address access time = $t_{Ecyc} - t_{EAD} - t_{EDSR}$
4. Chip select access time = $t_{Ecyc} - t_{ECSD} - t_{EDSR}$

A

Table A–9. QSPI Timing

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, 200 pF load on all QSPI pins)

Num	Characteristic	Symbol	Min	Max	Unit
0	Operating Frequency Master Slave	f_{op}	 DC DC	 1/4 1/4	 System Clock Frequency System Clock Frequency
1	Cycle Time Master Slave	t_{qcyc}	 4 4	 510 —	 t_{cyc} t_{cyc}
2	Enable Lead Time Master Slave	t_{lead}	 2 2	 128 —	 t_{cyc} t_{cyc}
3	Enable Lag Time Master Slave	t_{lag}	 — 2	 1/2 —	 SCK t_{cyc}
4	Clock (SCK) High or Low Time Master Slave[2]	t_{sw}	 2 t_{cyc} – 60 2 t_{cyc} – n	 255 t_{cyc} —	 ns ns
5	Sequential Transfer Delay Master Slave (Does Not Require Deselect)	t_{td}	 17 13	 8192 —	 t_{cyc} t_{cyc}
6	Data Setup Time (Inputs) Master Slave	t_{su}	 30 20	 — —	 ns ns
7	Data Hold Time (Inputs) Master Slave	t_{hi}	 0 20	 — —	 ns ns
8	Slave Access Time	t_a	—	1	t_{cyc}
9	Slave MISO Disable Time	t_{dis}	—	2	t_{cyc}
10	Data Valid (after SCK Edge) Master Slave	t_v	 — —	 50 50	 ns ns
11	Data Hold Time (Outputs) Master Slave	t_{ho}	 0 0	 — —	 ns ns
12	Rise Time Input Output	 t_{ri} t_{ro}	 — —	 2 30	 µs ns
13	Fall Time Input Output	 t_{fi} t_{fo}	 — —	 2 30	 µs ns

NOTES:

1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.
2. For high time, n = External SCK rise; for low time, n = External SCK fall time.

A

Table A–10. ADC Maximum Ratings

Num	Characteristic	Symbol	Min	Max	Unit
1	Analog Supply	V_{DDA}	– 0.3	6.5	V
2	Internal Digital Supply	V_{DDI}	– 0.3	6.5	V
3	Reference Supply	V_{RH}, V_{RL}	– 0.3	6.5	V
4	V_{SS} Differential Voltage	$V_{SSI} - V_{SSA}$	– 0.1	0.1	V
5	V_{DD} Differential Voltage	$V_{DDI} - V_{DDA}$	– 6.5	6.5	V
6	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	– 6.5	6.5	V
7	V_{REF} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	– 6.5	6.5	V
8	Disruptive Input Current[1, 2, 3, 4, 5, 6] $V_{NEGCLAMP} \cong -0.3$ V $V_{POSCLAMP} \cong V_{DDA} + 2$	I_{NA}	– 44	44	µA
9	Maximum Input Current [3, 4, 6] $V_{NEGCLAMP} \cong -0.3$ V $V_{POSCLAMP} \cong V_{DDA} + 2$	I_{MA}	– 500	500	µA

NOTES:

1. Below disruptive current conditions, the channel being stressed will have conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.
2. Input signals with large slew rates or high frequency noise components cannot be converted accurately. These signals also interfere with conversion of other channels.
3. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
4. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using positive and negative clamp values, then use the larger of the calculated values.
5. This parameter is periodically sampled rather than 100% tested.
6. Applies to single pin only.

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Table A–11. ADC DC Electrical Characteristics (Operating)

(V_{SS} = 0 Vdc, ADCLK = 2.1 MHz, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
1	Analog Supply[1]	V_{DDA}	4.5	5.5	V
2	Internal Digital Supply[1]	V_{DDI}	4.5	5.5	V
3	V_{SS} Differential Voltage	$V_{SSI} - V_{SSA}$	– 1.0	1.0	mV
4	V_{DD} Differential Voltage	$V_{DDI} - V_{DDA}$	– 1.0	1.0	V
5	Reference Voltage Low[2,5]	V_{RL}	V_{SSA}	V_{DDA} / 2	V
6	Reference Voltage High[2,5]	V_{RH}	V_{DDA} / 2	V_{DDA}	V
7	V_{REF} Differential Voltage[5]	$V_{RH} - V_{RL}$	4.5	5.5	V
8	Input Voltage[2]	V_{INDC}	V_{SSA}	V_{DDA}	V
9	Input High, Port ADA	V_{IH}	0.7 (V_{DDA})	V_{DDA} + 0.3	V
10	Input Low, Port ADA	V_{IL}	V_{SSA} – 0.3	0.2 (V_{DDA})	V
15	Analog Supply Current Normal Operation[3] Low-Power Stop	I_{DDA}	 — —	 1.0 200	 mA µA
16	Reference Supply Current	I_{REF}	—	250	µA
17	Input Current, Off Channel[4]	I_{OFF}	—	150	nA
18	Total Input Capacitance, Not Sampling	C_{INN}	—	10	pF
19	Total Input Capacitance, Sampling	C_{INS}	—	15	pF

NOTES:

1. Refers to operation over full temperature and frequency range.
2. To obtain full-scale, full-range results, $V_{SSA} \le V_{RL} \le V_{INDC} \le V_{RH} \le V_{DDA}$.
3. Current measured at maximum system clock frequency with ADC active.
4. Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each 10° C decrease from maximum temperature.
5. Accuracy tested and guaranteed at $V_{RH} - V_{RL} \le 5.0$ V ± 10%.

Table A–12. ADC AC Characteristics (Operating)

(V_{DD} and V_{DDA} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

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Num	Characteristic	Symbol	Min	Max	Unit
1	On-Chip PLL Frequency	f_{sys}	2.0	16.78	MHz
2	ADC Clock Frequency	F_{ADCLK}	0.5	2.1	MHz
3	8-Bit Conversion Time (16 ADC Clocks)[1]	T_{CONV}	7.62	—	µs
4	10-Bit Conversion Time (18 ADC Clocks)[1]	T_{CONV}	8.58	—	µs
5	Stop Recovery Time	T_{SR}	—	10	µs

NOTES:

1. Assumes 2.1-MHz ADC clock and selection of minimum sample time (2 ADC clocks).

Table A–13. ADC Conversion Characteristics (Operating)

(V_{DD} and V_{DDA} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, ADCLK = 2.1 MHz)

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	8-Bit Resolution[1]	1 Count	—	20	—	mV
2	8-Bit Differential Nonlinearity	DNL	–0.5	—	0.5	Counts
3	8-Bit Integral Nonlinearity	INL	–1	—	1	Counts
4	8-Bit Absolute Error[2]	AE	–1	—	1	Counts
5	10-Bit Resolution[1]	1 Count	—	5	—	mV
6	10-Bit Differential Nonlinearity	DNL	–0.5	—	0.5	Counts
7	10-Bit Integral Nonlinearity	INL	–2.0	—	2.0	Counts
8	10-Bit Absolute Error[3]	AE	–2.5	—	2.5	Counts
9	Source Impedance at Input[4]	R_S	—	20	—	kΩ

NOTES:

1. At $V_{RH} - V_{RL}$ = 5.12 V, one 10-bit count = 5 mV and one 8-bit count = 20 mV.
2. 8-bit absolute error of 1 count (20 mV) includes 1/2 count (10 mV) inherent quantization error and 1/2 count (10 mV) circuit (differential, integral, and offset) error.
3. 10-bit absolute error of 2.5 counts (12.5 mV) includes 1/2 count (2.5 mV) inherent quantization error and 2 counts (10 mV) circuit (differential, integral, and offset) error.
4. Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on leakage due to charge-sharing with internal capacitance.

   Error from junction leakage is a function of external source impedance and input leakage current. In the following expression, expected error in result value due to junction leakage is expressed in voltage (V_{errj}).

   $$V_{errj} = R_S \times I_{OFF}$$

   where I_{OFF} is a function of operating temperature. (See Table A–11, note 4).

   Charge-sharing leakage is a function of input source impedance, conversion rate, change in voltage between successive conversions, and the size of the decoupling capacitor used. Error levels are best determined empirically. In general, continuous conversion of the same channel may not be compatible with high source impedance.

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Table A–14. Flash EEPROM Specifications

(V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, specified f_{sys}, $T_A = T_L$ to T_H)

Num	Characteristic	Symbol	Min	Max	Unit
1	Program/Erase supply voltage[1] Read operation Program/Erase/Verify operation	V_{FPE}	 V_{DD} – 0.35 11.4	 5.5 12.6	V
2	Program/Erase/Verify supply current[2] Read operation Program/Erase/Verify operation Verify (ENPE = 0) Program byte (ENPE = 1) Program word (ENPE = 1) Erase (ENPE = 1)	I_{FPE}	 — — — — —	 15 50 15 30 4	 µa µa ma ma ma
3	Program recovery time	t_{pr}	—	10	µs
4	Program pulse width	pw_{pp}	20	25	µs
5	Number of program pulses[3]	n_{pp}	—	50	—
6	Program margin[4]	p_m	100	—	%
7	Number of erase pulses[3]	n_{ep}	—	2	—
8	Erase pulse time	t_{epk}	—	$t_{ei} \bullet k$	ms
9	Amount to increment t_{ep}	t_{ei}	90	110	ms
10	Erase margin	e_m	—	$\sum_{k=1}^{n_{ep}} t_{ei} \bullet k$	ms
11	Erase recovery time	t_{er}	—	1	ms
12	Low-power stop recovery time[5]	t_{sb}	—	1	µs

NOTES:

1. V_{FPE} must not be raised to programming voltage while V_{DD} is below specified minimum value. V_{FPE} must not be reduced below minimum specified value while V_{DD} is applied.
2. Current parameters apply to each individual EEPROM module.
3. Without margin.
4. At 100% margin, the number of margin pulses required is the same as the number of pulses used to program the byte or word.
5. Parameter measured from end of write cycle that clears STOP bit in FEEMCR.

A

Table A–15. Flash EEPROM Life

Num	Parameter	Symbol	Value	Unit
1	Program-erase endurance[1]	e_{pe}	100	cyc
2	Data retention[2]	r_d	10	yr

NOTES:

1. Number of program-erase cycles (1 to 0, 0 to 1) per bit.
2. Parameter based on accelerated-life testing with standard test pattern.

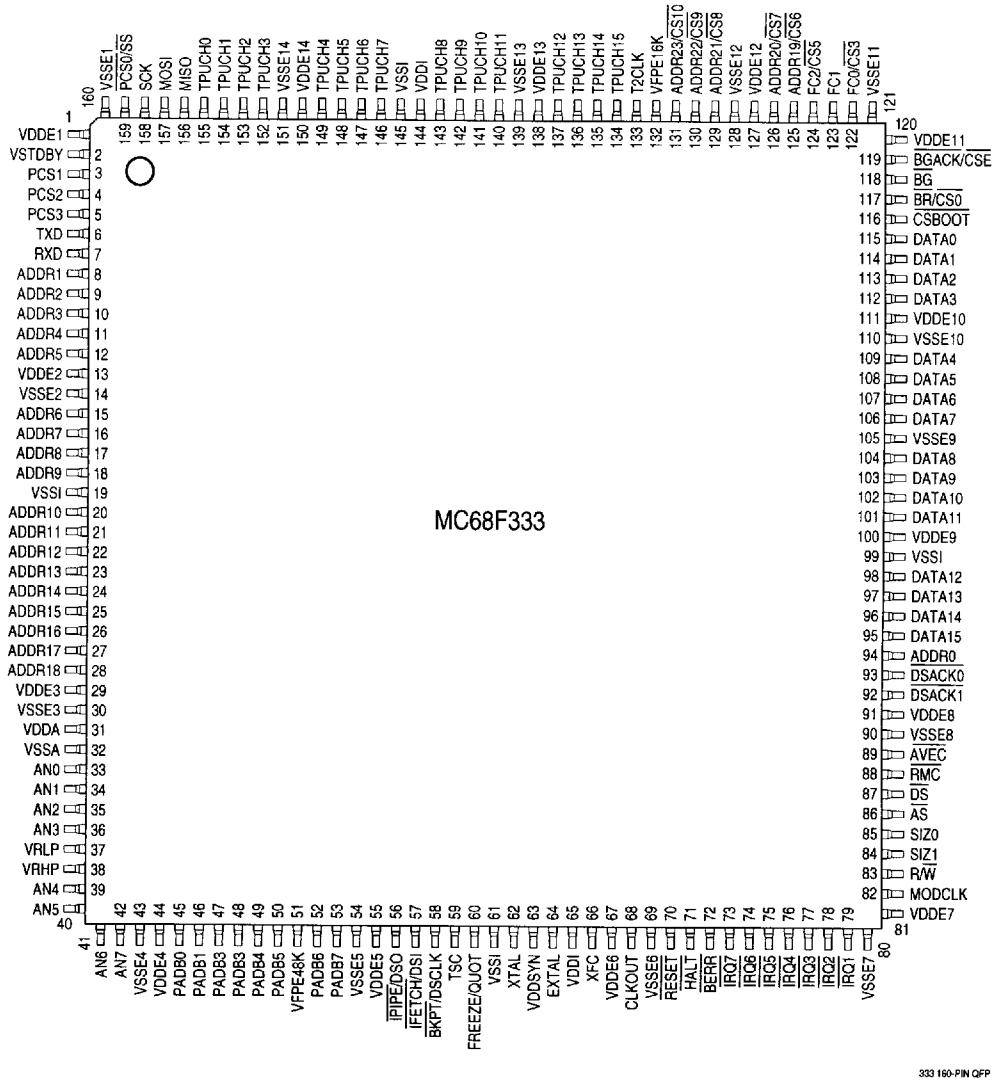
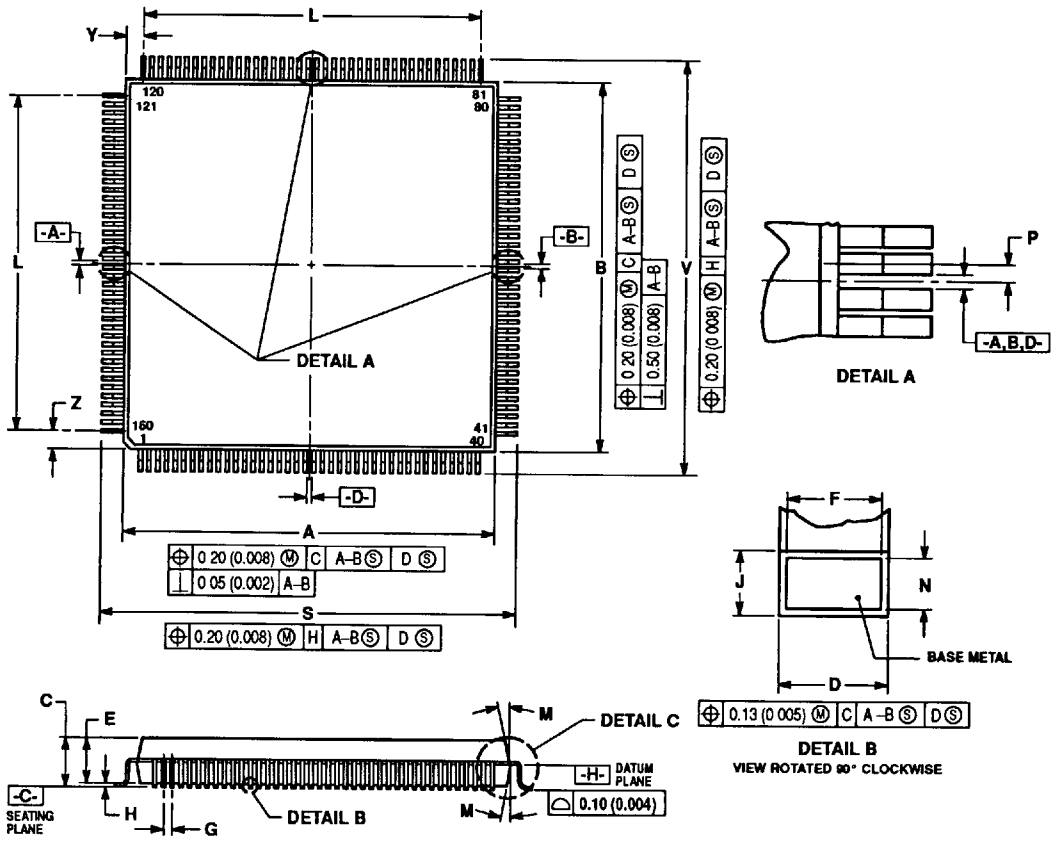


Figure B–1. 160-Pin Plastic Surface Mount Package Pin Assignments



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	0.152
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.650 BSC		0.0256 BSC	
H	0.25	0.35	0.010	0.012
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 REF		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.0130 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.00	31.40	1.220	1.236
W	0.40	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

CASE 864A–01
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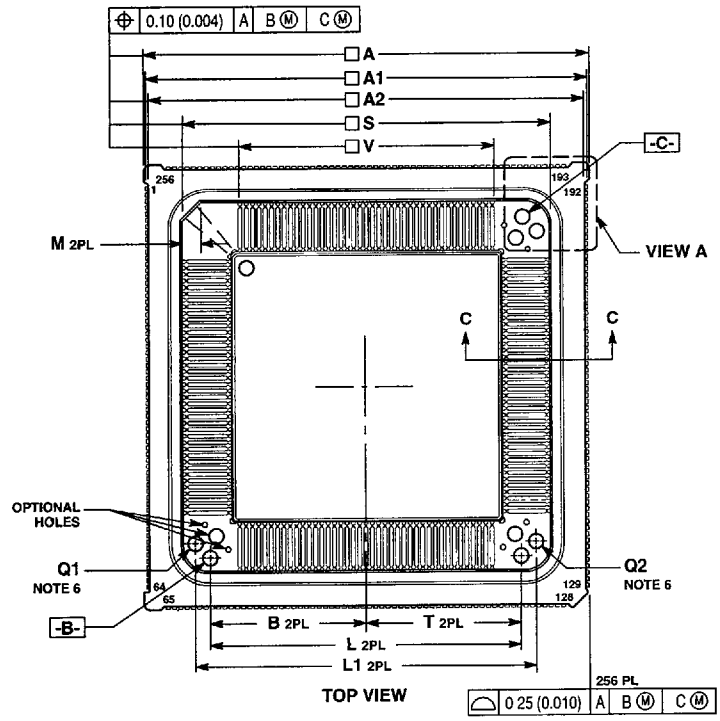
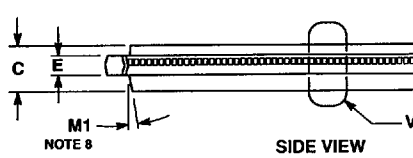
Figure B–2. 160-Pin Package Dimensions

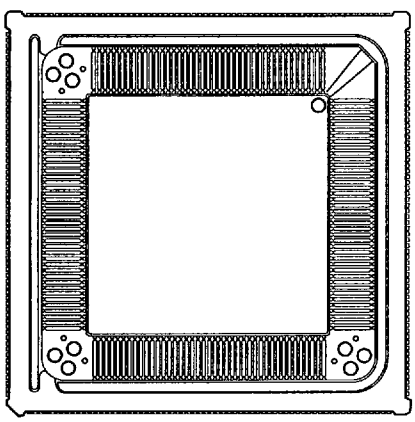
B



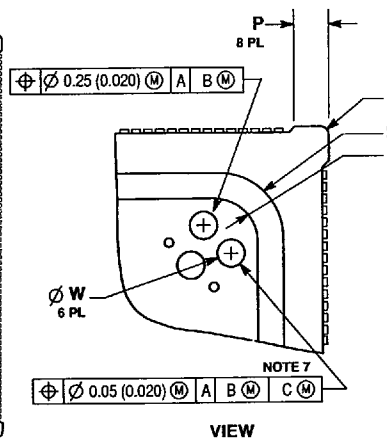
NOTES
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. A DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.20 (0.008) PER SIDE.
4. A AND S DIMENSIONS INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE.
5. UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTERLINES.
6. B AND C DATUM HOLES ARE TO BE USED FOR TRIM, FORM AND EXCISE OF THE MOLDED PACKAGE ONLY. HOLES Q1 AND Q2 ARE TO BE USED FOR ELECTRICAL TESTING ONLY.
7. NON-DATUM HOLES ONLY.
8. APPLIES TO RING AND PACKAGE FEATURES.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	45.87	46.13	1.806	1.816
A1	45.70 BSC		1.799 BSC	
A2	45.17	45.43	1.778	1.789
B	16.10 BSC		0.634 BSC	
C	4.70	4.90	0.185	0.193
D	0.40	0.50	0.016	0.020
D1	0.22	0.38	0.009	0.015
E	1.90	2.10	0.075	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
G1	0.65 BSC		0.026 BSC	
H	1.70	1.90	0.067	0.075
J	0.13	0.23	0.005	0.009
L	32.20 BSC		1.268 BSC	
L1	35.20 BSC		1.386 BSC	
M	1.30	2.30	0.051	0.091
M1	8° MAX		8° MAX	
N	0.13	0.17	0.005	0.007
P	1.77	2.03	0.070	0.080
R	0.40	0.60	0.016	0.024
R1	3.50	4.50	0.138	0.177
R2	2.00	3.00	0.079	0.118
S	37.87	38.13	1.491	1.501
T	16.10 BSC		0.634 BSC	
V	26.30	26.40	1.035	1.039
W	1.45	1.55	0.057	0.061
AA	0.45	0.85	0.018	0.033
AB	0.30	0.60	0.012	0.024
AC	1.37	1.63	0.054	0.064
AD	1.37	1.63	0.054	0.064
AH	27.90	28.10	1.098	1.106
AJ	3.20	3.40	0.126	0.134





BOTTOM VIEW OF UNIT IN MOLDED CARRIER RING



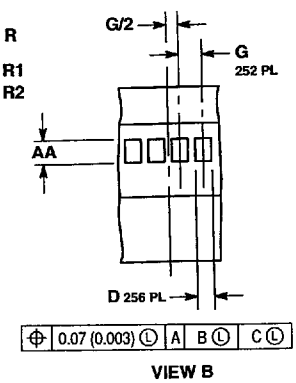


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Figure B–3. 160-Pin Molded Carrier Ring Assembly (Part 1)

B

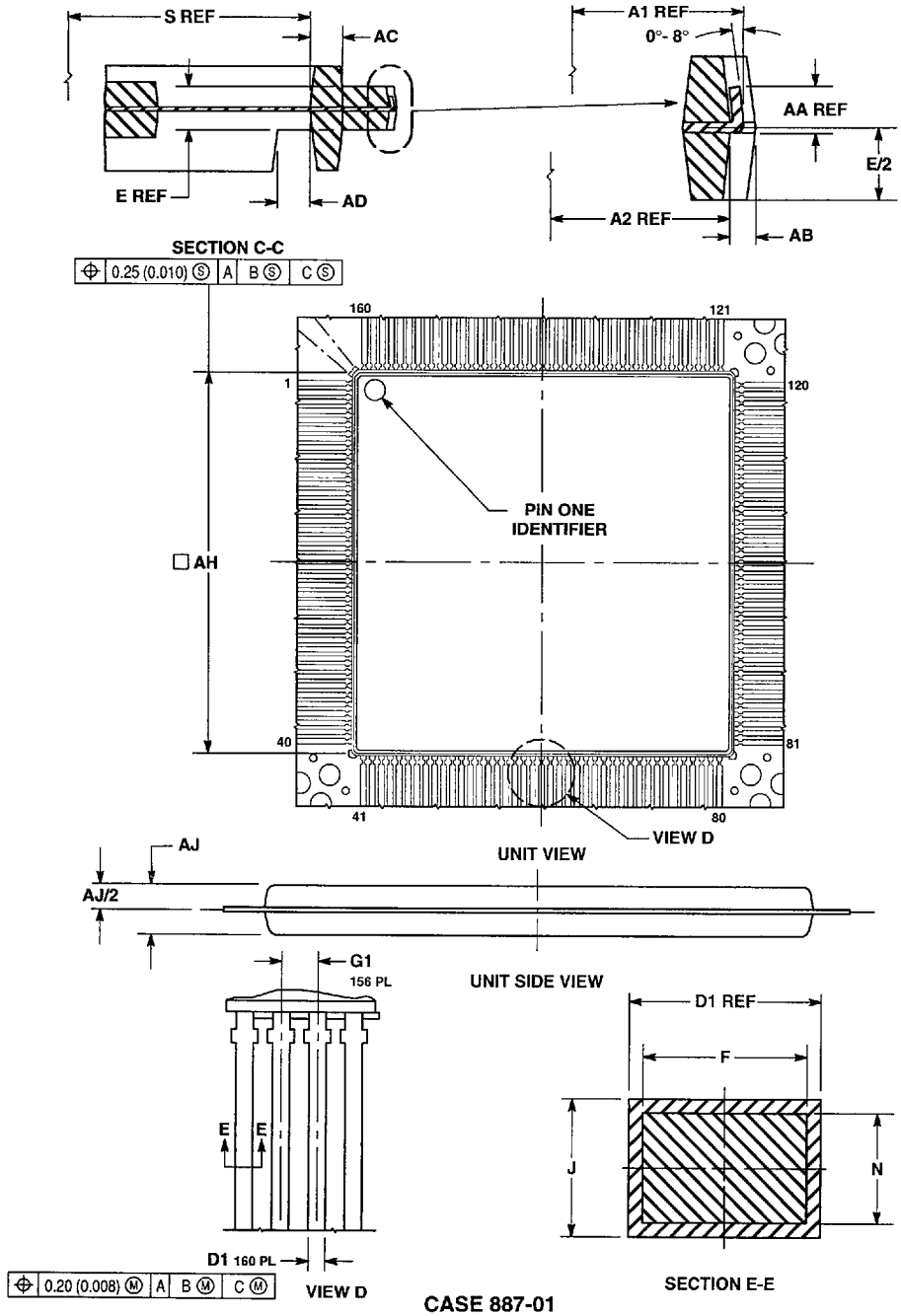

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Figure B–3. 160-Pin Molded Carrier Ring Assembly (Part 2)

B

Table B–1. MC68F333 Ordering Information

Package	Temperature	Frequency	Shipping Method	Order Number
160-Pin Plastic Surface Mount	–40 to +85°C	16.78 MHz	24 pc tray	XC68F333CFT16
			2 pc tray	SPAKXCF333CFT16
		20 MHz	24 pc tray	XC68F333CFT20
			2 pc tray	SPAKXCF333CFT20
		25 MHz	24 pc tray	XC68F333CFT25
			2 pc tray	SPAKXCF333CFT25
	–40 to +105°C	16.78 MHz	24 pc tray	XC68F333VFT16
			2 pc tray	SPAKXCF333VFT16
		20 MHz	24 pc tray	XC68F333VFT20
			2 pc tray	SPAKXCF333VFT20
		25 MHz	24 pc tray	XC68F333VFT25
			2 pc tray	SPAKXCF333VFT25
	–40 to +125°C	16.78 MHz	24 pc tray	XC68F333MFT16
			2 pc tray	SPAKXCF333MFT16
		20 MHz	24 pc tray	XC68F333MFT20
			2 pc tray	SPAKXCF333MFT20
		25 MHz	24 pc tray	XC68F333MFT25
			2 pc tray	SPAKXCF333MFT25
160-Pin Molded Carrier Ring	–40 to +85°C	16.78 MHz	10/tube	XC68F333CFM16
		20 MHz	10/tube	XC68F333CFM20
		25 MHz	10/tube	XC68F333CFM25
	–40 to +105°C	16.78 MHz	10/tube	XC68F333VFM16
		20 MHz	10/tube	XC68F333VFM20
		25 MHz	10/tube	XC68F333VFM25
	–40 to +125°C	16.78 MHz	10/tube	XC68F333MFM16
		20 MHz	10/tube	XC68F333MFM20
		25 MHz	10/tube	XC68F333MFM25

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