Features

- **4 Multiplier-Accumulators**
- **40 Bits Accuracy**
- **16 Bit Data and Coefficients**
- **4-tap Filter With 27 MHz Sample Rate**
- **Programmable to Give up to 256 Taps With Sampling Reducing Proportionally to 421,875 kHz**
- **Programmable Rounding and Truncation to 16 Bit**
- **8 Bit Standard Microprocessor Interface**
- **64-pin PQFP, 68-pin PGA68 or 68-pin LCC68 Packaging**

Description

The AT76C001 Programmable Finite Impulse Response (FIR) Filter implements a 4th order FIR cell built around 4 multiplier-accumulators. It contains a dual-port RAM and a RAM which are used to implement FIR filters of up to 256 taps. High order filters are achieved by multiplexing the 4th order cell and accumulating the intermediate results up to 40 bits, so that there is no loss of accuracy.

The maximum frequency of the AT76C001 is 27 MHz. For 4-tap FIR filter, the incoming sample rate can be as high as 27 MHz. For higher order FIR filters, the sample rate can be as high as the circuit frequency divided by the 4th order cell multiplexing factor.

A programmable normalization block allows the choice of the 16 significant bits from the 40 bit internal result which can be previously rounded by adding 0.5 LSB according to the 16 significant bit locations. The AT76C001 has a microprocessor interface which can be configured to be Intel or Motorola compatible.

Applications

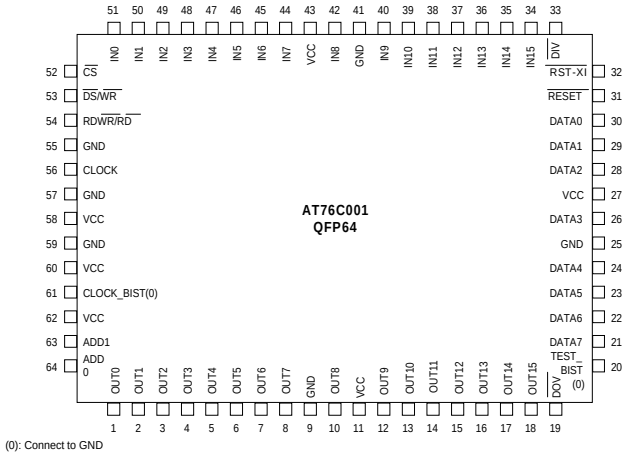
- **Digital Filters (video, audio, etc.)**
- **Correlation**
- **Image Processing**

CBIC Programmable FIR Filter

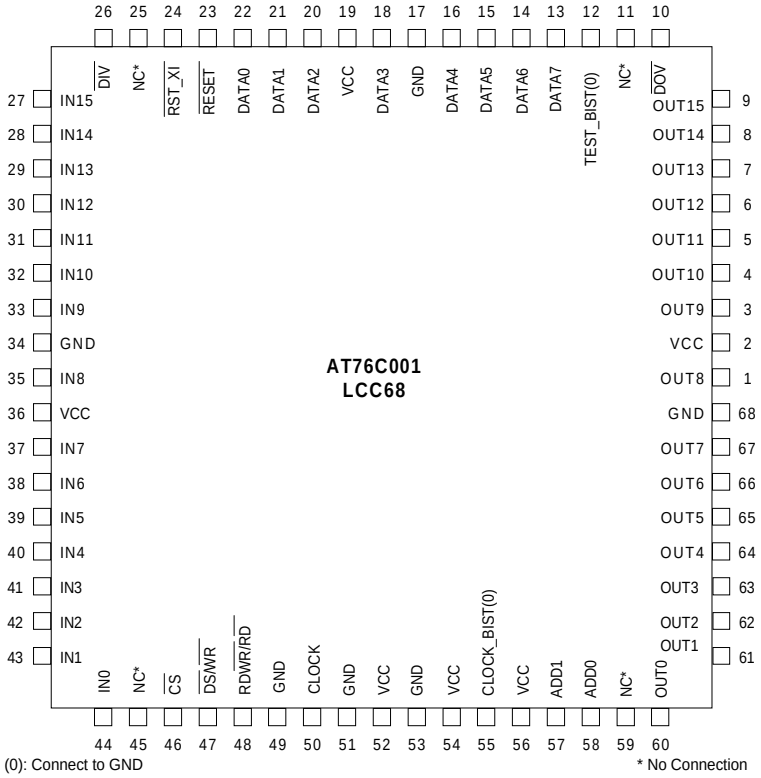
AT76C001

Pin Description

Name	Pin Number			Type	Function
	QFP64 Packaging	LCC68 Packaging	PGA68 Packaging		
IN<15:0>	34-40, 42, 44-51	27-33, 35, 37-44	K10-11, J10-11, H10-11, G10, F10, E10-11, D10-11, C10-11, B11-10	I	Input sample
DIV	33	26	L10	I	Input sample valid. Active low
RST_X1	32	24	K9	I	Force input sample to 0. Useful for interpolation implementation
OUT<15:0>	18-12, 10, 8-1	9-3, 1, 67-60	K1, J1-2, H1-2, G1-2, F2, E2, D1-2, C1-2, B1-2, A2	O	Output filtered sample
DOV	19	10	K2	O	Output filtered sample valid. Active low
DATA<7:0>	21-24, 26, 28-30	13-16, 18, 20-22	L3, K4, L4, K5-7, L7, K8	I/O	Microprocessor interface data bus. Used for accessing internal registers and to write the coefficients of the filter
CS	52	46	B9	I	Chip select. Active low
DS/WR	53	47	A9	I	Microprocessor interface data strobe (Motorola mode) or Write signal (Intel mode). Active low
RDWR/RD	54	48	B8	I	Microprocessor interface Read/Write signal (Motorola mode) or Read signal (Intel mode). Active low
ADD<1:0>	63-64	57-58	A4, B3	I	Microprocessor interface address bus
RESET	31	23	L8	I	Circuit master reset. Active low
CLOCK	56	50	B7	I	Circuit clock (27 MHz max)
CLOCK_BIST	61	55	A5	I	For internal use. Connect to ground
TEST_BIST	20	12	K3	I	For internal use. Connect to ground
VCC	11, 27, 43, 58, 60, 62	2, 19, 36, 52, 54, 56	B4-6, F1, F11, L6		Power supply (+5V)
GND	9, 25, 41, 55, 57, 59	17, 34, 49, 51, 53	A6-8, E1, G11, L5		Ground
NC		11, 25, 45, 59	A3, A10, L2, L9		No connection



Plan View of AT76C001 in QFP64 Package



Plan view of AT76C001 in LCC68 package

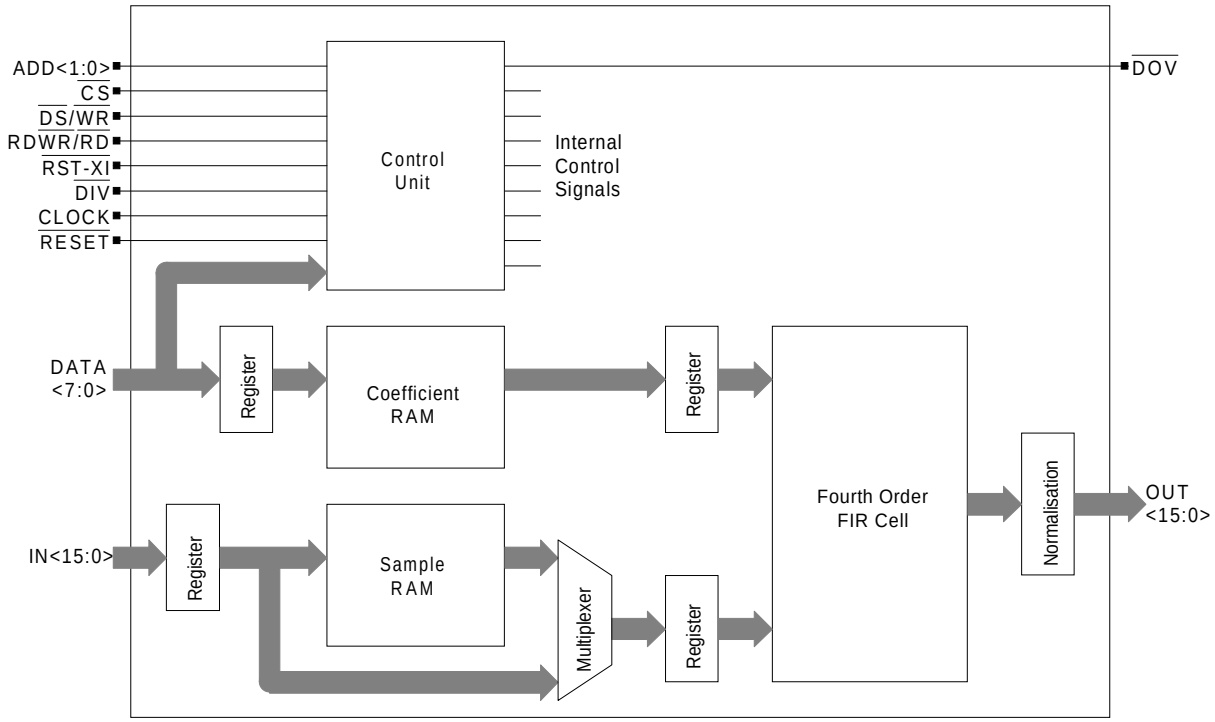
	1	2	3	4	5	6	7	8	9	10	11
L		NC*	DATA7	DATA5	GND	VCC	DATA1	$\overline{\text{RESET}}$	NC*	$\overline{\text{DIV}}$	
K	OUT15	$\overline{\text{DOV}}$	TC(0)	DATA6	DATA4	DATA3	DATA2	DATA0	$\overline{\text{RST\_XI}}$	IN15	IN14
J	OUT14	OUT13								IN13	IN12
H	OUT12	OUT11								IN11	IN10
G	OUT10	OUT9								IN9	GND
F	VCC	OUT8				**AT76C001 PGA68**				IN8	VCC
E	GND	OUT7								IN7	IN6
D	OUT6	OUT5								IN5	IN4
C	OUT4	OUT3								IN3	IN2
B	OUT2	OUT1	ADD0	VCC	VCC	VCC	CLOCK	RD$\overline{\text{WR}}$/ $\overline{\text{RD}}$	$\overline{\text{CS}}$	IN0	IN1
A		OUT0	NC*	ADD1	CB(0)	GND	GND	GND	$\overline{\text{DS}}$/$\overline{\text{WR}}$	NC*	

(0): Connect to GND

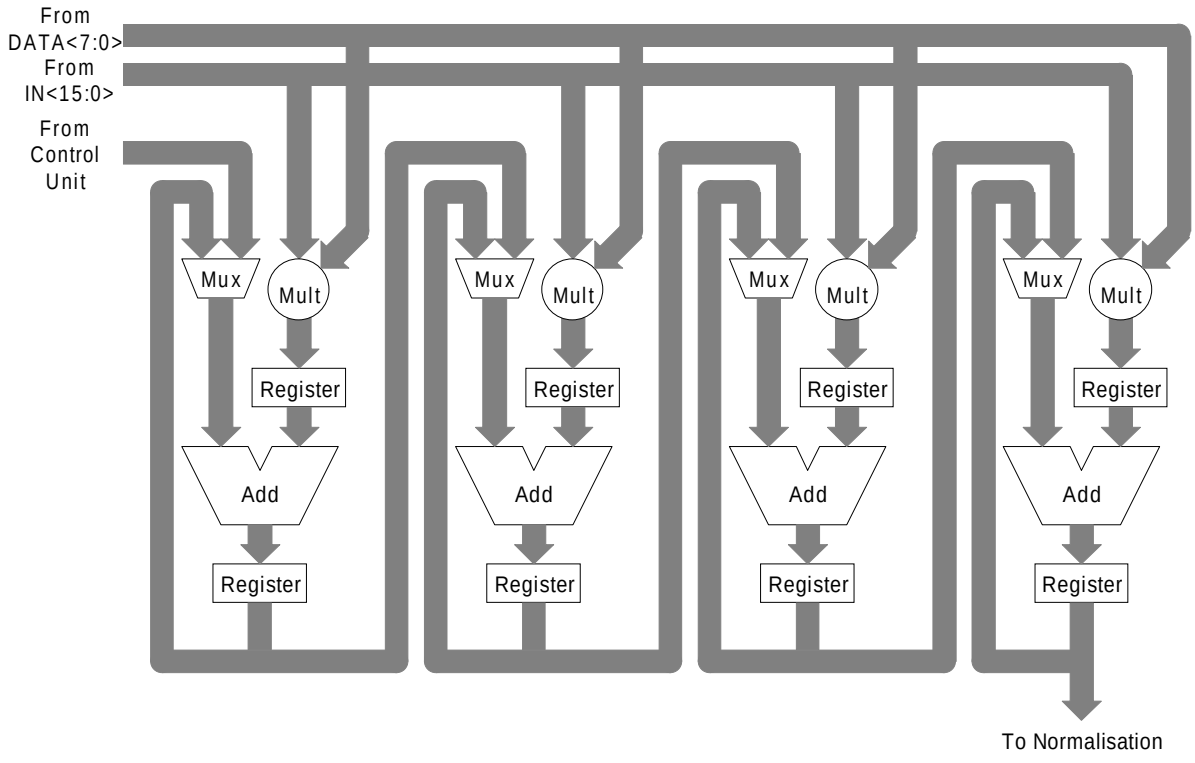
* No Connection

Plan view of AT76C001 in PGA68 package

Block Diagram



Fourth Order FIR Cell



Functional Description

The AT76C001 has an architecture built around a 4-tap non-recursive filter cell. This allows a 4-tap filter to be implemented, e.g.

$$y(n) = a(0)x(n) + a(1)x(n-1) + a(2)x(n-2) + a(3)x(n-3)$$

where x = 16 bit incoming sample

y = 16 bit filtered sample

a = 16 bit coefficient

This operating mode is called ‘single mode’.

The AT76C001 can implement up to 256-tap filters by multiplexing the 4th order structure, using internal RAMs. Nth order FIR filters can be divided into P 4th-order FIR sub-filters where P is the integer part of (N+3)/4. Thus the complete filter is evaluated by accumulating the contributions of each elementary 4th order sub-filter:

$$y(n) = y(n,0) + y(n,1) + ... + y(n,P-1)$$

where $y(n,j) = a(4j)x(n-4j) + a(4j+1)x(n-4j-1)$

$+ a(4j+2)x(n-4j-2) + a(4j+3)x(n-4j-3)$

j = number of the sub-filter

This operating mode is called ‘sequential mode’.

If (N+3)/4 is greater than P, then some coefficients of the last sub-filter will be set to zero automatically by the circuit.

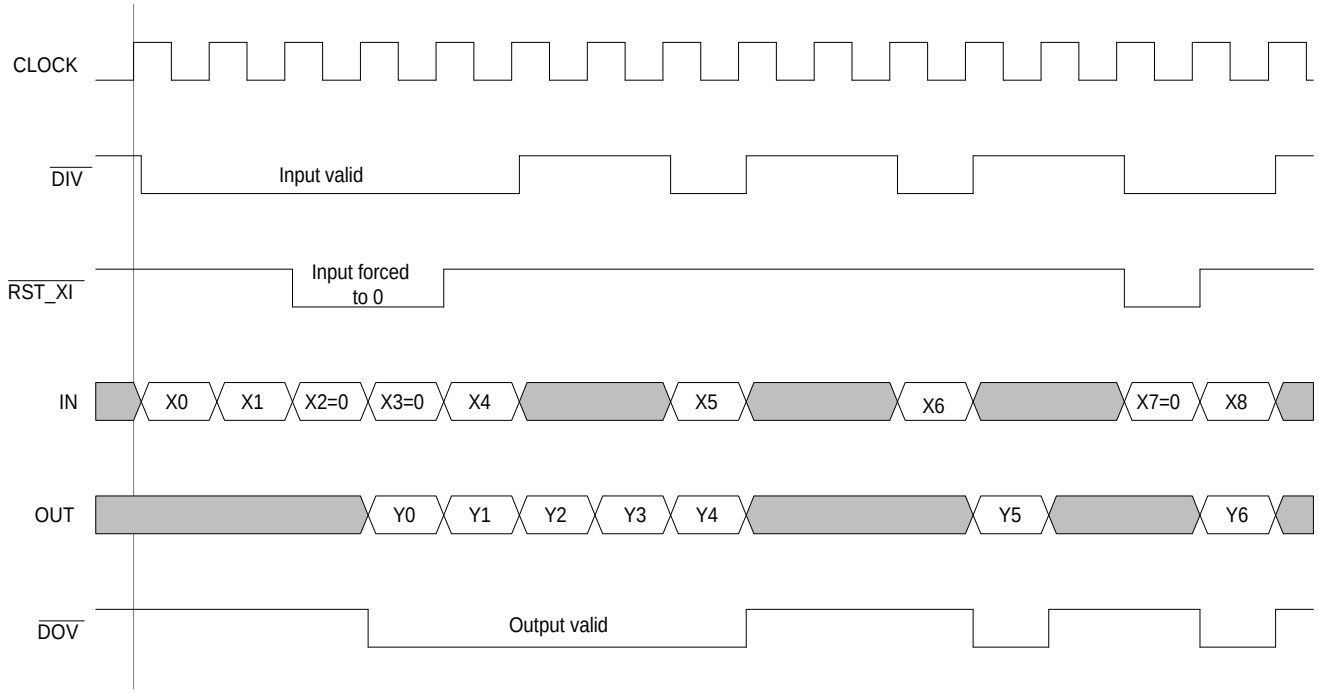
In single mode, the incoming sample rate can be as high as the circuit frequency (27 MHz). A new incoming sample is notified by a low level on DIV input signal and clocked by the rising edge of the circuit clock CLOCK.

If there is a low level set on DIV and then a low level is set on RST_XI input, then a ‘zero’ sample is fed internally into the circuit.

For each new sample, a filtered sample is calculated. Valid output filtered samples are notified by a low level on DOV output signal. The timing diagram below illustrates the single mode operation.

In sequential mode, an N-tap filter is divided into P 4-tap filters. Consequently, the incoming sample rate must be at least P times slower than the circuit rate. As in single mode, a new incoming sample is notified by a low level on DIV input signal and clocked by the rising edge CLOCK. But here, DIV defines a temporal window where XIN is valid and whose width must be at least one CLOCK period and at most P-1 clock periods. The timing diagrams below illustrate the case for an N-tap filter, where N is greater than 4 but less than 9, i.e., DIV must go to high level between two incoming signals.

Timing Diagram for Single Mode Operation



Microprocessor Interface

The AT76C001 has an 8 bit configurable microprocessor interface comprising the following signals:

DATA <7:0>	8 bit data bus
AD– <1:0>	2 bit address bus
CS	Chip Select
DS/WR	Data Strobe or Write signal
RDWR/RD	Read/Write signal or Read signal

By setting bit 1 of the configuration interface (INTEL/MOTO), it is possible to configure the microprocessor interface to be Motorola or Intel compatible. When chosen, the configuration must be locked by setting bit LOCK_CFG of the configuration register. This must be done first of all otherwise the circuit will not function properly.

Configuration	Motorola Mode	Intel Mode
Intel/Moto bit	Bit set to 0	Bit set to 1
Signals	DATA<7:0>	DATA<7:0>
	ADD<1:0>	ADD<1:0>
	CS	CS
	DS	WR
	RD/WR	RD

Internal Registers

The AT76C001 contains three internal registers accessible in Read and Write via the microprocessor interface, as soon as it is configured and locked. They are:

Configuration register (CFGR)
Normalization and Rounding Register (NORR)
Filter Order Register (FILR)

Configuration Register

It is an 8 bit register mapped at address 1hex = 01bin

Bit 0 = START/STOP	Activates/deactivates filtering
Bit 1 = INTEL/MOTO	Configures microprocessor interface to be Intel or Motorola.
Bit 2 = MSB/LSB	Indicates if 16 bit coefficients are written with Most Significant Byte or Least Significant Byte ahead.
Bit 3 = LOCK_CFG	Locks the microprocessor interface configuration.
Bit 4 = SING/SEQ	Indicates the operating mode of the 4th order cell, i.e. Single Mode or Sequential Mode.
Bit 5 = BUFF_FULL	Indicates that the sample input buffer contains N samples when implementing an N-tap FIR filter.

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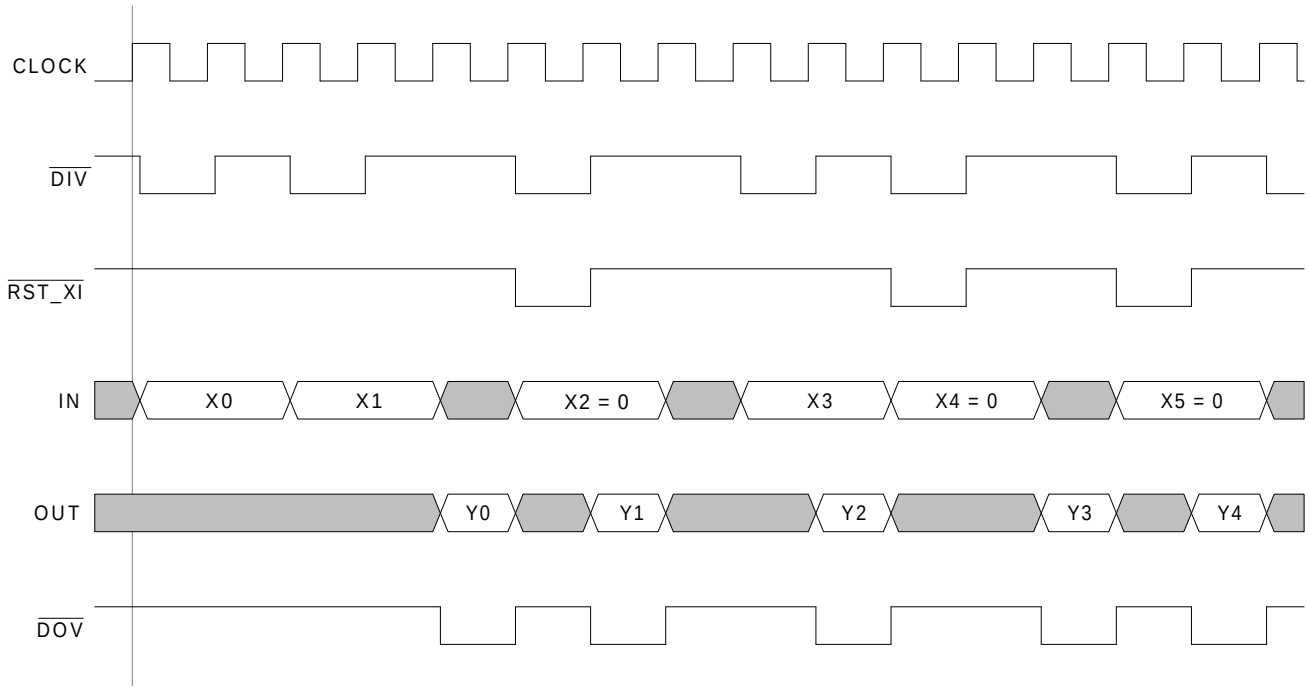
Timing Diagram for N-tap Filter where 4<N<9



Internal Registers (Continued)

Bit 6 = LAST_SFILT Indicates that the last sub-filter is accessed.

Bit 7 = END_INCOEFF Indicates that the last coefficient of the last sub-filter is being accessed.

Bit No	7	6	5	4	3	2	1	0
Bit Name	END_IN COEFF	LAST_S FILT	BUFF_ FULL	SING/ SEQ	CFG LOCK	INT/ MOTO	MSB/LSB	START/ STOP
Acc. Mode	R	R	R	R	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	0	0	1	0

Normalization and Rounding Register

The normalization and rounding register is a 5 bit register mapped at address 2h = 10b allows the selection of the 16 bit significant part of the internal 40 bit result; also defines the number of bits rounding value if rounding is desired.

Bit <3:0>= SEL <3:0> Selects the 16 bit part and defines the number of bits rounding value as illustrated in the following table:

Bit 3:0	OUT<15:0>	Rounding Value (Hex)
0000	RES<31:16>	00 0000 8000
0001	RES<32:17>	00 0001 0000
0010	RES<33:18>	00 0002 0000
0011	RES<34:19>	00 0004 0000
0100	RES<35:20>	00 0008 0000
0101	RES<36:21>	00 0010 0000
0110	RES<37:22>	00 0020 0000
0111	RES<38:23>	00 0040 0000
1XXX	RES<39:24>	00 0080 0000

Bit 4 = ROUNDEN Enables/disables rounding of the 40 bit result before normalization.

Bit No	4	3	2	1	0
Bit Name	ROUNDEN	SEL3	SEL2	SEL1	SEL0
Access Mode	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0

Filter Order Register

The filter order register is an 8 bit register mapped at address 3h=11b. It contains the number of the order of the filter to be implemented **minus 1**.

Reset Values

Bit No	7	6	5	4	3	2	1	0
Bit Name	FILT7	FILT6	FILT5	FILT4	FILT3	FILT2	FILT1	FILT0
Acc. Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Coefficient Writing

Filter coefficients are stored internally by writing to address 0hex = 00bin. The bit MSB/LSB of the configuration register indicates if the MSB is sent before the LSB and vice versa. Stored coefficients are not readable via the microprocessor interface. For an N-tap filter, 2xN writing is necessary. If N is not a multiple of 4, the remaining coefficients of the last sub-filter are set automatically to zero.

Application Examples

A 4-Tap FIR Filter in Motorola Mode

Example with coefficient MSB ahead and rounding enabled.

$$y_n = c_0x_n + c_1x_{n-1} + c_2x_{n-2} + c_3x_{n-3}$$

Where y_n is the output filtered sample, c is the coefficient and x is the incoming samples.

1. Firstly, unlock the microprocessor interface by writing a zero to bit 3 (this is normally performed by applying a Master reset).
2. Write 1100bin in the configuration register. This sets the configuration with bit 0 selecting stop mode, bit 1 selecting Motorola mode, bit 2 selecting MSB ahead, and bit 3 locks the configuration.
3. Write the Filter Order-1 in the FILT_ORD register, i.e. 03hex.
4. Write the 4 coefficients starting with the Most Significant Byte of c_0, then the LSB of c_0, etc.
5. Write 00010bin in the NORM register to enable rounding, and to select range of bits, for example bits 33 to18 of the 40 bit internal result.
6. Write 1101bin in the Configuration register to start the filter. At each new incoming sample, XIN, specified by a low level on DIV. The filtered sample XOUT is calculated and is notified by a low level on DOV. The

(continued)

Application Examples (Continued)

filtered XOUT is output 4 clock cycles after the sampling of the corresponding XIN input.

A 130-Tap FIR Filter in Intel Mode

Example with coefficient LSB ahead and rounding disabled.

$$y_n = c_0x_n + c_1x_{n-1} + \ldots\ldots + c_{128}x_{n-12} + c_{129}x_{n-129}$$

1. Firstly, unlock the microprocessor interface by writing a zero to bit 3 (this is normally performed by applying a Master reset).
2. Write 1010bin in the configuration register. This sets the configuration with bit 0 selecting stop mode, bit 1 selecting Intel mode, bit 2 selecting LSB ahead, and bit 3 locks the configuration.
3. Write the Filter Order-1 in the FILT_ORD register, i.e. 81hex
4. Write the 130 coefficients beginning with the LSB of c_0, then the MSB of c_0, etc.
5. Write 11xxx in the NORM register to disable rounding and to select bits 39 to 24 of the 40 bit internal result..
6. Write 1011bin in the Configuration register to start the filter. At each new transition high to low on DIV input signal, a new sample is fed into the filter. The corresponding filtered sample is output 4+33 clock cycles later and specified by a low level on DOV output signal. Here the incoming sample rate must at most be 33 times less than the circuit clock rate, where 33 represents the number of times the 4th order cell is multiplexed.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Conditions
V_{DD}	DC supply voltage	-0.5	5.5	V	
V_I	DC input voltage	-0.5	V_{DD}+ 0.5V	V	or see +-IIk
V_O	DC output voltage	-0.5	V_{DD}+ 0.5V	V	or see +-IOk
+-IIk	DC input diode current		10	mA	V_I<-0.5V V_I>V_{DD}+0.5V
+-IOk	DC output diode current		20	mA	V_O<-0.5V V_O>V_{DD}+0.5V
I_{OL}MAX	Continuous output current		10	mA	Industrial
I_{OH}-MAX	Continuous output current		10	mA	Industrial
T_{SH}	Time of outputs shorted		5	sec	

(continued)

Absolute Maximum Ratings (Continued)

T_A	Temperature range	-40	+85	C	Industrial
T_{SG}	Storage temperature	-65	+150	C	

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DD}	DC supply voltage	4.5	5.0	5.5	V	
V_I	DC input voltage	0	5.0	V_{DD}	V	
V_O	DC output voltage	0	5.0	V_{DD}	V	
T_A	Temperature range	-40		+85	C	Ind
T_R	Input rise time			15	ns	10%-90% CMOS
T_F	Input fall time			15	ns	10%-90% CMOS

DC Characteristics

Symbol	Parameter	Min	Max	Unit	Conditions
I_{IH}	Input leakage, no pullup	-1.0	+1.0	uA	V_{IN} = V_{DD} = 5.5V
I_{IL}	Input leakage, no pullup	-1.0	+1.0	uA	V_{IN} = 0 V_{DD}=5.5V
I_{OZ}	High-impedance output current bi-directional pins	-1.0	+1.0	uA	V_{DD}=5.5V
V_{IL}	Low level input voltage		30% V_{DD}	V	CMOS inputs and bi-dir
V_{IH}	High level input voltage	70% V_{DD}		V	CMOS inputs and bi-dir
V_{OL}	Low level output voltage		0.5	V	I_{OL}=5.0mA
V_{OH}	High level output voltage	V_{DD}-0.5		V	I_{OH}=5.0mA
C_{IN}	Input capacitance		7	pF	

AC Characteristics

Code	Description	Min	Max	Units
TCPH	Clock period	37		ns
TCLH	Clock high	15		ns
TCLL	Clock low	15		ns
TWRP	Write/read period	37		ns
TWRH	Write/read high	15		ns
TWRL	Write/read low	15		ns
TSIS	Synchronous signals to rising clock setup	5		ns
TSIH	Synchronous inputs to rising clock hold	5		ns
TSOD	Synchronous outputs to rising clock delay		10	ns
TWRCLD	Write/read to clock high	5		ns
TACWS	Asynchronous input setup	20		ns
TACWH	Asynchronous inputs hold	5		ns
TAOE	Asynchronous output enable		12	ns
TAOD	Asynchronous output disable		7	ns

See the illustration below for the interpretations of these characteristics.

AC Characteristics for Single Mode Operation