# ASYNCHRONOUS SRAM

# 512K x 8 SRAM

**+3.3V SUPPLY**
**REVOLUTIONARY PINOUT**

## FEATURES

- Fast access times: 10, 12 and 15ns
- Fast OE# access times: 5, 6and 7ns
- Single +3.3V ±0.3V power supply
- Fully static -- no clock or timing strobes necessary
- All inputs and outputs are TTL-compatible
- Three state outputs
- Center power and ground pins for greater noise immunity
- JEDEC standard for functionality and revolutionary pinout
- Easy memory expansion with CE# and OE# options
- Automatic CE# power down
- High-performance, low-power consumption, CMOS double-poly, double-metal process

## OPTIONS       MARKING

- Timing
  | | |
  |---|---|
  | 10ns access | -10 |
  | 12ns access | -12 |
  | 15ns access | -15 |

- Packages
  | | |
  |---|---|
  | 36-pin SOJ (400 mil) | J |

- Temperature
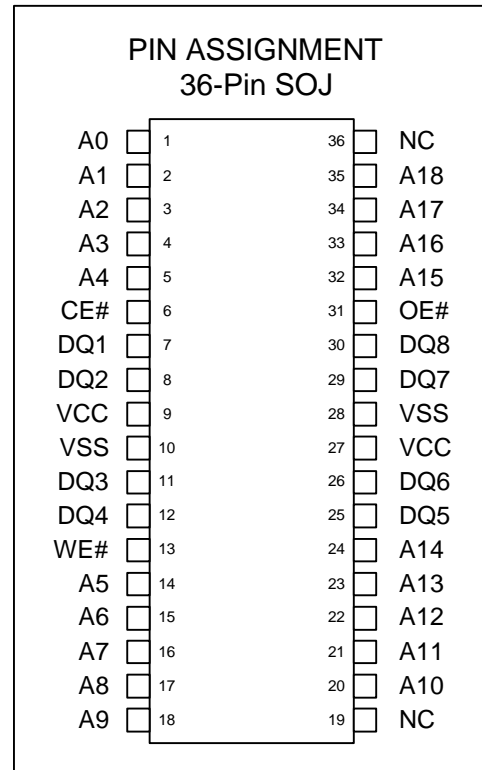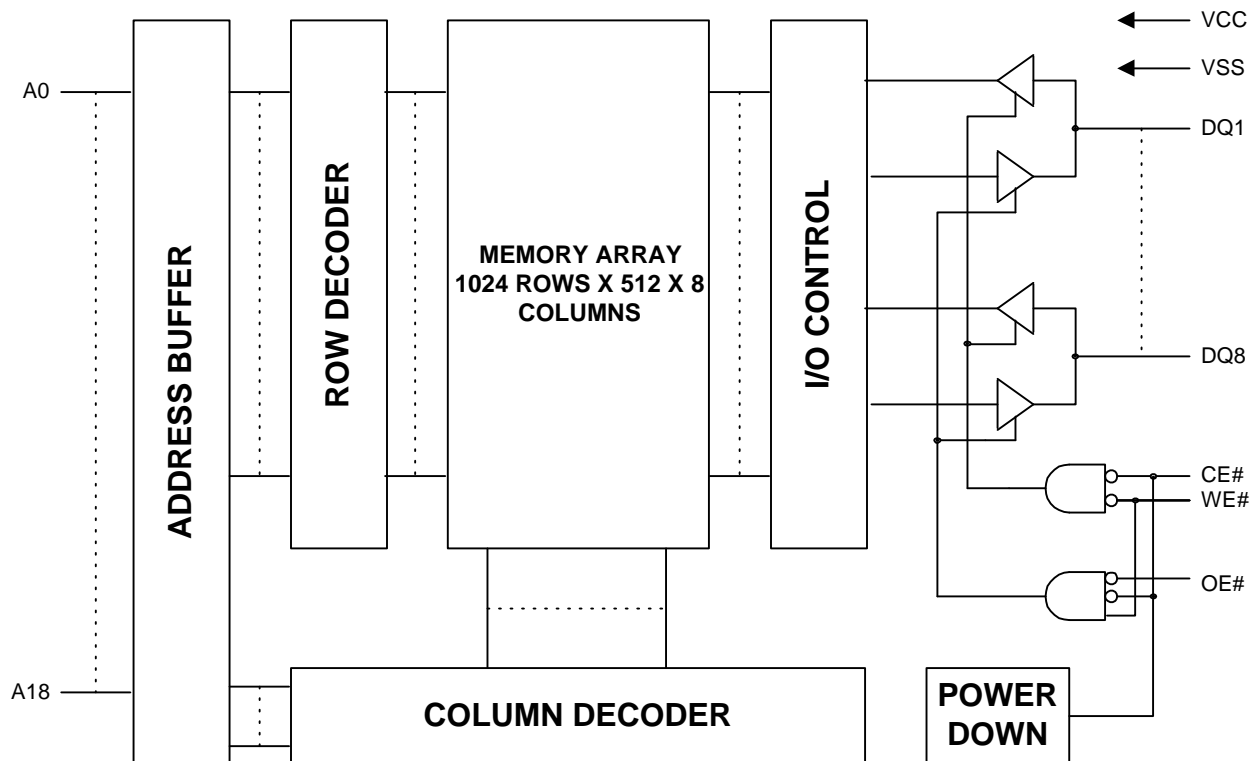  | | | |
  |---|---|---|
  | Commercial | None | (0°C to 70°C) |
  | Industrial | I | (-40°C to 85°C) |

## GENERAL DESCRIPTION

The GVT73512A8 is organized as a 524,288 x 8 SRAM using a four-transistor memory cell with a high performance, silicon gate, low-power CMOS process. Galvantech SRAMs are fabricated using double-layer polysilicon, double-layer metal technology.

This device offers center power and ground pins for improved performance and noise immunity. Static design eliminates the need for external clocks or timing strobes. For increased system flexibility and eliminating bus contention problems, this device offers chip enable (CE#) and output enable (OE#) with this organization.

Writing to these devices is accomplished when write enable (WE#) and chip enable (CE#) inputs are both LOW. Reading is accomplished when (CE#) and (OE#) go LOW with (WE#) remaining HIGH. The device offers a low power standby mode when chip is not selected. This allows system designers to meet low standby power requirements.

### PIN ASSIGNMENT
### 36-Pin SOJ

| | | | | |
|---|---|---|---|---|
| A0 | 1 | | 36 | NC |
| A1 | 2 | | 35 | A18 |
| A2 | 3 | | 34 | A17 |
| A3 | 4 | | 33 | A16 |
| A4 | 5 | | 32 | A15 |
| CE# | 6 | | 31 | OE# |
| DQ1 | 7 | | 30 | DQ8 |
| DQ2 | 8 | | 29 | DQ7 |
| VCC | 9 | | 28 | VSS |
| VSS | 10 | | 27 | VCC |
| DQ3 | 11 | | 26 | DQ6 |
| DQ4 | 12 | | 25 | DQ5 |
| WE# | 13 | | 24 | A14 |
| A5 | 14 | | 23 | A13 |
| A6 | 15 | | 22 | A12 |
| A7 | 16 | | 21 | A11 |
| A8 | 17 | | 20 | A10 |
| A9 | 18 | | 19 | NC |

## FUNCTIONAL BLOCK DIAGRAM



## TRUTH TABLE

| MODE | CE# | WE# | OE# | DQ | POWER |
|------|-----|-----|-----|-----|-------|
| READ | L | H | L | Q | ACTIVE |
| WRITE | L | L | X | D | ACTIVE |
| OUTPUT DISABLE | L | H | H | HIGH-Z | ACTIVE |
| STANDBY | H | X | X | HIGH-Z | STANDBY |

## PIN DESCRIPTIONS

| SOJ Pin Numbers | SYMBOL | TYPE | DESCRIPTION |
|------|--------|------|-------------|
| 1, 2, 3, 4, 5, 14, 15, 16, 17, 18, 20, 21, 22, 23, 24, 32, 33, 34, 35 | A0-A18 | Input | Addresses Inputs: These inputs determine which cell is addressed. |
| 13 | WE# | Input | Write Enable: This input determines if the cycle is a READ or WRITE cycle. WE# is LOW for a WRITE cycle and HIGH for a READ cycle. |
| 6 | CE# | Input | Chip Enable: This active LOW input is used to enable the device. When CE# is LOW, the chip is selected. When CE# is HIGH, the chip is disabled and automatically goes into standby power mode. |
| 31 | OE# | Input | Output Enable: This active LOW input enables the output drivers. |
| 7, 8,11, 12, 25, 26, 29, 30 | DQ1-DQ8 | Input/Output | SRAM Data I/O: Data inputs and data outputs |
| 9, 27 | VCC | Supply | Power Supply:3.3V ±0.3V |
| 10, 28 | VSS | Supply | Ground |

## ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to VSS........-0.5V to +4.6V

$V_{IN}$ .........................................................-0.5V to VCC+0.5V

Storage Temperature (plastic) ..........................-55°C to +125°

Junction Temperature ....................................................+125°

Power Dissipation ...........................................................1.2W

Short Circuit Output Current .......................................50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS
(All Temperature Ranges; VCC = 3.3V ±0.3V unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input High (Logic 1) voltage | | $V_{IH}$ | 2.2 | VCC+0.5 | V | 1, 2 |
| Input Low (Logic 0) Voltage | | $V_{IL}$ | -0.5 | 0.8 | V | 1, 2 |
| Input Leakage Current | $0V \leq V_{IN} \leq VCC$ | $IL_I$ | -5 | 5 | uA | |
| Output Leakage Current | Output(s) disabled, $0V \leq V_{OUT} \leq VCC$ | $IL_O$ | -5 | 5 | uA | |
| Output High Voltage | $I_{OH}$ = -4.0mA | $V_{OH}$ | 2.4 | | V | 1 |
| Output Low Voltage | $I_{OL}$ = 8.0mA | $V_{OL}$ | | 0.4 | V | 1 |
| Supply Voltage | | VCC | 3.0 | 3.6 | V | 1 |

| DESCRIPTION | CONDITIONS | SYM | TYP | -10 | -12 | -15 | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|
| Power Supply Current: Operating | Device selected; CE# $\leq V_{IL}$; VCC =MAX; f=$f_{MAX}$; outputs open | Icc | 90 | 240 | 210 | 175 | mA | 3, 14 |
| TTL Standby | CE# $\geq V_{IH}$; VCC = MAX; f=$f_{MAX}$ | $I_{SB1}$ | 30 | 85 | 80 | 70 | mA | 14 |
| CMOS Standby | CE1# $\geq$VCC -0.2; VCC = MAX; all other inputs $\leq$ VSS +0.2 or $\geq$VCC -0.2; all inputs static; f= 0 | $I_{SB2}$ | 0.1 | 10 | 10 | 10 | mA | 14 |

## CAPACITANCE

| DESCRIPTION | CONDITIONS | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance | $T_A$ = 25°C; f = 1 MHz VCC = 3.3V | $C_I$ | 6 | pF | 4 |
| Input/Output Capacitance (DQ) | | $C_{I/O}$ | 8 | pF | 4 |

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## AC ELECTRICAL CHARACTERISTICS

(Note 5) (All Temperature Ranges; VCC = 3.3V $\pm$0.3V)

| DESCRIPTION | SYM | - 10 | | - 12 | | - 15 | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| **READ Cycle** | | | | | | | | | |
| READ cycle time | $^t$RC | 10 | | 12 | | 15 | | ns | |
| Address access time | $^t$AA | | 10 | | 12 | | 15 | ns | |
| Chip Enable access time | $^t$ACE | | 10 | | 12 | | 15 | ns | |
| Output hold from address change | $^t$OH | 3 | | 3 | | 3 | | ns | |
| Chip Enable to output in Low-Z | $^t$LZCE | 3 | | 3 | | 3 | | ns | 4, 7 |
| Chip disable to output in High-Z | $^t$HZCE | | 5 | | 6 | | 7 | ns | 4, 6, 7 |
| Output Enable access time | $^t$AOE | | 5 | | 6 | | 7 | ns | |
| Output Enable to output in Low-Z | $^t$LZOE | 0 | | 0 | | 0 | | ns | |
| Output Enable to output in High-Z | $^t$HZOE | | 5 | | 6 | | 7 | ns | 4, 6 |
| Chip Enable to power-up time | $^t$PU | 0 | | 0 | | 0 | | ns | 4 |
| Chip disable to power-down time | $^t$PD | | 10 | | 12 | | 15 | ns | 4 |
| **WRITE Cycle** | | | | | | | | | |
| WRITE cycle time | $^t$WC | 10 | | 12 | | 15 | | ns | |
| Chip Enable to end of write | $^t$CW | 8 | | 8 | | 9 | | ns | |
| Address valid to end of write, with OE# HIGH | $^t$AW | 8 | | 8 | | 9 | | ns | |
| Address setup time | $^t$AS | 0 | | 0 | | 0 | | ns | |
| Address hold from end of write | $^t$AH | 0 | | 0 | | 0 | | ns | |
| WRITE pulse width | $^t$WP2 | 10 | | 10 | | 11 | | ns | |
| WRITE pulse width, with OE# HIGH | $^t$WP1 | 8 | | 8 | | 9 | | ns | |
| Data setup time | $^t$DS | 5 | | 6 | | 7 | | ns | |
| Data hold time | $^t$DH | 0 | | 0 | | 0 | | ns | |
| Write disable to output in Low-Z | $^t$LZWE | 3 | | 4 | | 5 | | ns | 4, 7 |
| Write Enable to output in High-Z | $^t$HZWE | | 6 | | 6 | | 7 | ns | 4, 6, 7 |

## AC TEST CONDITIONS

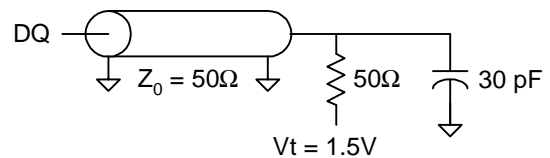| | |
|---|---|
| Input pulse levels | 0V to 3.0V |
| Input rise and fall times | 1.5ns |
| Input timing reference levels | 1.5V |
| Output reference levels | 1.5V |
| Output load | See Figures 1 and 2 |

## OUTPUT LOADS
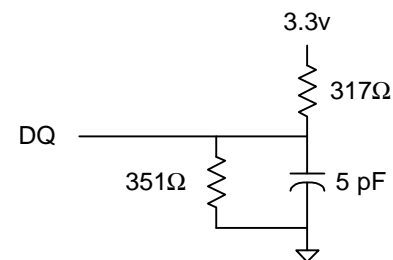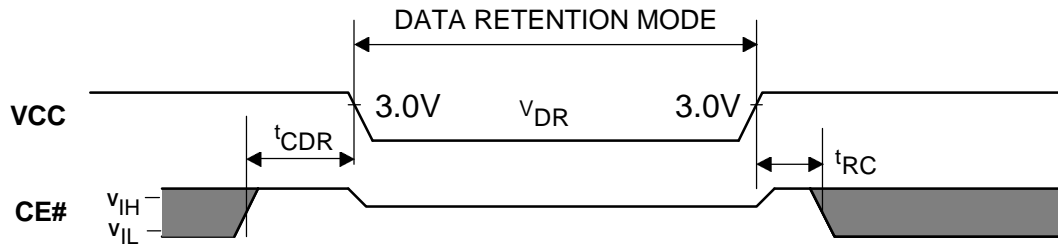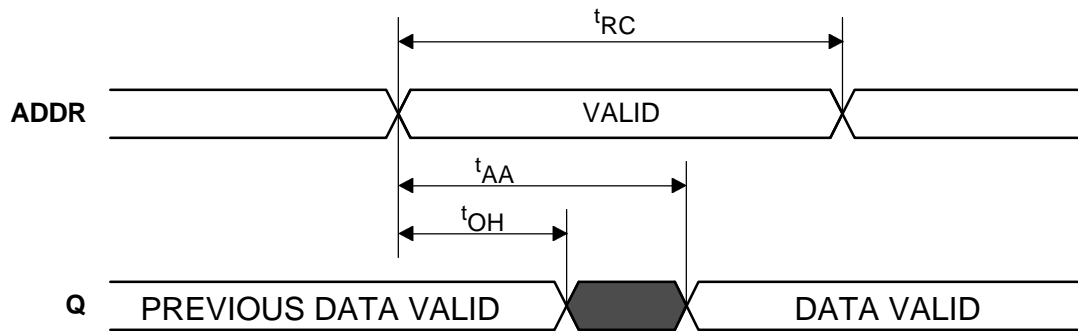


Fig. 1 OUTPUT LOAD EQUIVALENT



Fig. 2 OUTPUT LOAD EQUIVALENT

### NOTES

1.  All voltages referenced to VSS (GND).

2.  Overshoot:     $V_{IH} \leq$ +6.0V for t $\leq$ $^tRC$ /2.
    Undershoot:     $V_{IL} \leq$ -2.0V for t $\leq$ $^tRC$ /2

3.  $I_{cc}$ is given with no output current. $I_{cc}$ increases with greater output loading and faster cycle times.

4.  This parameter is sampled.

5.  Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.

6.  Output loading is specified with $C_L$=5pF as in Fig. 2. Transition is measured $\pm$500mV from steady state voltage.

7.  At any given temperature and voltage condition, $^t$HZCE is less than $^t$LZCE and $^t$HZWE is less than $^t$LZWE.

8.  WE# is HIGH for READ cycle.

9.  Device is continuously selected. Chip enable and output enables are held in their active state.

10. Address valid prior to, or coincident with, latest occurring chip enable.

11. $t_{RC}$ = Read Cycle Time.

12. Chip Enable and Write Enable can initiate and terminate a WRITE cycle.

13. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.

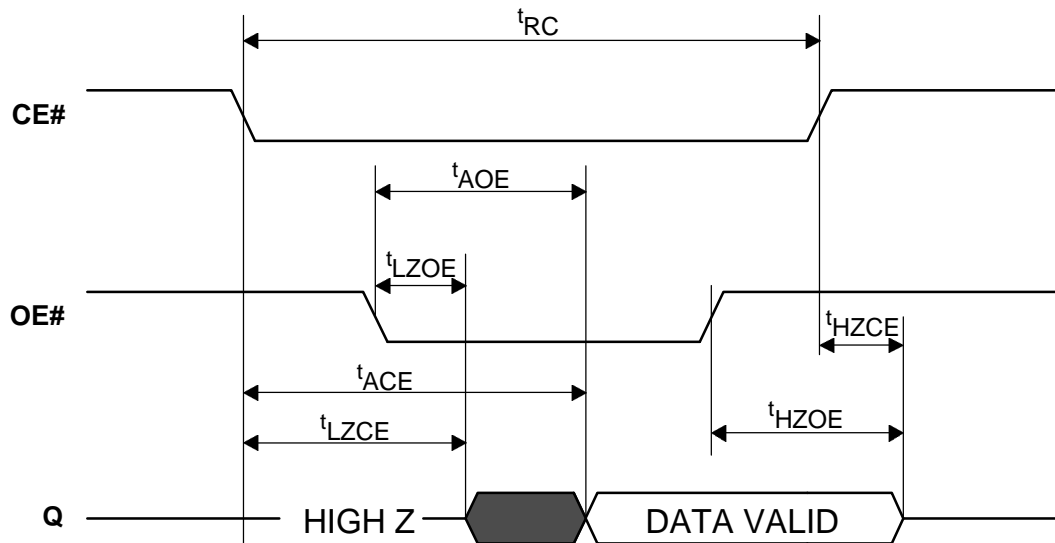14. Typical values are measured at 3.3V, 25$^o$C and 20ns cycle time.

## LOW VCC DATA RETENTION WAVEFORM



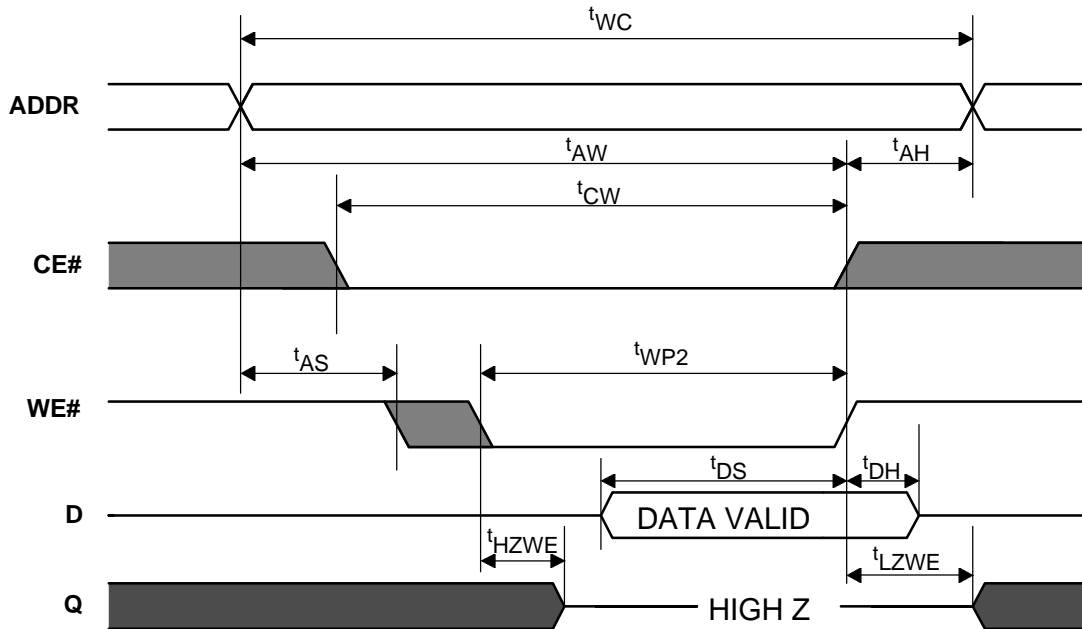## READ CYCLE NO. 1[8, 9]



## READ CYCLE NO. 2[7, 8, 10, 12]



DON'T CARE

UNDEFINED

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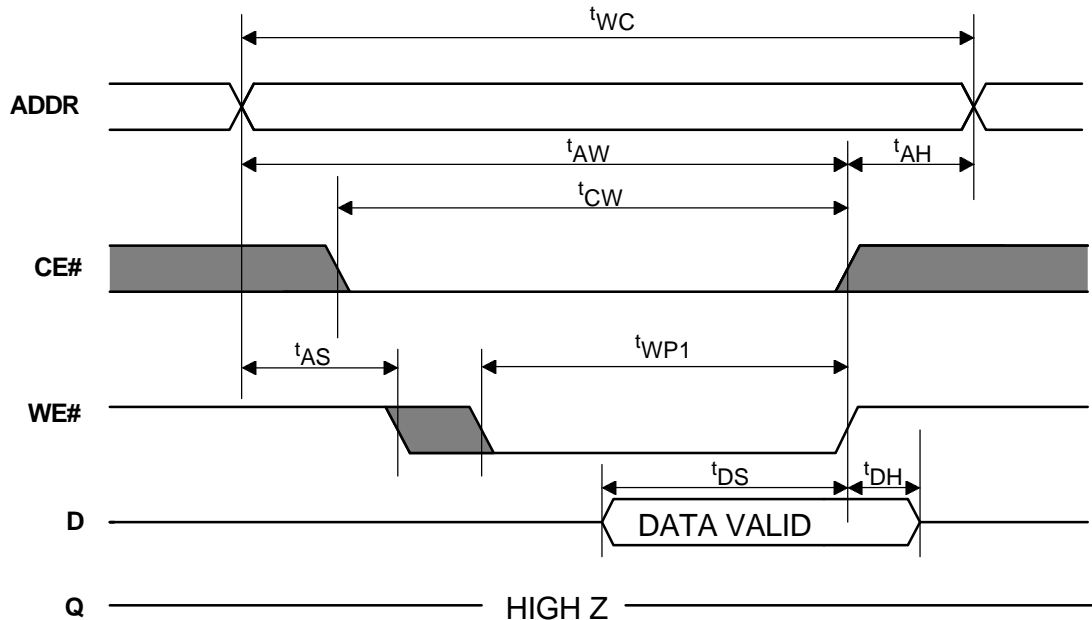Galvantech, Inc. reserves the right to change products or specifications without notice.

## WRITE CYCLE NO. 1 [7, 12, 13]
### (Write Enable Controlled with Output Enable OE# active LOW))



## WRITE CYCLE NO. 2 [12, 13]
### (Write Enable Controlled with Output Enable OE# inactive HIGH)
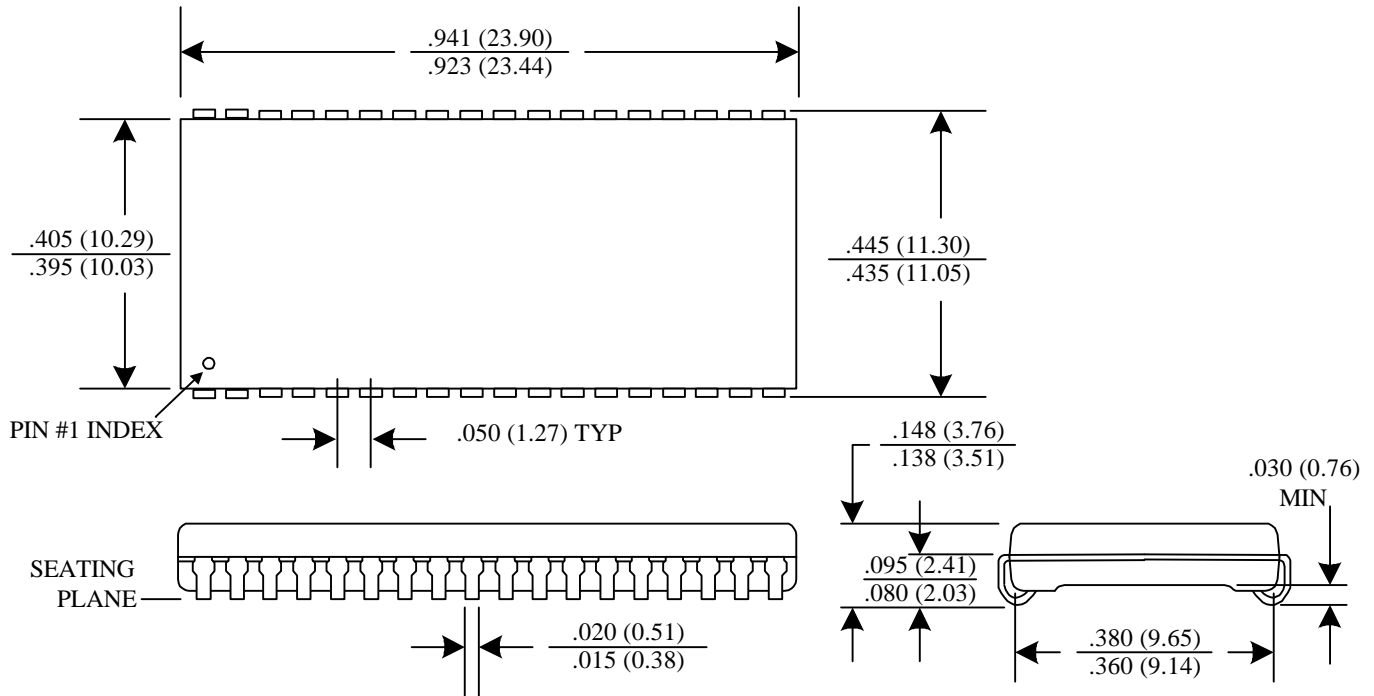


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## WRITE CYCLE NO. 3[12, 13]
### (Chip Enable Controlled)



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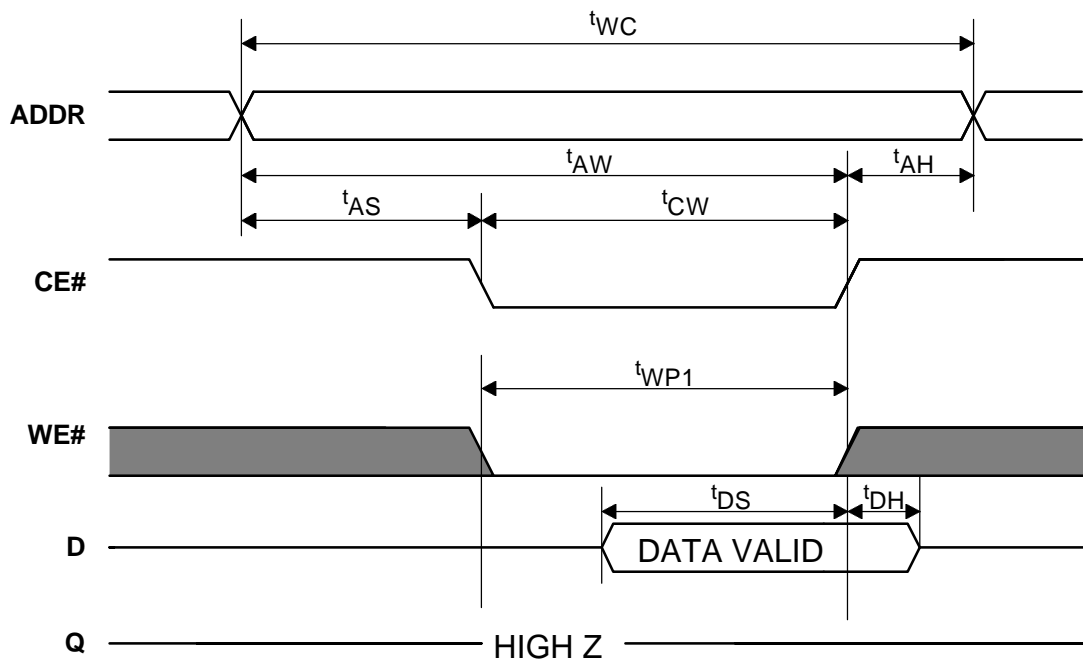
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**Package Dimensions**

## 36-pin 400 Mil Plastic SOJ (J)



.941 (23.90) / .923 (23.44)

.405 (10.29) / .395 (10.03)

.445 (11.30) / .435 (11.05)

PIN #1 INDEX

.050 (1.27) TYP

.148 (3.76) / .138 (3.51)

.030 (0.76) MIN

SEATING PLANE

.095 (2.41) / .080 (2.03)

.020 (0.51) / .015 (0.38)

.380 (9.65) / .360 (9.14)

Note: All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical, min where noted.

## Ordering Information

### GVT 73512A8 XX - XX X



Galvantech Prefix

Part Number

Temperature (Blank = Commercial
I = Industrial)

Speed ( 10 = 10ns
12 = 12ns, 15= 15ns)

Package (J = 400 mil SOJ)