v01.0604

HMC375LP3

GaAs PHEMT MMIC LOW NOISE AMPLIFIER, 1.7 - 2.2 GHz

Typical Applications

The HMC375LP3 is ideal for basestation receivers:

- GSM, GPRS & EDGE
- CDMA & W-CDMA
- DECT

Features

Noise Figure: 0.9 dB

+34 dBm Output IP3

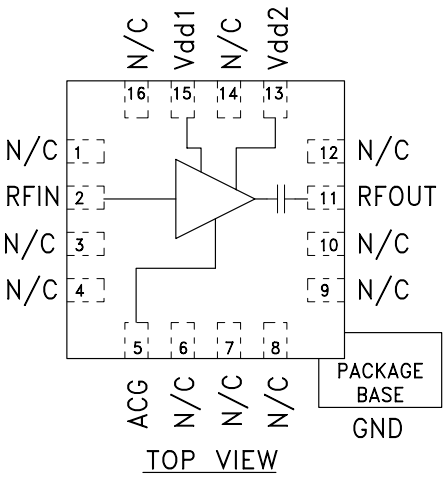
Gain: 17 dB

Very Stable Gain vs. Supply & Temperature

Single Supply: +5.0 V @ 136 mA

50 Ohm Matched Output

Functional Diagram



General Description

The HMC375LP3 high dynamic range GaAs PHEMT MMIC Low Noise Amplifier is ideal for GSM & CDMA cellular basestation front-end receivers operating between 1.7 and 2.2 GHz. This LNA has been optimized to provide 0.9 dB noise figure, 17 dB gain and +33 dBm output IP3 from a single supply of +5.0V @ 136mA. Input and output return losses are 14 dB typical with the LNA requiring minimal external components to optimize the RF input match, RF ground and DC bias. The HMC375LP3 shares the same package with the HMC356LP3 and HMC372LP3 high IP3 LNAs. A low cost, leadless 3x3 mm (LP3) SMT QFN package houses the low noise amplifier.

Electrical Specifications, T_A = +25° C, Vs = +5V

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		1.8 - 1.9			1.9 - 2.0			2.0 - 2.1			2.1 - 2.2		GHz
Gain	16.5	18.5		15.5	17.5		15	17		13	15		dB
Gain Variation Over Temperature		0.014	0.021		0.014	0.021		0.014	0.021		0.014	0.021	dB/°C
Noise Figure		1.0	1.35		0.95	1.2		0.9	1.2		0.9	1.3	dB
Input Return Loss		12			13			14			15		dB
Output Return Loss		13			16			11			8		dB
Reverse Isolation		35			34			34			34		dB
Output Power for 1dB Compression (P1dB)	16	18.5		16	18.5		15	18		14.5	17.5		dBm
Saturated Output Power (Psat)		19.5			19.5			19.5			19.5		dBm
Output Third Order Intercept (IP3) (-20 dBm Input Power per tone, 1 MHz tone spacing)		34			33.5			33			32.5		dBm
Supply Current (Idd)		136			136			136			136		mA

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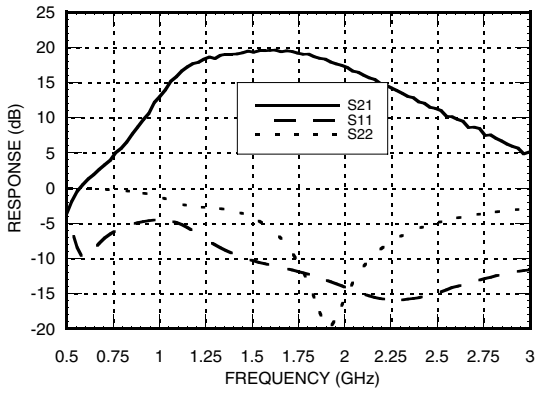
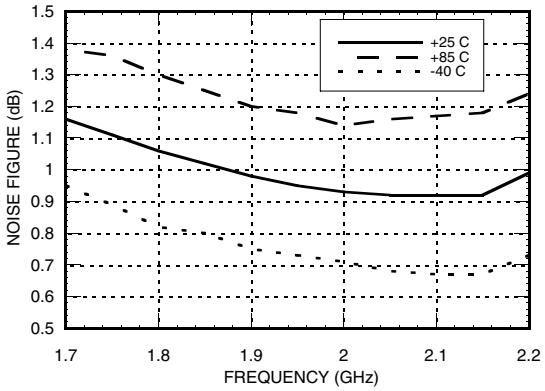
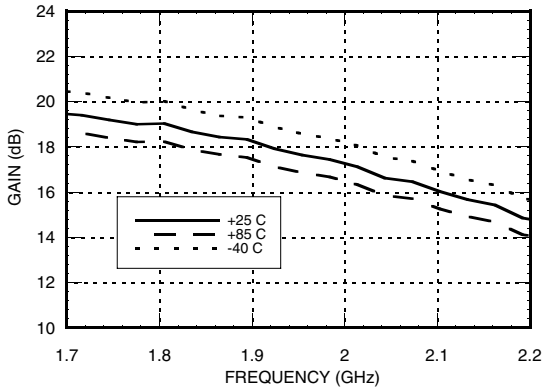
Broadband Gain & Return Loss



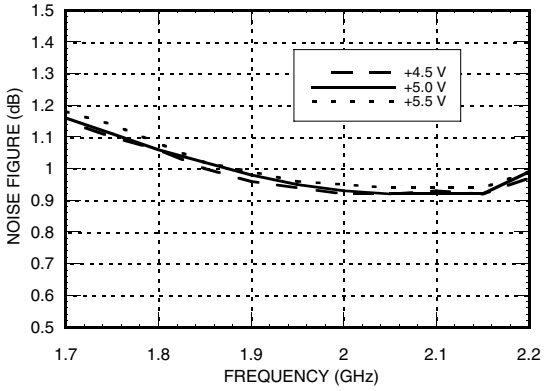
Noise Figure vs. Temperature



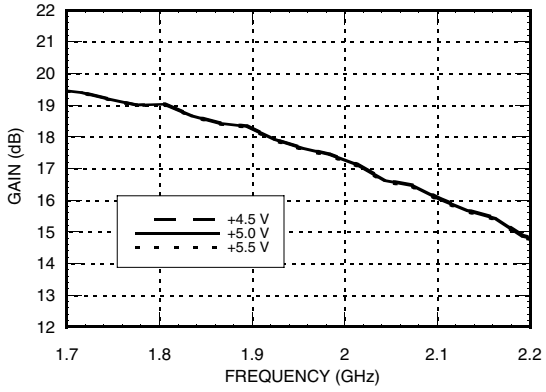
Gain vs. Temperature



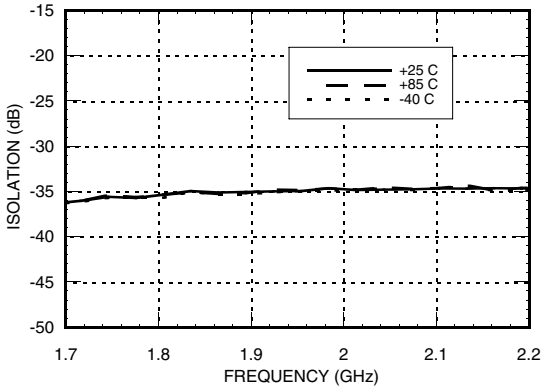
Noise Figure vs. Vdd



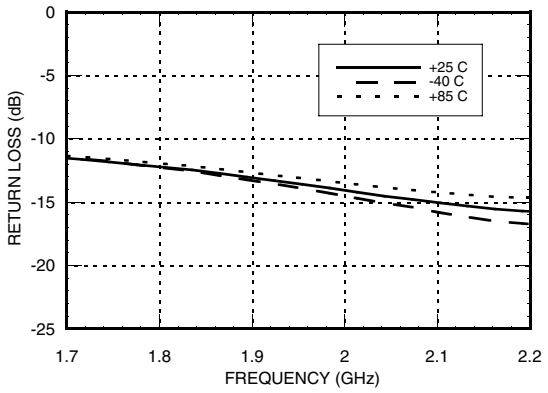
Gain vs. Vdd



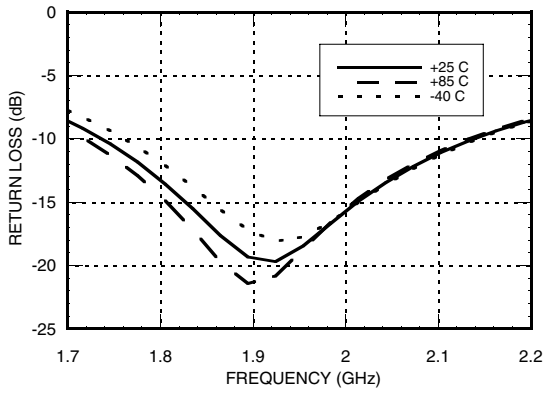
Reverse Isolation vs. Temperature



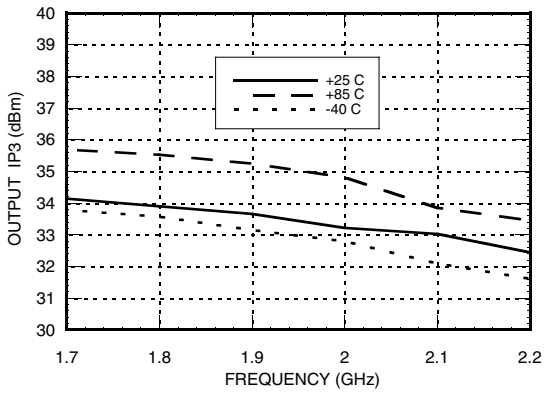
Input Return Loss vs. Temperature



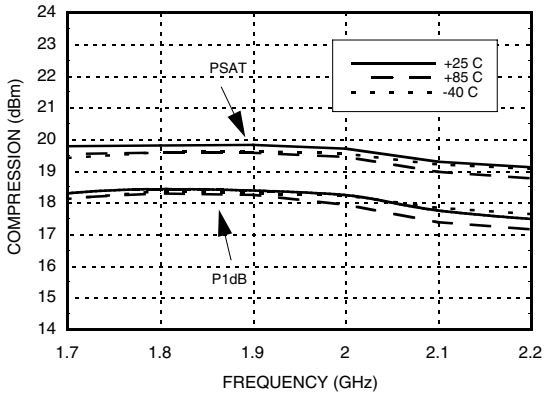
Output Return Loss vs. Temperature



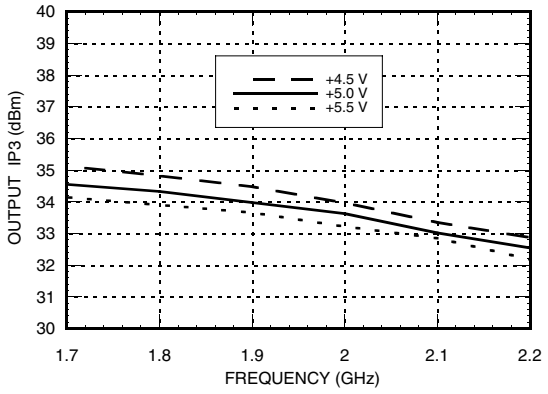
Output IP3 vs. Temperature



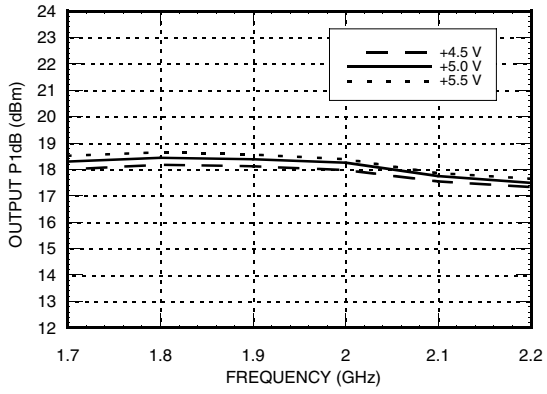
P1dB & PSAT vs. Temperature



Output IP3 vs. Vdd



P1dB vs. Vdd



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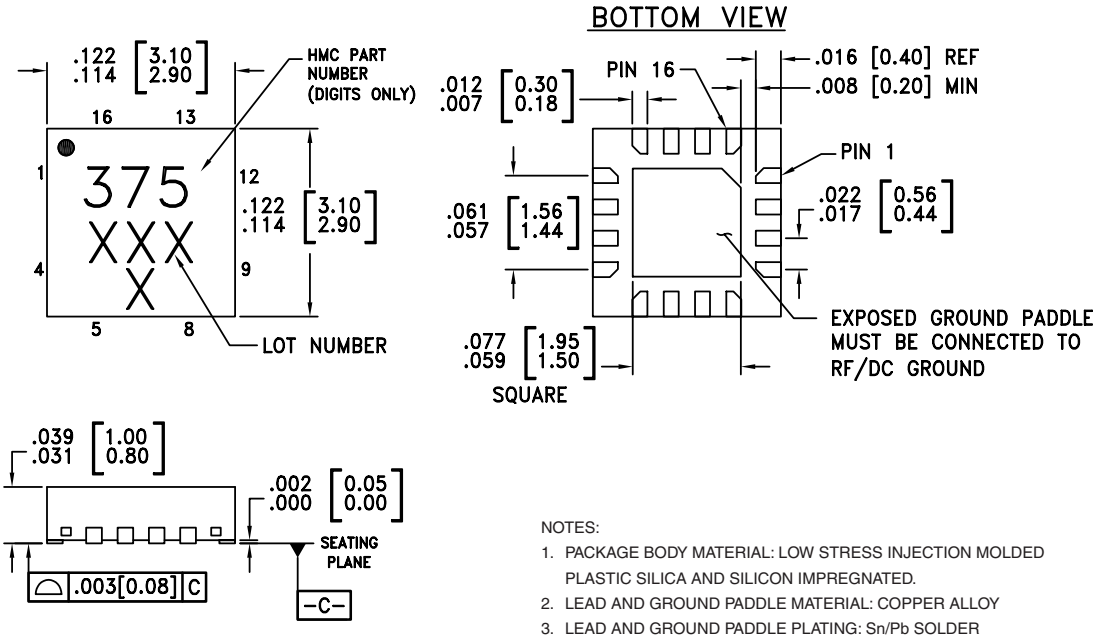
Absolute Maximum Ratings

Drain Bias Voltage (Vdd1, Vdd2)	+8.0 Vdc
RF Input Power (RFin)(Vs = +5.0 Vdc)	+15 dBm
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 15.6 mW/°C above 85 °C)	1.015 W
Thermal Resistance (channel to ground paddle)	64.1 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Typical Supply Current vs. Vdd

Vdd (Vdc)	Idd (mA)
+4.5	135
+5.0	136
+5.5	137

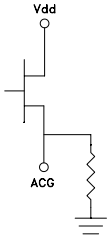
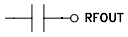
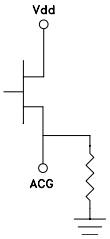
Outline Drawing



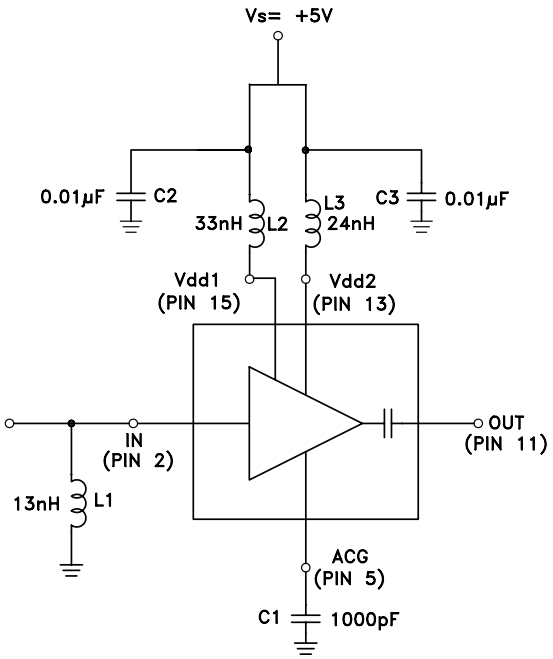
NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY
3. LEAD AND GROUND PADDLE PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
6. CHARACTERS TO BE HELVETICA MEDIUM, 0.35 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Pin Descriptions

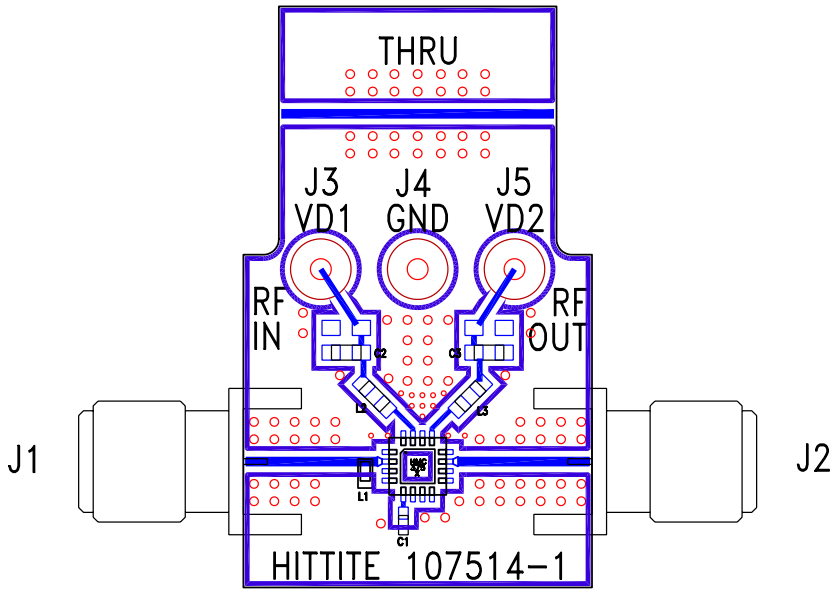
Pin Number	Function	Description	Interface Schematic
1, 3, 4, 6-10,12,14,16	N/C	No connection necessary. These pins may be connected to RF/DC ground.	
2	RF IN	This pin is matched to 50 Ohms with a 13 nH inductor to ground. See Application Circuit.	
5	ACG	AC Ground - An external capacitor of 0.01µF to ground is required for low frequency bypassing. See Application Circuit for further details.	
11	RF OUT	This pin is AC coupled and matched to 50 Ohms.	
13,15	Vdd2, Vdd1	Power supply voltage. Choke inductor and bypass capacitor are required. See application circuit.	
	GND	Package bottom must be connected to RF/DC ground.	

Application Circuit



Note: L1, L2, L3 and C1 should be located as close to pins as possible.

Evaluation PCB



List of Material

Item	Description
J1 - J2	PC Mount SMA RF Connector
J3 - J4	DC Pin
C1	1000 pF Capacitor, 0402 Pkg.
C2, C3	10000 pF Capacitor, 0603 Pkg.
L1	13nH Inductor, 0402 Pkg.
L2	33nH Inductor, 0603 Pkg.
L3	24nH Inductor, 0402 Pkg.
U1	HMC375LP3 Amplifier
PCB*	107514 Eval Board
* Circuit Board Material: Rogers 4350	

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.