

M5L8216P / M5L8226P

T-52-09

MITSUBISHI(MICMPTR/MIPRC)

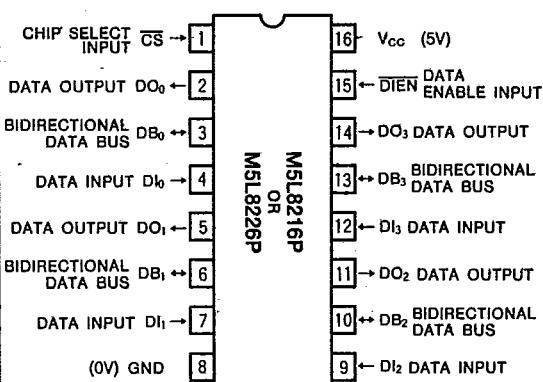
4-BIT PARALLEL BIDIRECTIONAL BUS DRIVERS

DESCRIPTION

The M5L8216P and M5L8226P are 4-bit bidirectional bus drivers and suitable for the 8-bit parallel CPU M5L8085AP.

FEATURES

- Parallel 8-bit data bus buffer driver
- Low input current DIEN, CS: $I_{IL} = -500\mu A$ (max.)
DI, DB: $I_{IL} = -250\mu A$ (max.)
- High output current M5L8216P
DB: $I_{OL} = 55mA$ (max.)
 $I_{OH} = -10mA$ (max.)
DO: $I_{OH} = -1mA$ (max.)
- M5L8226P
DB: $I_{OL} = 50mA$ (max.)
 $I_{OH} = -10mA$ (max.)
DO: $I_{OH} = -1mA$ (max.)
- Outputs can be connected with the CPU M5L8085AP: $V_{OH} = 3.65V$ (min.)
- Three-state output

PIN CONFIGURATION (TOP VIEW)

Outline 16P4

APPLICATION

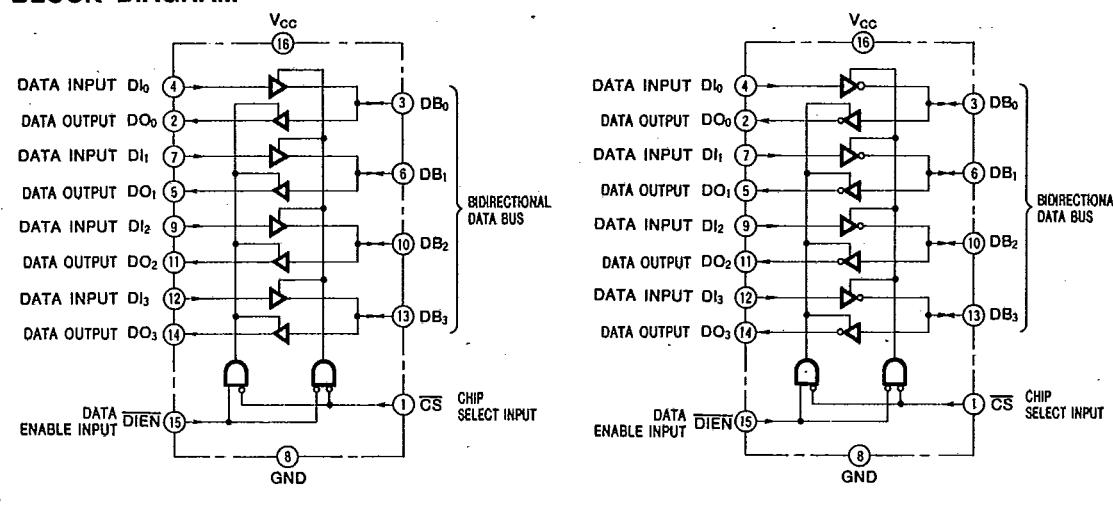
Bidirectional bus driver/receiver for various types of micro-computer systems.

FUNCTION

The M5L8216P is a non-inverting and the M5L8226P is an inverting 4-bit bidirectional bus driver.

When the terminal CS is high-level, all outputs are in high-impedance state, and when low-level, the direction of the bidirectional bus can be controlled by the terminal DIEN.

The terminal DIEN controls the data flow. The data flow control is performed by placing one of a pair of buffers in high-impedance state and allowing the other to transfer the data.

BLOCK DIAGRAM

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4-BIT PARALLEL BIDIRECTIONAL BUS DRIVERS**ABSOLUTE MAXIMUM RATINGS** ($T_a=0\sim75^\circ C$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	7	V
V_I	Input voltage, CS, DIEN, DI inputs		5.5	V
V_I	Input voltage, DB input		V_{CC}	V
V_O	High-level output voltage		V_{CC}	V
P_d	Power dissipation	$T_a=25^\circ C$	700	mW
T_{opr}	Operating free-air temperature range		0~75	°C
T_{stg}	Storage temperature range		-65~+150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a=0\sim75^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Norm	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High-level output current, DO output			-1	mA
I_{OL}	High-level output current, DB output			-10	mA
I_{OL}	Low-level output current, DO output			15	mA
I_{OL}	Low-level output current, DB output			25	mA

ELECTRICAL CHARACTERISTICS ($T_a=0\sim75^\circ C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.95	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V, I_C=-5mA$			-1	V
V_{OH}	High-level output voltage, DO output	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.95V$	$I_{OH}=-1mA$	3.65		V
V_{OH}	High-level output voltage, DB output		$I_{OH}=-10mA$	2.4		V
V_{OL}	Low-level output voltage, DO output		$I_{OL}=15mA$		0.45	V
V_{OL}	Low-level output voltage, DB output		$I_{OL}=25mA$		0.45	V
V_{OL2}	Low-level output voltage, DB output		$I_{OL}=55mA$		0.6	V
	M5L8216P		$I_{OL}=50mA$		0.6	
	M5L8226P					
I_{OZH}	Off-state output current, DO output	$V_{CC}=5.25V$	$V_O=5.25V$		20	μA
I_{OZH}	Off-state output current, DB output		$V_O=0.45V$		100	μA
I_{OZL}	Off-state output current, DO output				-20	μA
I_{OZL}	Off-state output current, DB output				-100	μA
I_{IH}	High-level input current, DIEN, CS inputs	$V_{CC}=5.25V, V_{IH}=4.5V$			20	μA
I_{IH}	High-level input current, DI, DB inputs				10	μA
I_{IL}	Low-level input current, DIEN CS inputs	$V_{CC}=5.25V, V_{IH}=4.5V$			-500	μA
I_{IL}	Low-level input current, DI, DB input				-250	μA
I_{os}	Short-circuit output DO output (Note 2)	$V_{CC}=5.25V, V_O=0V$		-15	-65	mA
I_{os}	Short-circuit output, DB output (Note 2)			-30	-120	mA
I_{oc}	Supply current	$V_{CC}=5.25V$			100	mA
	M5L8216P				100	
	M5L8226P				120	
I_{ocz}	Supply current z				100	
	M5L8216P					
	M5L8226P					

Note 1 : Current flowing into an IC is positive, out is negative.

2 : All measurements should be done quickly, and not more than one output should be shorted at a time.

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4-BIT PARALLEL BIDIRECTIONAL BUS DRIVERS**SWITCHING CHARACTERISTICS** ($V_{CC}=5V \pm 5\%$, $T_A=25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions (Note 3)	Limits			Unit
			Min	Typ	Max	
$t_{PHL(DB-DO)}$	High-to-low and low-to-high output propagation time, from input DB to output DO	$C_L=30pF, R_{L1}=300\Omega, R_{L2}=600\Omega$			25	ns
$t_{PLH(DB-DO)}$						
$t_{PHL(DI-DB)}$	High-to-low and low-to-high output propagation time, from input DI to output DB	M5L8216P M5L8226P	$C_L=300pF, R_{L1}=90\Omega, R_{L2}=180\Omega$		30	ns
$t_{PLH(DI-DB)}$					25	ns
$t_{PHZ(\bar{CS}-DO)}$	High-to-Z and low-to-Z output propagation time, from inputs \bar{DIEN}, \bar{CS} , to output DO	M5L8216P M5L8226P	$C_L=5pF, R_{L1}=10k\Omega, R_{L2}=1k\Omega$		35	ns
$t_{PLZ(\bar{CS}-DO)}$			$C_L=5pF, R_{L1}=300\Omega, R_{L2}=600\Omega$			
$t_{PHZ(\bar{CS}-DB)}$	Output enable time, from inputs \bar{DIEN}, \bar{CS} , to output DB	M5L8216P M5L8226P	$C_L=5pF, R_{L1}=10k\Omega, R_{L2}=1k\Omega$		65	ns
$t_{PLZ(\bar{CS}-DB)}$					54	ns
$t_{PHZ(\bar{CS}-DB)}$	Output disable time, from inputs \bar{DIEN}, \bar{CS} , to output DB	M5L8216P M5L8226P	$C_L=5pF, R_{L1}=90\Omega, R_{L2}=180\Omega$		65	ns
$t_{PLZ(\bar{CS}-DB)}$					54	ns
$t_{PZH(\bar{CS}-DO)}$	Output enable time, from inputs \bar{DIEN}, \bar{CS} , to output DO	M5L8216P M5L8226P	$C_L=300pF, R_{L1}=10k\Omega, R_{L2}=1k\Omega$		65	ns
$t_{PZL(\bar{CS}-DO)}$					54	ns
$t_{PZH(\bar{CS}-DB)}$	Output enable time, from inputs \bar{DIEN}, \bar{CS} , to output DB	M5L8216P M5L8226P	$C_L=300pF, R_{L1}=90\Omega, R_{L2}=180\Omega$		65	ns
$t_{PZL(\bar{CS}-DB)}$					54	ns

TIMING DIAGRAM (Reference level=1.5V)

Note 3 : Test circuit

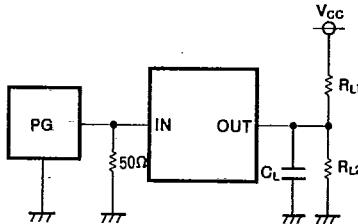
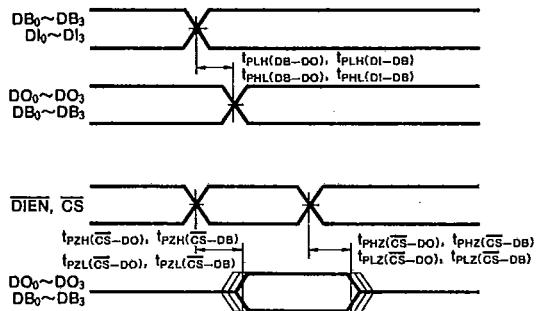
**APPLICATION EXAMPLES**

Fig. 1 shows a pair of M5L8216Ps or M5L8226Ps which are directly connected with the 8080A CPU data bus, and their control signal. Fig. 2 shows an example circuit in which the M5L8216P or M5L8226P is used as an interface for memory and I/O to a bidirectional bus.

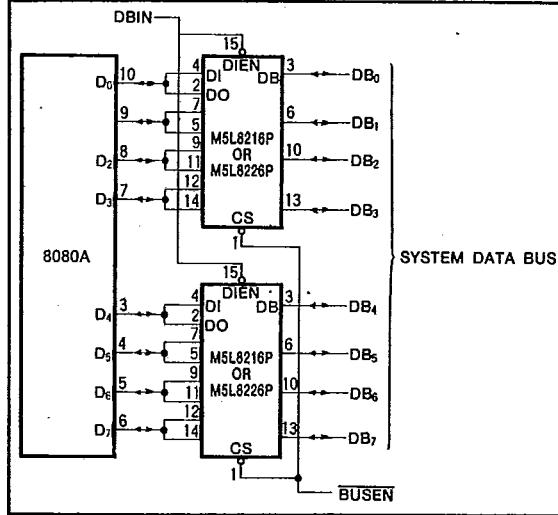


Fig. 1 Data bus buffer

M5L8216P/M5L8226P

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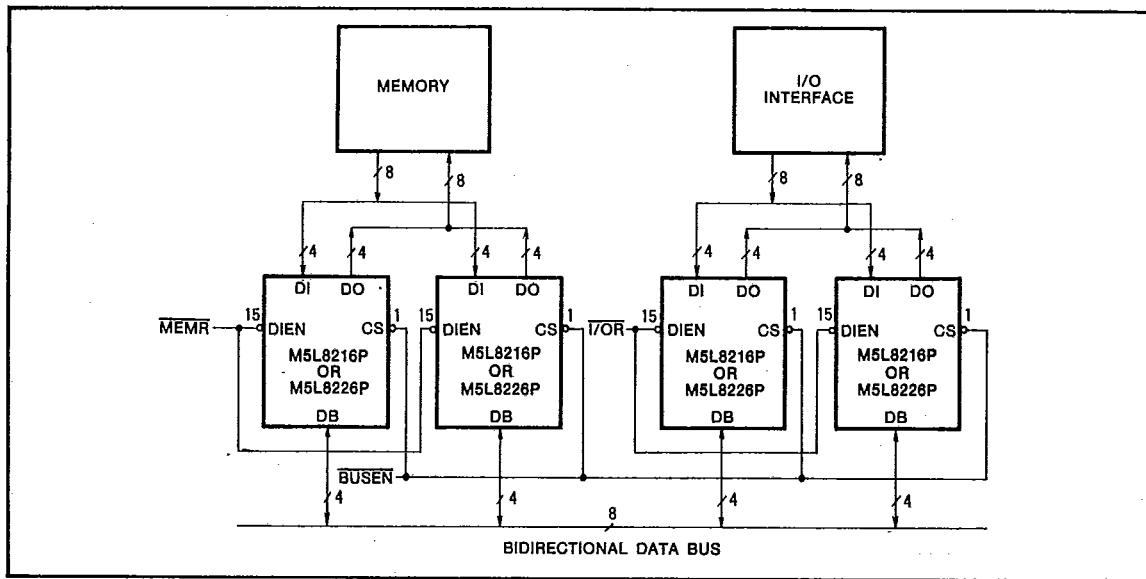
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Fig. 2 Memory and I/O Interface to bidirectional data bus

PRECAUTIONS FOR USE

When the M5L8216P data input or two-way data bus is set to high to disable-output from the two-way bus or data output, care is required as a low glitch of approximate width 10ns will be generated.