

OKI Semiconductor

MSM6690

ROM Interface IC

GENERAL DESCRIPTION

The MSM6690 can drive three devices of 131,072 x 8-bit EPROM or Mask ROM.

The MSM6690 contains a built-in internal address generator circuit and one external clock input that enables continued serial read operations. The internal address counter is automatically incremented by one each read operation. The external serial address input allows 1,024 words to be addressed in the X-direction, and 1,024 words in the Y-direction.

* ROM is selected through $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ pins.

FEATURES

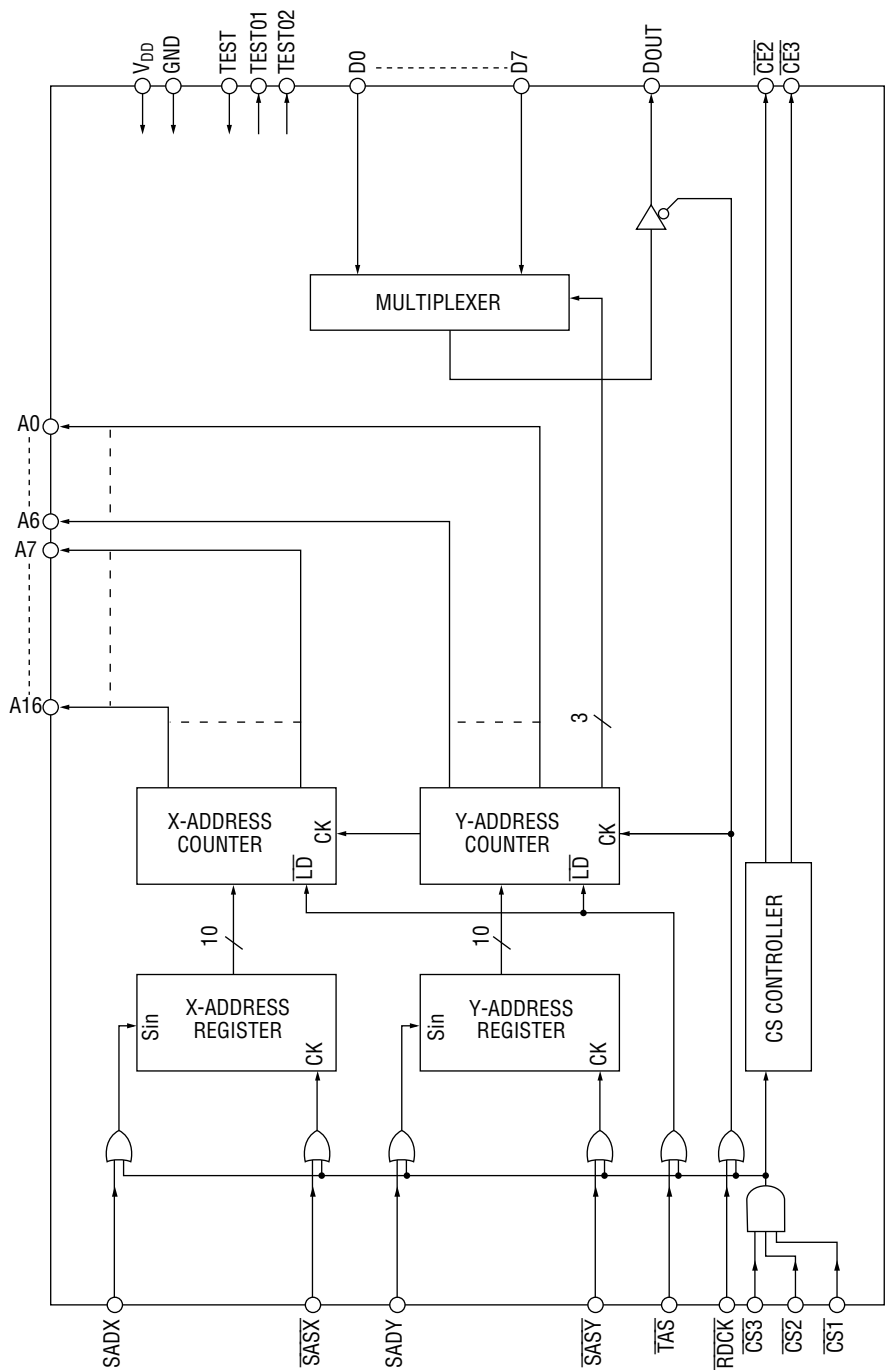
- Capable of driving three devices of 1 Mbit EPROM
- Capable of driving three devices of 1 Mbit Mask ROM
- Supply voltage : Single 5 V
- Package options : 42-pin plastic DIP (DIP42-P-600) (Product name: MSM6690RS)
44-pin plastic QFP (QFP44-P-910-2K) (Product name: MSM6690GS-2K)

* Available combinations

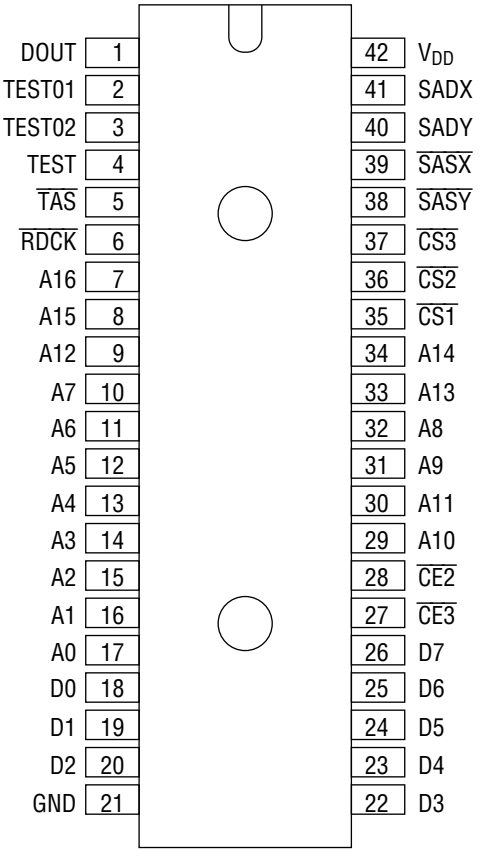
MSM6388/6588	MSM6688/6788/6789A
+	+
MSM6389/6587/6586	(MSM6684/6685)
+	+
MSM6690	MSM6690
+	+
ROM	ROM

Note: When driving the MSM6690 with the MSM6388 or the MSM6588, a serial register (MSM6389, MSM6688 or MSM6586) is required.
In the case of the MSM6688, MSM6788 and MSM6789A, a playback system can be constructed without a serial register (MSM6684 or MSM6685).

BLOCK DIAGRAM

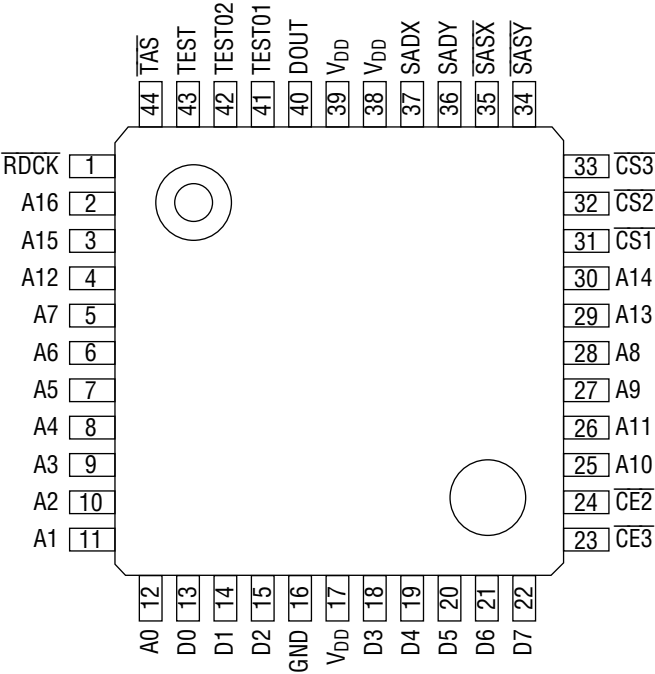


PIN CONFIGURATION (TOP VIEW)



42-Pin Plastic DIP

PIN CONFIGURATION (TOP VIEW) (Continued)



44-Pin Plastic QFP

PIN DESCRIPTIONS

Symbol	Type	Description																									
V _{DD}	—	Power Supply																									
GND	—	Ground																									
SADX	I	(SERIAL ADDRESS) Starting X address. 1024 words are addressed, and 1024 address data can be input as serial data of 10 bit (AX0 to AX9) via SADX pin.																									
SADY	I	(SERIAL ADDRESS) Starting Y address. 1024 words are addressed, and 1024 address data can be input as serial data of 10 bit (AY0 to AY9) via SADY pin.																									
SASX	I	(SERIAL ADDRESS STROBE) Clock to load X address's serial address data to internal register.																									
SASY	I	(SERIAL ADDRESS STROBE) Clock to load Y address's serial address data to internal register.																									
TAS	I	(TRANSFER ADDRESS STROBE) Serial address data loaded in address register, to internal address counter. X address and Y address data are loaded at fall of TAS pin.																									
RDCK	I	(READ CLOCK) Clock to read data in data register. Internal operation starts on falling edge of RDCK, and data in the data register is output via DOUT pin. And internal address counter is automatically incremented by one due to the falling of RDCK.																									
DOUT	O	(DATA OUT) In case CS1, CS2 and CS3 are all at "H" level, or RDCK is at "H" level data output pin is always at high impedance state. When "H" level data or "L" level data is read out, output pin is set to "H" level or "L" level and its read data is kept until RDCK turns to "H" level.																									
CS1 CS2 CS3	I	(CHIP SELECT) Three ROMs selection. <table><tr><th>CS1</th><th>CS2</th><th>CS3</th><th>CE2</th><th>CE3</th></tr><tr><td>L</td><td>—</td><td>—</td><td>H</td><td>H</td></tr><tr><td>H</td><td>L</td><td>—</td><td>L</td><td>H</td></tr><tr><td>H</td><td>H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td></tr></table> When CS1, CS2 and CS3 are all set to "H" level, all input/output pins become disabled. By use of these pins, three ROM data output pins can be connected in parallel.	CS1	CS2	CS3	CE2	CE3	L	—	—	H	H	H	L	—	L	H	H	H	L	H	L	H	H	H	H	H
CS1	CS2	CS3	CE2	CE3																							
L	—	—	H	H																							
H	L	—	L	H																							
H	H	L	H	L																							
H	H	H	H	H																							
CE2 CE3	O	(CHIP ENABLE) ROM enable. Connect it to ROM's CE.																									
A0 - A16	O	(ADDRESS OUT) ROM address.																									
D0 - D7	I	(DATA IN) ROM data.																									
TEST	I	IC test. Input "L" level data.																									
TEST01 TEST02	O	IC test. Set to open.																									

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C Typical: GND = 0 V	−0.3 to +7.0	V
Input Voltage	V_I		−0.3 to $V_{DD}+0.3$	V
Output Voltage	V_O		−0.3 to $V_{DD}+0.3$	V
Input Current	I_I		−10 to +10	mA
Output Current	I_O		−20 to +20	mA
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Parameter	Symbol	Range	Unit
Power Supply Voltage	V_{DD}	+3.0 to +6.0	V
Operating Temperature	T_{op}	−40 to +85	°C

ELECTRICAL CHARACTERISTICS

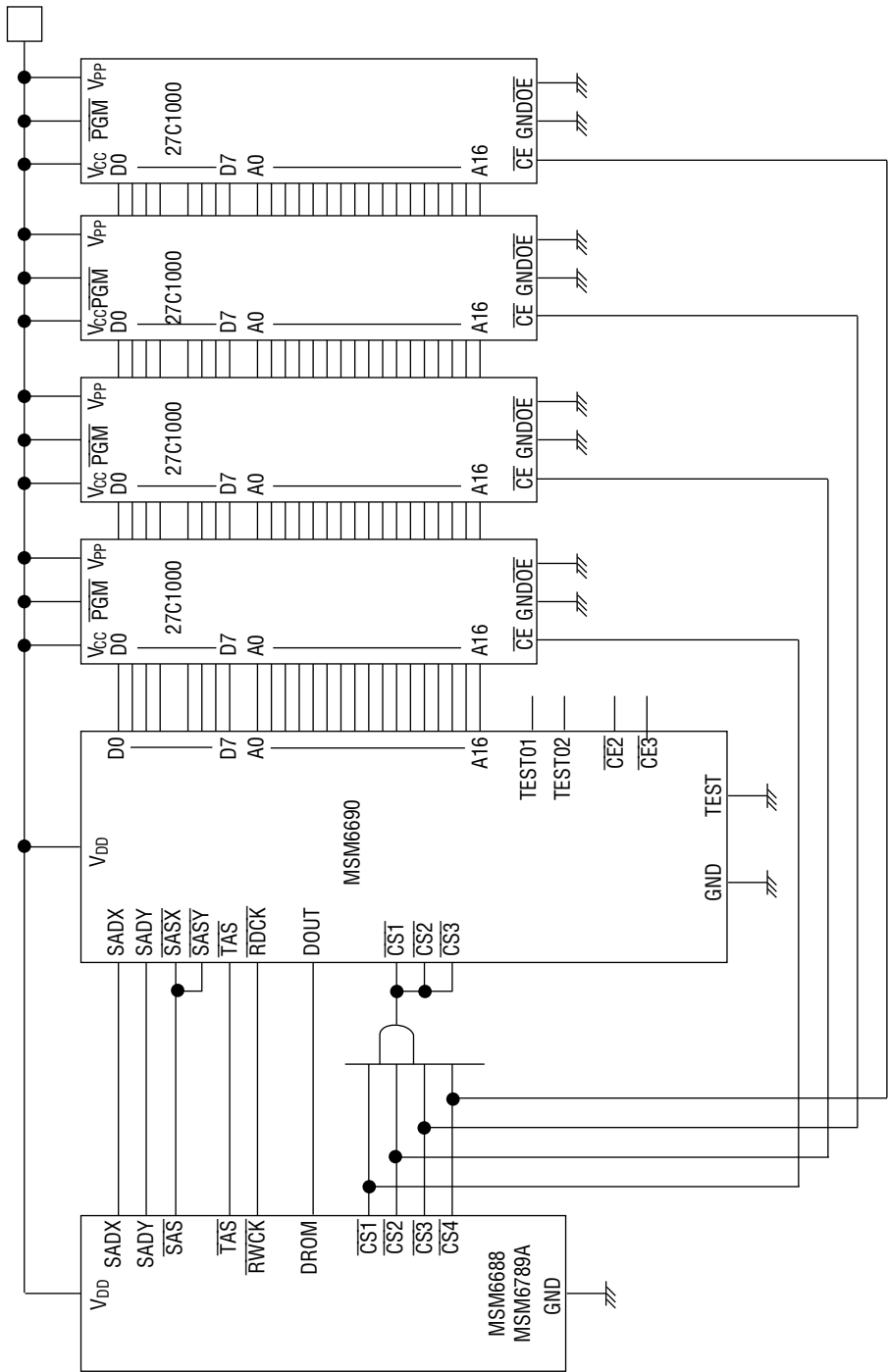
DC Characteristics

(V_{DD} = 5.0 V ± 10%, GND = 0 V, Ta = −40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.*	Max.	Unit
"H" level Input Voltage	V_{IH}	CMOS level input	3.5	—	$V_{DD}+0.3$	V
"L" level Input Voltage	V_{IL}	CMOS level input	−0.3	—	1.5	V
"H" level Input Current	I_{IH}	$V_{IH} = V_{DD}$	—	0.01	10	μA
"L" level Input Current	I_{IL}	$V_{IL} = GND$	−10	−0.01	—	μA
3-state Output Leak Current (with open drain output)	I_{OZH}	$V_{OH} = V_{DD}$	—	0.01	10	μA
	I_{OZL}	$V_{OL} = GND$	−10	−0.01	—	
"H" level Output Voltage	V_{OH}	$I_{OH} = -5.0\text{ mA}$	2.4	4.2	V_{DD}	V
"L" level Output Voltage	V_{OL}	$I_{OL} = 5.0\text{ mA}$	GND	0.24	0.5	V
Supply Current at Standby	I_{DS}	Output open $V_{IH} = V_{DD}$ $V_{IL} = GND$	—	0.1	100	μA
Supply Current at Operating	I_{DD}	—	—	—	2	mA

* Typical operation is with V_{DD} = 5.0 V, Ta = 25°C

APPLICATION CIRCUITS (Continued)



Example of application circuit where MSM6688/6789A and four 1-Mbit EPROMs are connected.